Effect of Power Noise on Multi-Gigabit Serial Links

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Introduction

This paper presents a proof-of-concept analysis that was performed to test the hypothesis that a typical printed circuit board (PCB) and package power distribution system (PDS) has a significant impact on the signal quality of a 10Gbps serial link. In addition to the presence of the non-ideal PDS, a noise source was also set up to inject noise current into the PDS, and its result on the serial link signal quality was analyzed.

The following sections are included:

- Technical approach
- Test vehicle description
- Results
- Conclusions
- Appendix

Technical Approach

The basic approach to this analysis was to mimic some of the general design practices observed in the industry, and lay out a representative package and PCB layout. The coupled differential signals would be extracted together with the full PDS using Sigrity's PowerSI software. The resulting S-parameters would then be incorporated into a serial link topology in Sigrity's Channel Designer software. A realistic voltage regulator module (VRM) would be connected to the PCB to supply power to the serializer/deserializer (SerDes) transmitter (Tx) and receiver (Rx) through the package PDS.

With this topology in place, a noise current source would be connected to a point on the PCB PDS power plane, and the amplitude of this current swept to observe its effect on a 10Gbps serial link with Feed Forward Equalization (FFE) at the Tx and Decision Feedback Equalization (DFE) at the Rx.

Test Vehicle Description

The PCB layout is shown below.
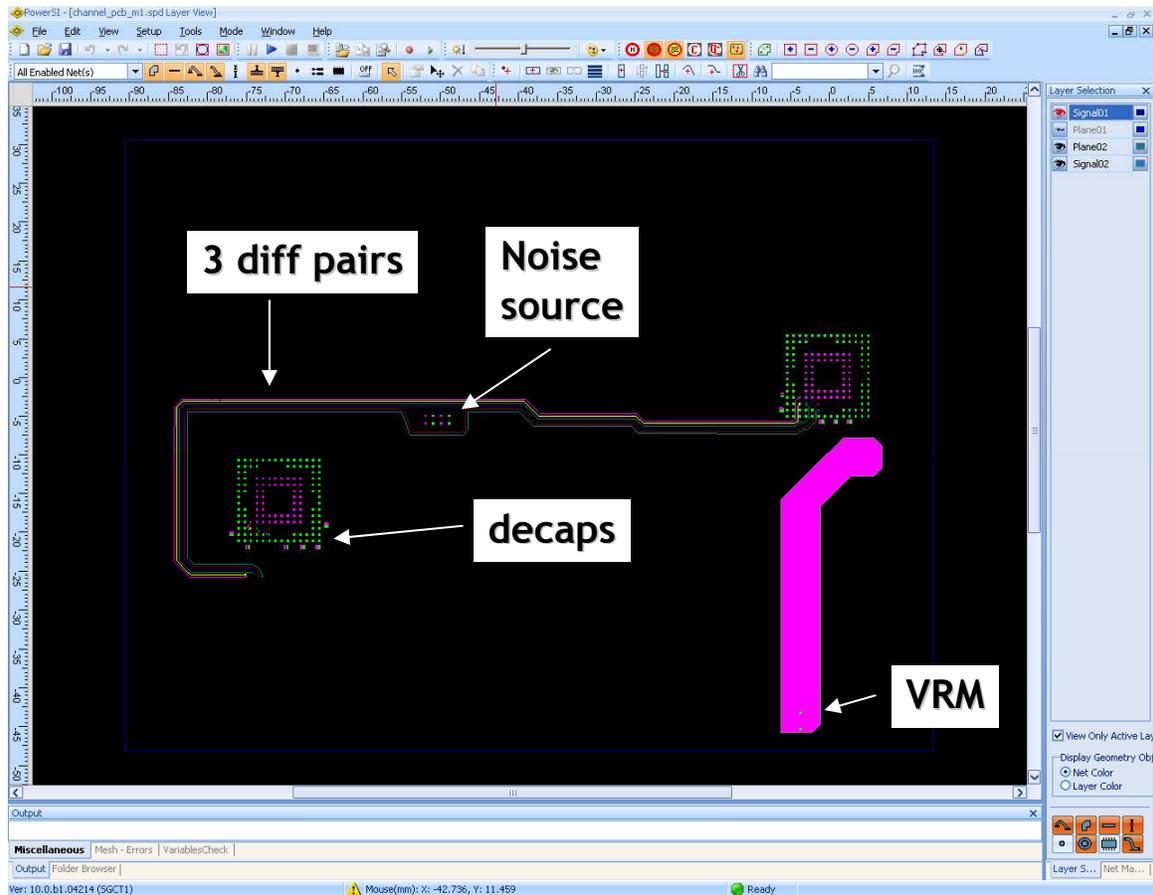
PCB layout of test vehicle

The three differential pairs are routed with 4 mil lines and 6 mil spaces on typical FR4 materials for a length of about 5 inches. Several 0.1uF decoupling caps were placed around each component, and a location for the noise source was placed about halfway between the driving and receiving components. The VRM was located in the lower right-hand corner of the PCB, and connected to the power plane with a large copper shape.

The PCB stack-up is shown below.

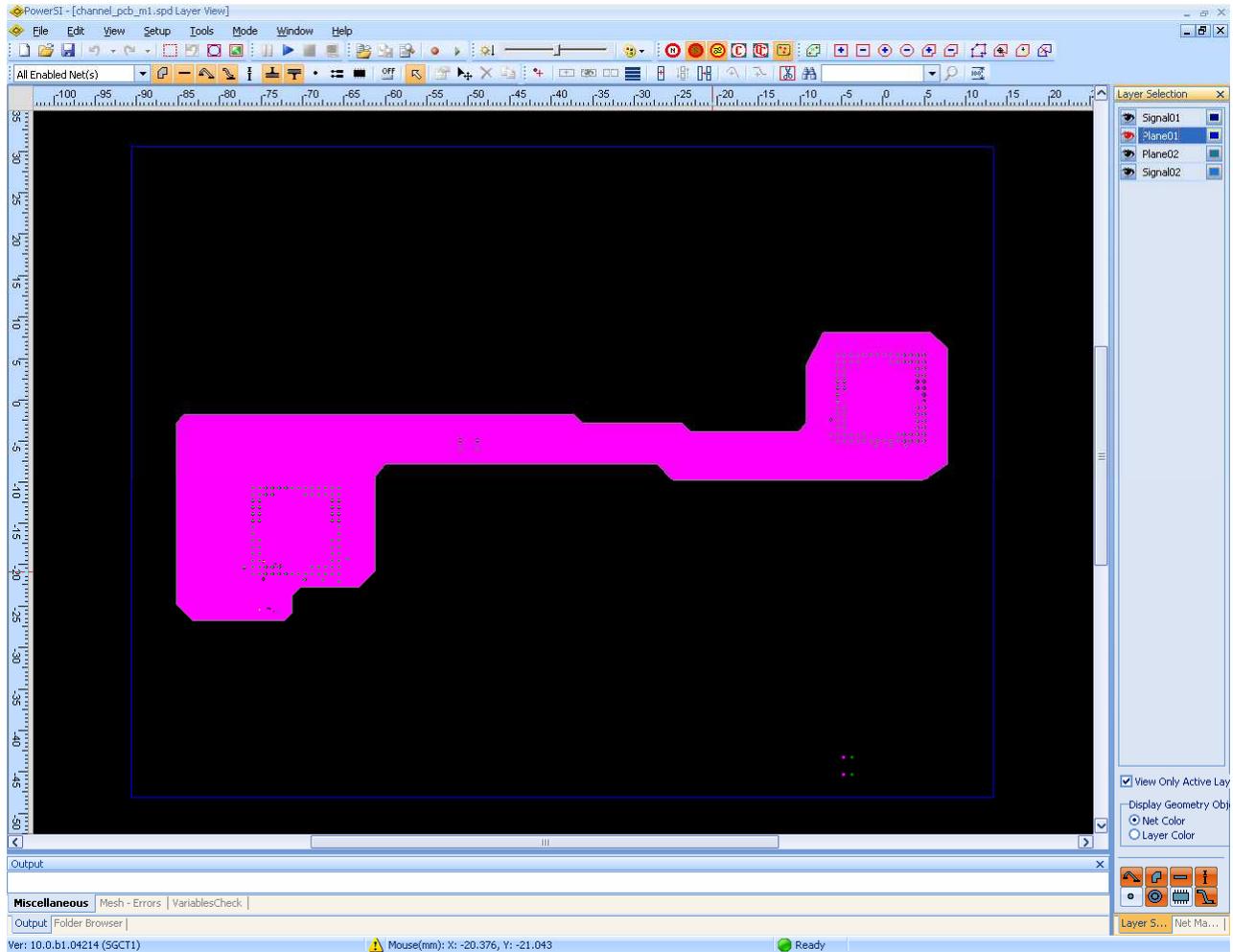| I..	Color	Layer Icon	Layer Name	Thickness(mil)	Material	Conductivity(S/m)	Permittivity	Loss Tangent	Fill-in Dielectric	Shape Name	TraceWidth(mil)
1			Medium$14	0.7			2.5	0.035			
2			Signal01	1.7		5.8e+007				PseudoNull...	4
3			Medium01	3.2			3.7	0.035			
4			Plane01	1.2		5.8e+007				Shape001	
5			Medium02	49			4	0.035			
6			Plane02	1.2		5.8e+007				Shape002	
7			Medium03	3.2			3.7	0.035			
8			Signal02	1.7		5.8e+007					4
9			Medium04	0.7			2.5	0.035			

Total Thickness: 6.2600e+001 mil

Unit: mil ▾ ☐ Enforce causality   View Material

Import   OK   Cancel

PCB stack-up

The ground plane covered the entire 3rd layer, while the power plane on the 2nd layer only surrounds the components and the routing, as shown below.

PCB power plane

The package layout also uses 4 mil trace routing for 100 ohm differential impedance, similar to that for the PCB. The package trace routing is shown below.
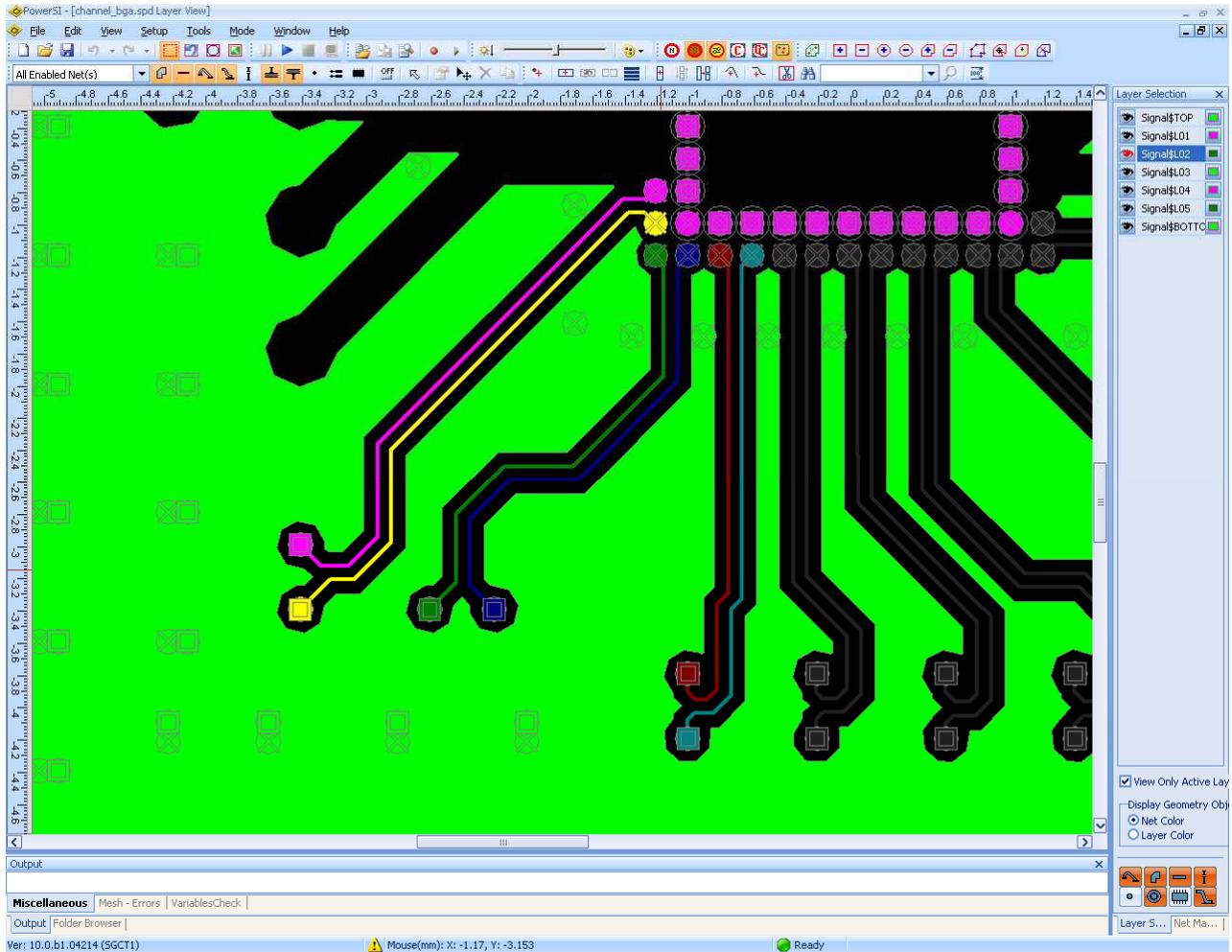
Package signal routing

The stack-up used for the package is shown below. Routing was done on the highlighted layer.

I.	Color	Layer Icon	Layer Name	Thickness(mm)	Material	Conductivity(S/m)	Permittivity	Loss Tangent	Fill-in Dielectric	Shape Name	Trace Width(mm)
1			Signal$TOP	0.12		4.6e+006					0.1
2			Medium$2	0.025			3.7	0.02			
3			Signal$L01	0.015		5.8e+007				Shape$L01	0.1
4			Medium$DRILL_1	0.035			3.1	0.02			
5			Signal$L02	0.015		5.8e+007				Shape$L02	0.1
6			Medium$DRILL_2	0.035			3.1	0.02			
7			Signal$L03	0.021		5.8e+007				Shape$L03	0.1
8			Medium$DRILL_3	0.8			4.2	0.02			
9			Signal$L04	0.021		5.8e+007				Shape$L04	0.1
10			Medium$DRILL_4	0.035			3.1	0.02			
11			Signal$L05	0.015		5.8e+007				Shape$L05	0.1
12			Medium$DRILL_5	0.035			3.1	0.02			
13			Signal$BOTTOM	0.015		5.8e+007				Shape$BO...	0.1
14			Medium$14	0.025			3.7	0.02			

Total Thickness: 1.2120e+000 mm

Unit: mm ▼ ☐ Enforce causality View Material

Import   OK   Cancel

Package stack-up

S-parameters were extracted with PowerSI up to 20GHz and used to build the Channel Designer topology shown below.
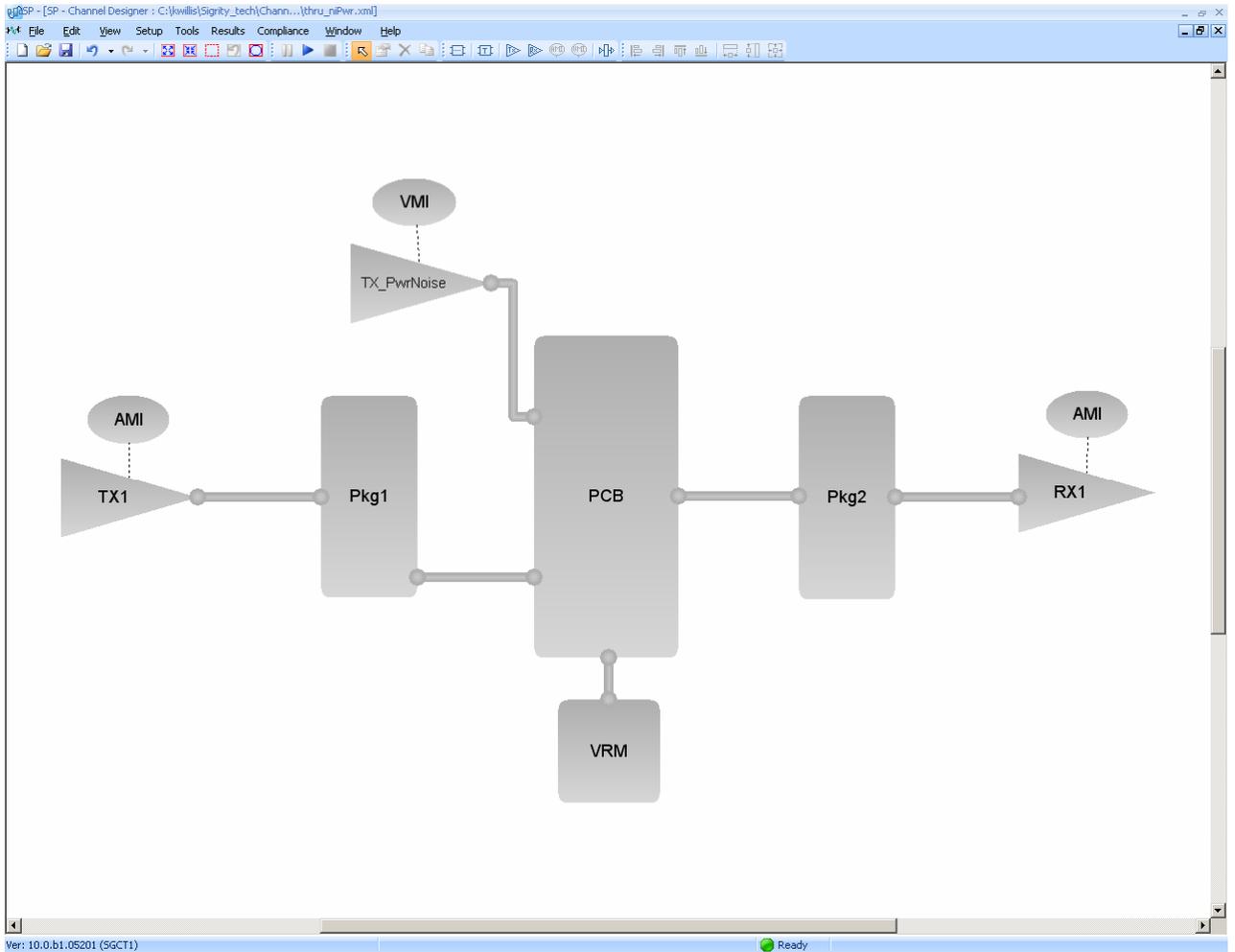
Serial link topology

One of the three differential pairs is shown above as the "through" channel for the signals. The "AMI" bubbles associated with the through channel Tx and Rx represent the algorithmic models used for the FFE and DFE, respectively. The two unused differential pairs were terminated off with 50 ohms to ground to avoid any reflections from noise induced on those traces.

The Tx circuit model initially used was a simple behavioral Spice model for a current-mode logic (CML) driver, which consisted of a pullup resistor, a pulldown dependent current source, and some pad capacitance on each leg. The Rx circuit model consisted of pullup resistors and pad capacitance.
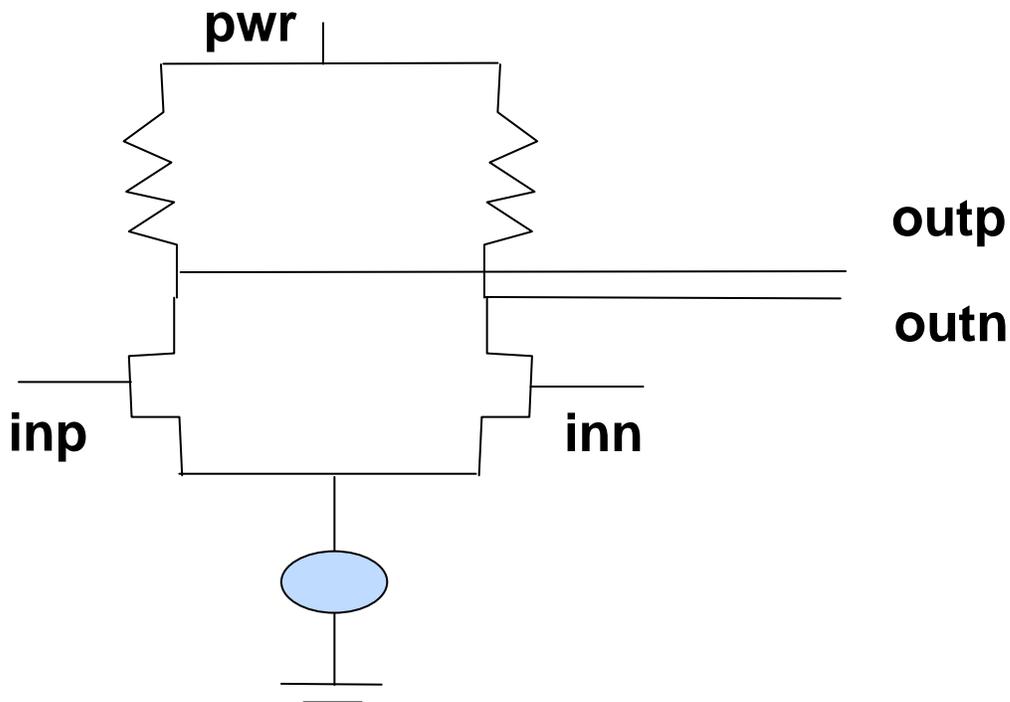

Tx circuit diagram

The "VRM" block in the schematic contains a typical VRM subcircuit borrowed from the paper "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology", listed in the "References" section.

The "TX_PwrNoise" block shown above is connected directly to ports in the PDS (see "Noise Source" in the PCB layout figure), and is used to inject current into the PDS to represent power noise. Impulse response techniques are used to characterize this noise injection, as seen in the paper "Statistical Simulation of Power Supply Noise in Multi-Gigabit Systems", listed in the "References" section.

Results

The first simulation that was run was for the "ideal" power scenario, in which an ideal voltage source is directly connected to the Tx and Rx IO models. This essentially represents a perfect power supply on the chip, and is the assumption that signal integrity (SI) tools have generally used. With this as the baseline case, a second simulation was run with the real, non-ideal PDS in place, with the VRM supplying power on the PCB. The comparison of the results is shown below.
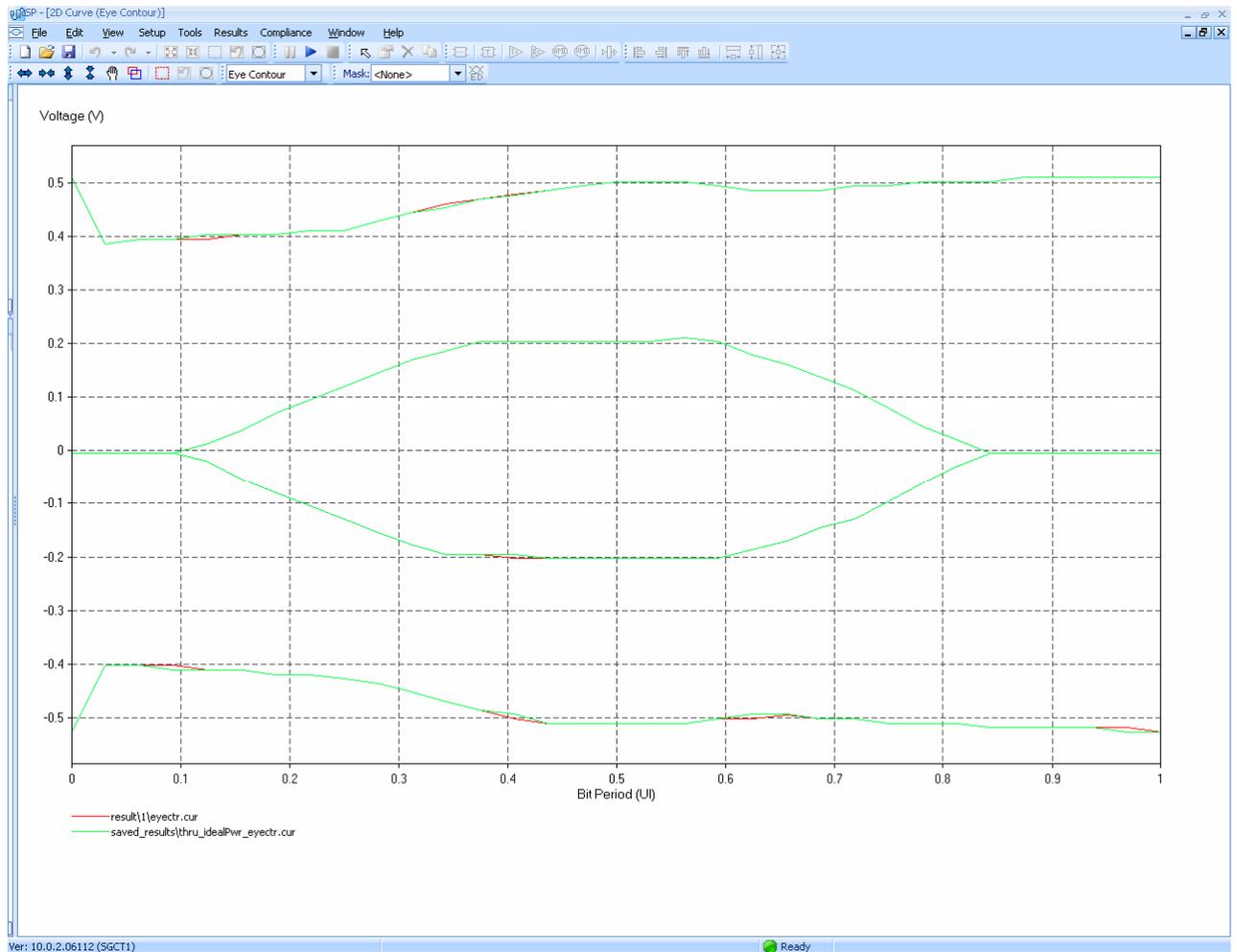
*Ideal power (green) and non-ideal power (red) scenarios*

The presence of the real PDS had minimal effect in this case.

Next, the effect of PDS noise on the eye was analyzed. The power noise current source magnitude was automatically swept from 10mA to 300mA, using a 1Gbps random stimulus pattern, with the goal of mimicking the behavior seen with modern DDR3 memory bus interfaces, which often must co-exist with multi-gigabit serial links. The eye contours produced from these simulation runs are shown below.
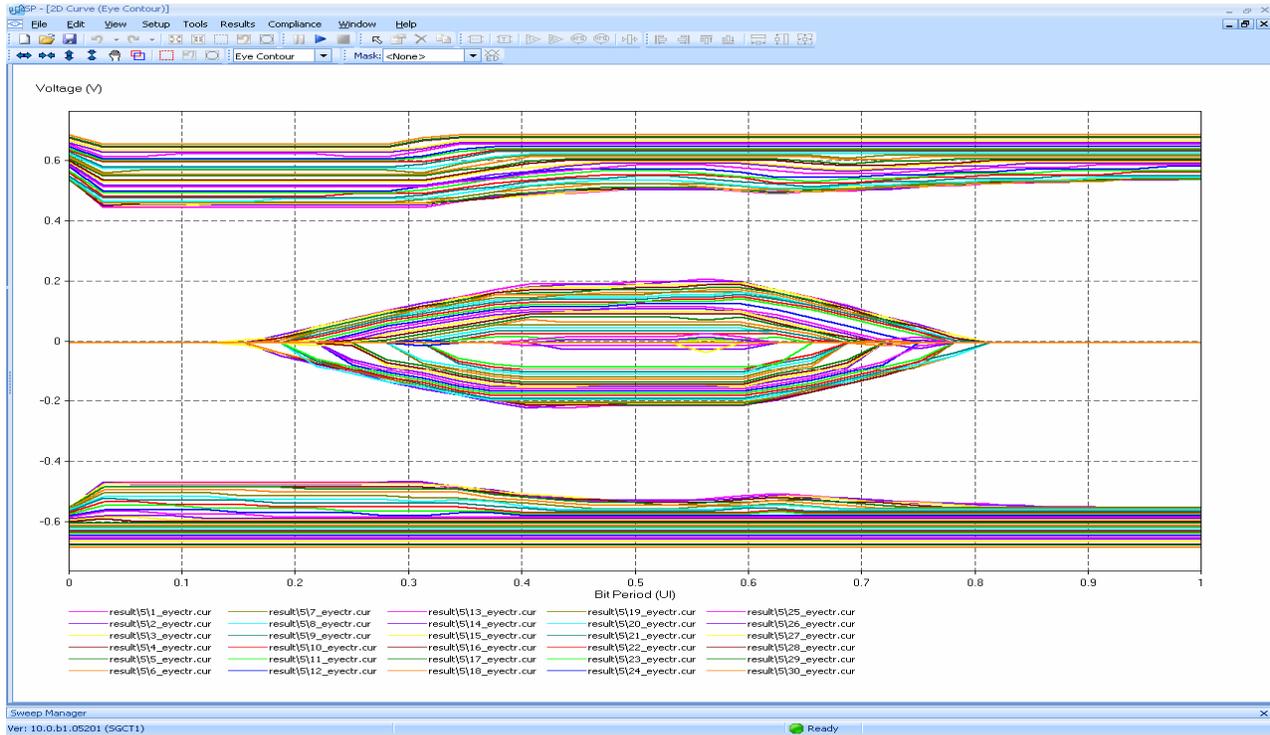
*Eye contours for power noise current from 10mA to 300mA*

The bathtub curves produced from these runs are also shown.
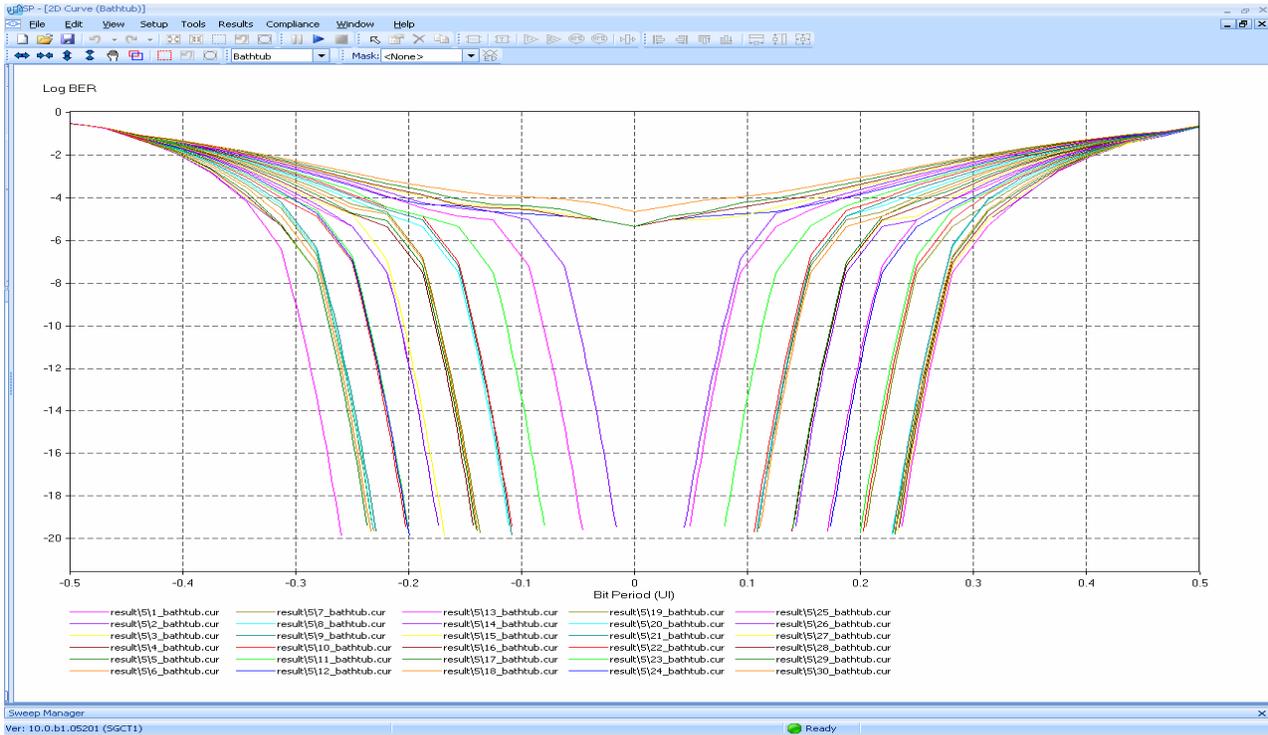
Bathtub curves for power noise current from 10mA to 300mA

Note how the BER consistently worsens as the noise current increases, to the point where the eye becomes fully closed.

Next, the behavioral Tx circuit model was enhanced to enforce a constant total current through the positive and negative legs of the differential driver, which is more representative of how a CML driver behaves. When the sweeps were re-run, the results were significantly different.
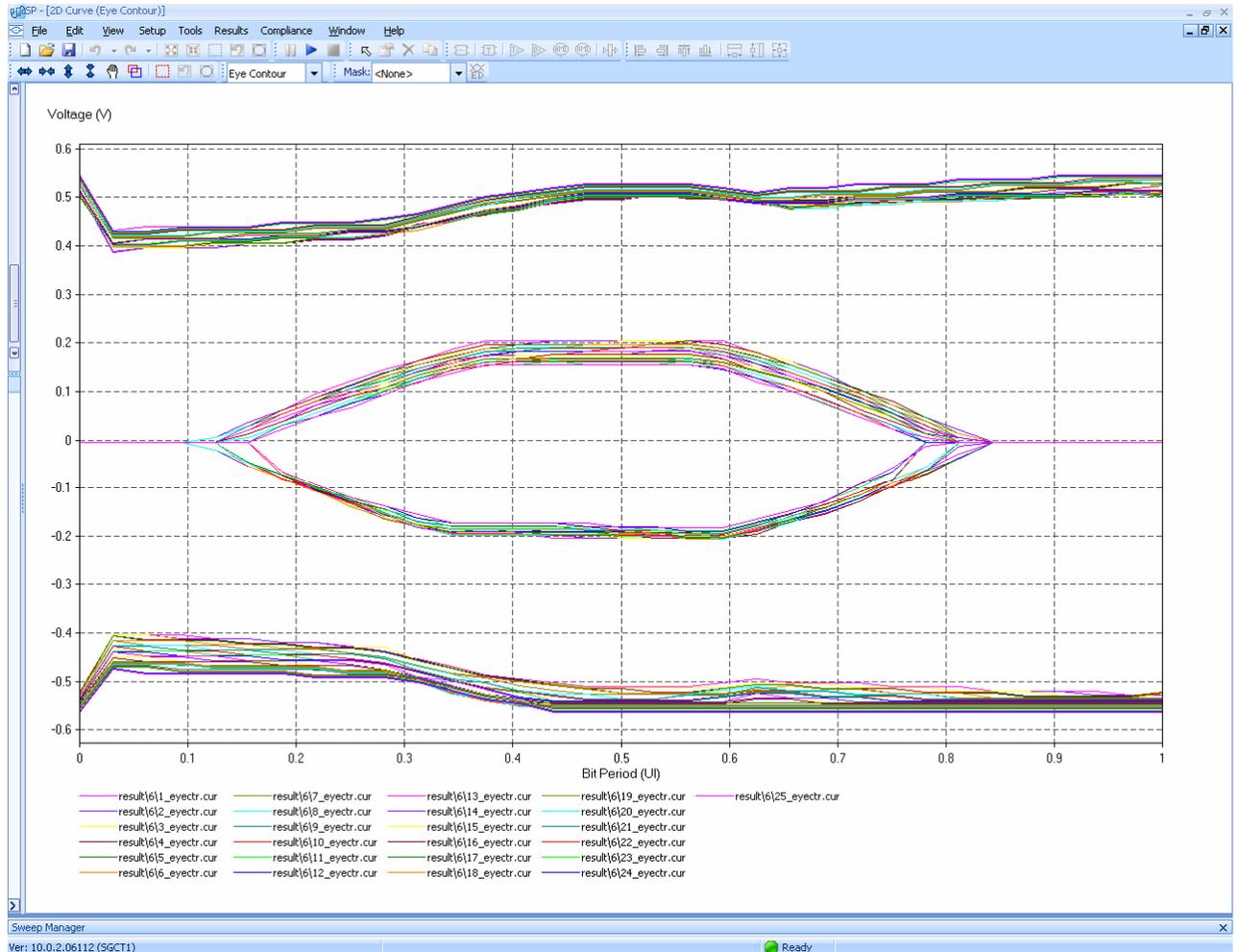

*Eye contours with enhanced Tx CML model*
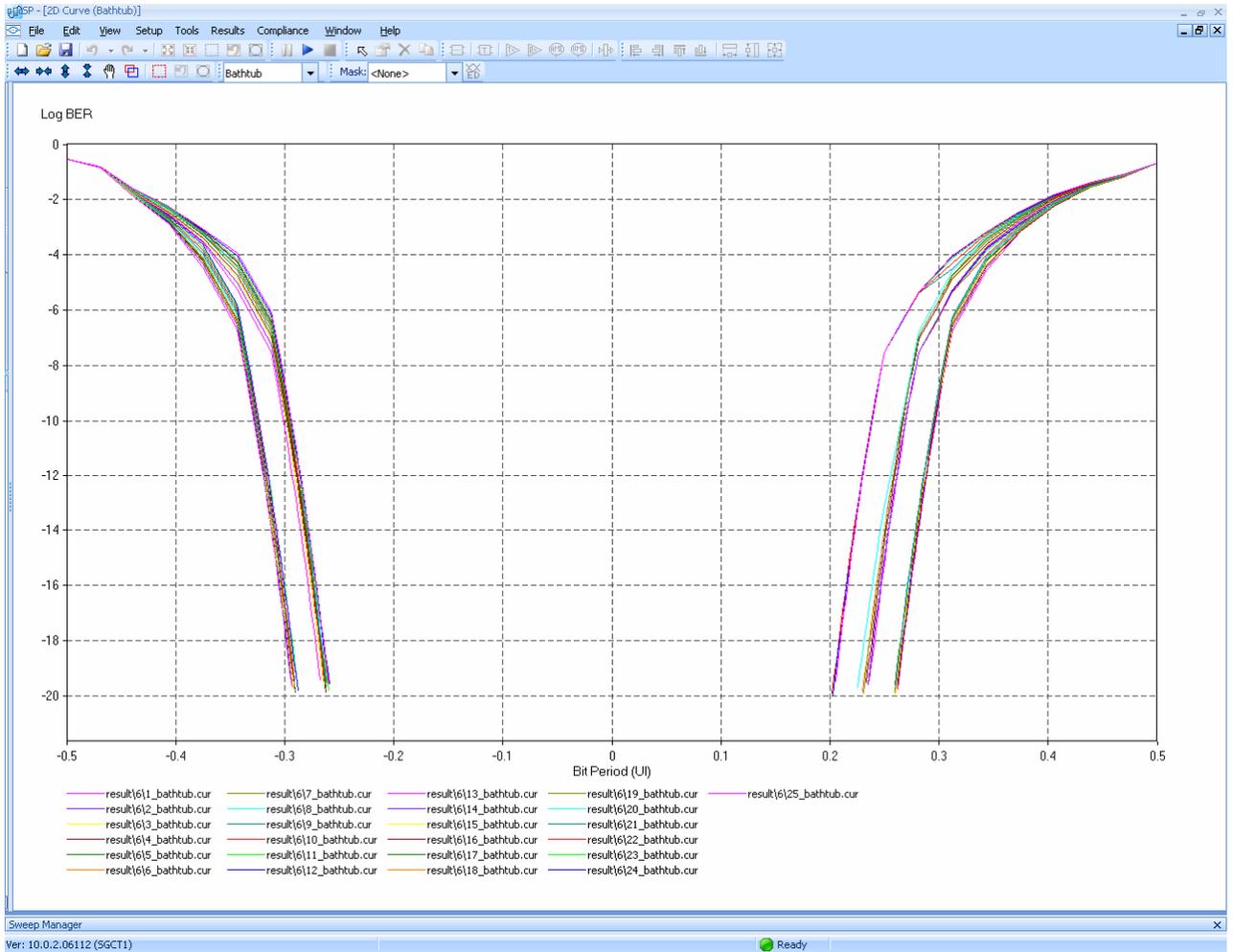
Bathtub curves with enhanced Tx CML model

Note that these results are significantly less pessimistic than the previous run, and more realistic as compared with what you would expect to see in hardware. The Tx circuit model had a significant impact on the results.
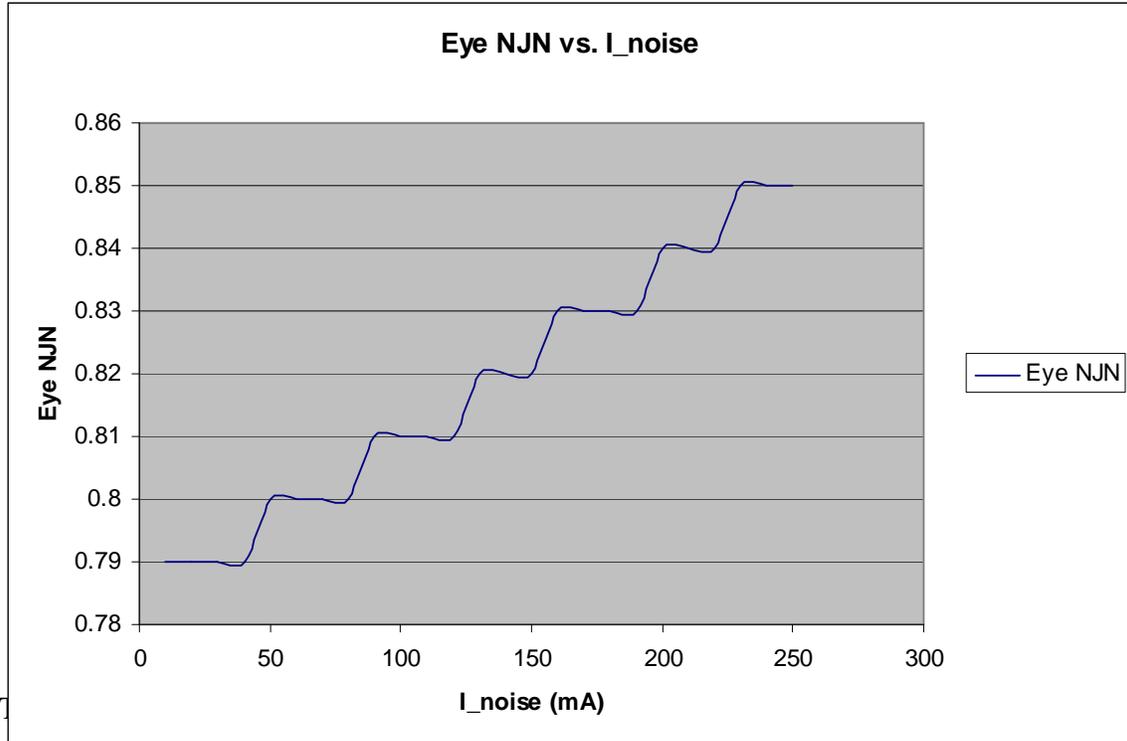
The simulation results were exported to a spreadsheet, where a number of other plots were generated to see the effect of the power noise on the metrics of eye height, eye jitter, and normalized jitter and noise.
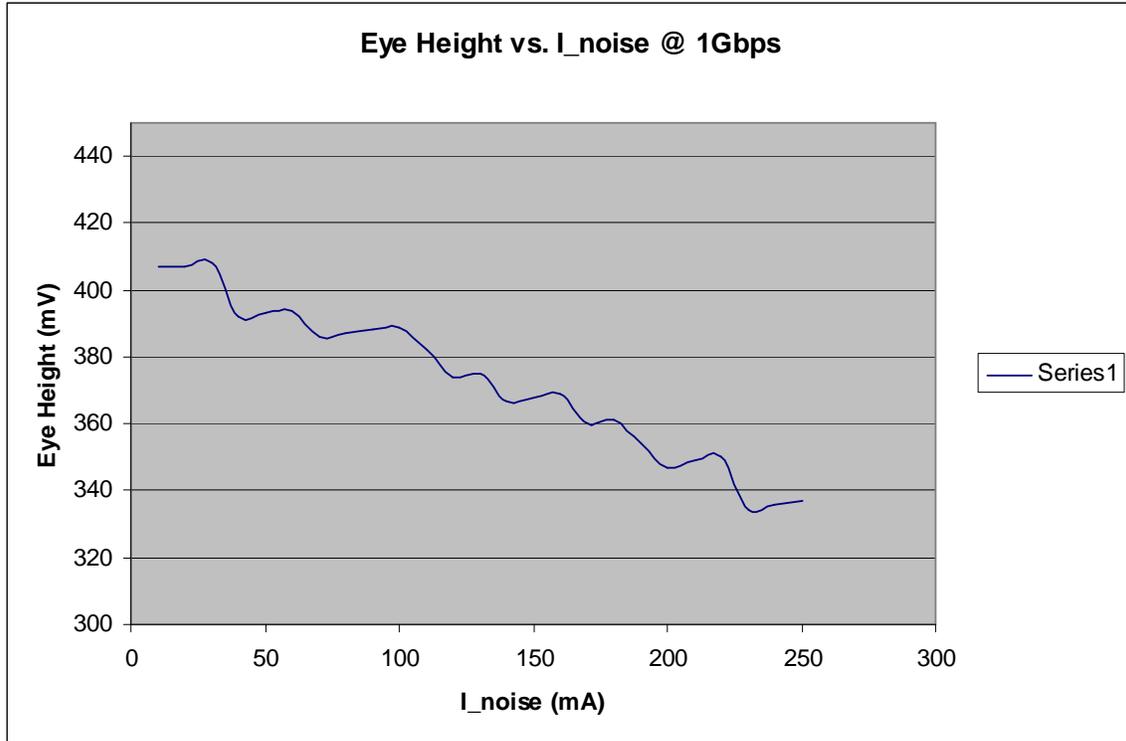
Eye height vs. power noise current
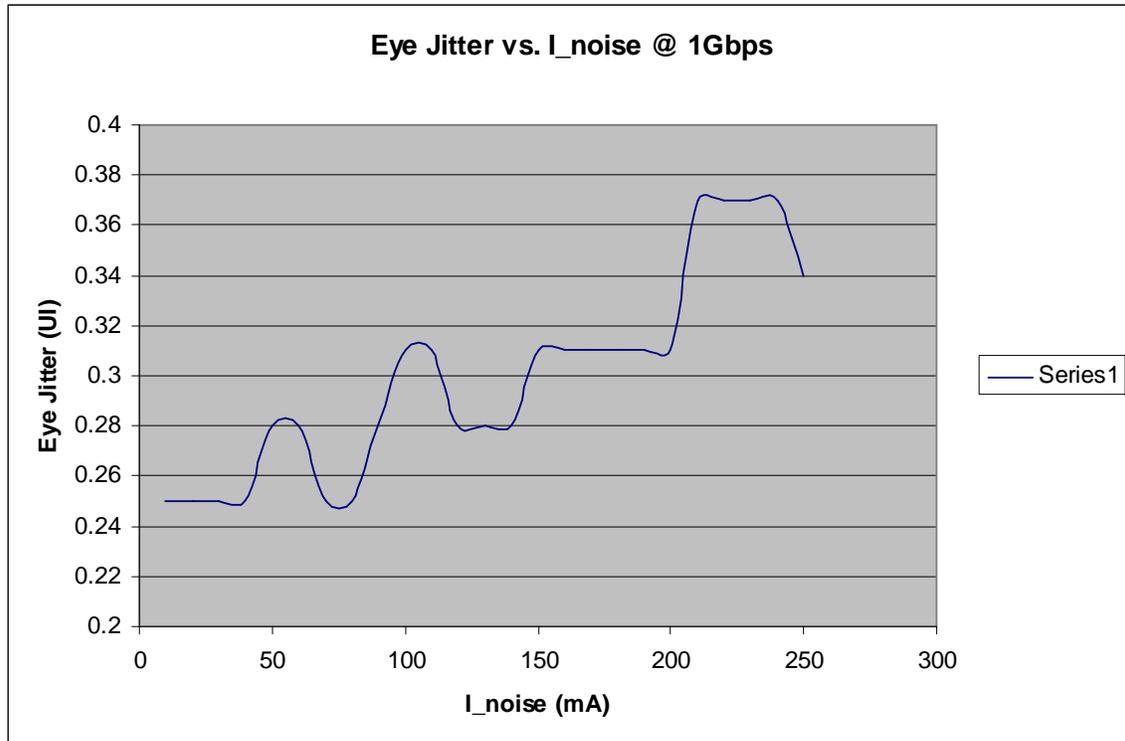
Eye jitter vs. power noise current

Eye NJN vs. I_noise

Normalized jitter and noise vs. power noise current

See the Appendix A for a description of the "normalized jitter and noise" metric used in the chart above.

Conclusions

Simply including the real PDS as part of the serial link topology (without injecting any power noise) had a minimal impact on the signal quality in this case.

Injecting a noise current into the PDS had a fairly dramatic effect on eye quality. In the second set of runs with the enhanced CML Tx model, the eye height dropped by 17% as noise current was injected, and eye jitter increased by about 10%.

It appears that the primary noise coupling mechanism in this case is from the power planes, through the pullup resistors in the Tx, and onto the transmitted signals. The asymmetry in the differential signal routing between the P and N sides of the differential pair accounts for the noise contribution seen at the receiver.

In summary, some conclusions from this initial effort are as follows:

- The "ideal power" assumption appears quite dangerous for multi-gigabit serial links.
- Eye quality can be directly and significantly impacted by the presence of even relatively small noise currents in the PDS.
- Representing the IO circuit models in a "structurally accurate" way (i.e. modeling all the main current paths that exist in them) has a major impact on the results.
- Due to the purposely low-loss nature of a PDS, and therefore its ability to easily propagate noise signals, it appears that PDS noise may rival and even surpass traditional signal-to-signal crosstalk as a main factor in serial link performance.

Appendix A. – Normalized Jitter and Noise

Normalized jitter and noise is a key metric used by Sigrity to evaluate the signal quality of serial links. Refer to the figure below.
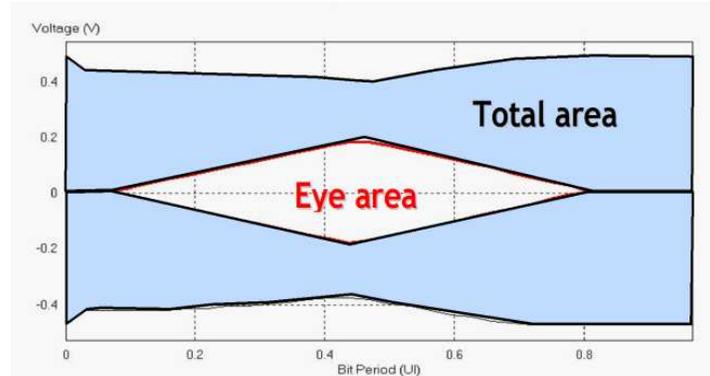
Normalized jitter and noise

Looking at an eye diagram with a window of 1UI, the total area within the outer envelope is computed. Next, the area of the eye opening is computed. The difference between the two is essentially jitter and noise. The percentage of the total area that is comprised of this jitter and noise (i.e. not eye opening) is reported as the "normalized jitter and noise" metric.

References

Larry Smith, Ray Anderson, Doug Forehand, Tom Pelc, and Tanmoy Roy , "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology" (Sun Microsystems)

Wendemagegnehu T. Beyene, Amir Amirkhany, Aliazam Abbasfar, "Statistical Simulation of Power Supply Noise in Multi-Gigabit Systems", DesignCon 2010 (Rambus)