
A New Power Delivery System Design Practice

Wednesday, January 30, 2008|Brad Brim, Sigrity

The design of the PCB's power delivery system (PDS) is growing more complex each day. Continued advances in IC technologies have reduced supply voltages to below 1 volt, with correspondingly reduced power plane noise margins. At the same time, both static and dynamic current requirements have dramatically increased.

These two effects have resulted in a more than 100X reduction in power plane impedance requirements, which are necessary to assure proper PDS performance. Further complications include faster signal rise times, more high-speed I/Os, and the application of multiple high-power components (ASIC, FPGA, CPU) on a single PCB. Given this situation, assuring PDS performance through low-power plane impedance is no easy task.

Despite these complexities, it is possible for the average PCB designer – with access only to the PCB design database and a library of decoupling capacitor components – to implement cost-effective and performance-assured PDS designs with cost savings of 15 to 50% beyond present designs.

Several factors concerning modern PDS designs must be considered in determining how to accomplish this design optimization task. Traditional design procedures and EDA tools also must be examined, because this challenging task cannot be accomplished with the status quo.

PCBs use voltage regulator modules (VRMs) to control external supply voltages. A VRM and its associated bulk capacitors can maintain low power plane impedance from DC to frequencies of 10kHz to 100kHz. Above this frequency, decoupling capacitors (decaps) are responsible for maintaining low power plane impedance. While bulk capacitors simply provide a DC charge reserve for switching currents, decaps form series RLC resonances that provide high-frequency, low-impedance paths between power and ground planes.

To maintain low impedance over a broad frequency range, a broad spectrum of decap resonances must exist. Therefore, a wide range of decap values provides for the best PDS design. The upper frequency for which PCB decaps can maintain low power plane impedance is bounded by the minimum decap value and the minimum PCB loop inductance, typically less than 100MHz.

At frequencies above which PCB decaps are effective, low power plane impedance is maintained for IC switching currents by decaps in-package. These decaps operate in exactly the same manner as PCB decaps – by forming series RLC resonances. Package loop inductances are much lower than for PCBs and, therefore, the maximum frequency for which in-package decaps are effective can be as high as 400MHz. Above this frequency, on-chip decaps must be present to maintain a low power plane impedance.

These frequency behaviors imply that maintaining low power plane impedance over a broad frequency range can be a multi-domain design task, spanning board/package/chip. PCB designers have no control over packaged components and must rely on manufacturers of such components to provide a target impedance (Z_{target}) that the PCB power plane must not exceed. If no such specification is provided, it can be approximated as a ratio of the maximum allowed voltage ripple versus the peak switching current amplitude. The voltage ripple typically is bounded by 5% of the power rail voltage, and the maximum switching current is a quantity provided by the device manufacturer, typically called "I current."

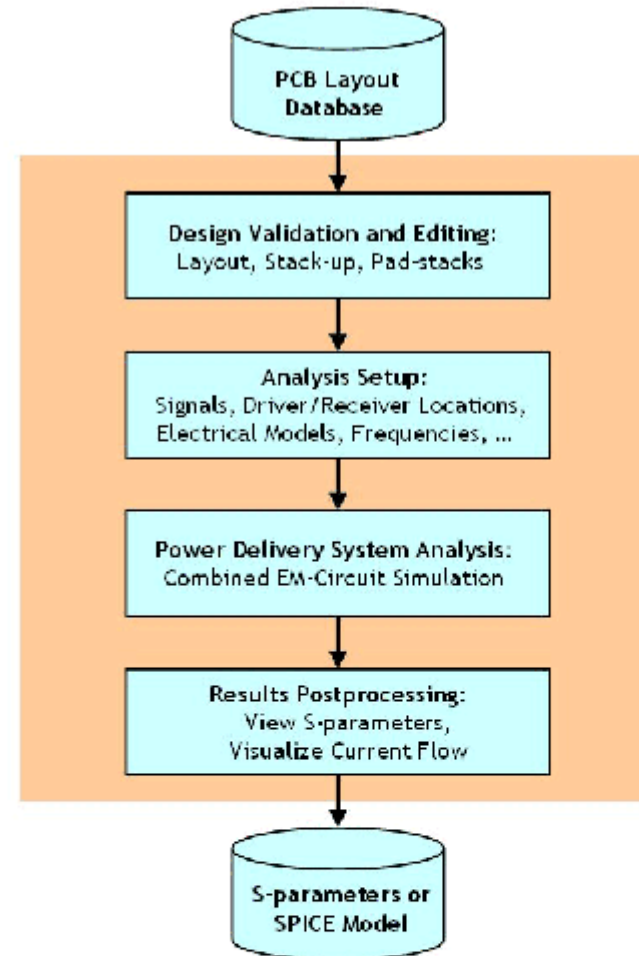
Traditional PDS Design

Many PCB designers rely on heuristic rules for PDS design, some of which are based on false assumptions, resulting in unnecessarily expensive designs with inadequate broadband performance. One well-founded heuristic rule is to place decaps as close as possible to power pins that carry high switching currents. This rule too often is interpreted as "place a decap at every high current power pin," and even generalized to "place decaps in any location near a device where area is available."

Another less-well-founded heuristic rule says apply the same value of decap across the entire PCB, to support volume pricing advantages. A common generalization of this rule is to apply the highest capacitance available for this single component type. However, to achieve high PDS performance, it is more effective to apply a broad range of decap values. These heuristic selection rules provide a power plane impedance far below Z_{target} near only one frequency, away from which the power plane impedance quickly exceeds Z_{target} . This single frequency can be surprisingly low if large-valued decaps are applied.

Many enterprise design flow companies provide utilities to support the efficient implementation of these heuristic design procedures for PDS layout and first-order circuit simulation. Software companies in the PCB/packages arena such as Sigrity and Ansoft, as well as IC companies like Magma and Apache, support a more analytical approach to PDS design for power integrity (PI) engineers, who commonly apply detailed numerical analysis tools. The EDA tools for PCBs leverage both circuit theory and numerical electromagnetic (EM) simulation to perform board-level characterization of an entire PDS.

Both static and dynamic power delivery analysis solutions are available for consideration of DC and high-frequency switching effects, respectively. Static power delivery analysis is important – it helps eliminate DC voltage drop across the PCB due to resistive loss in the copper power planes, which can consume valuable dynamic noise margins. Another role of static analysis is to assure via and plane current density constraints are met to avoid thermal issues, and to prevent vias from acting like fuses. Dynamic PDS analysis solutions provide power plane impedance values that can be applied to characterize decap placement strategies and component selection schemes. This approach enables PI experts to craft small board designs with a minimum number of intelligently selected and placed decaps. However, for practical PCBs, this manual tuning of decaps becomes a time-consuming process that is impractical for designs with more than a handful of decaps. The flow of board-level detailed numerical analysis is shown in **Figure 1a**.

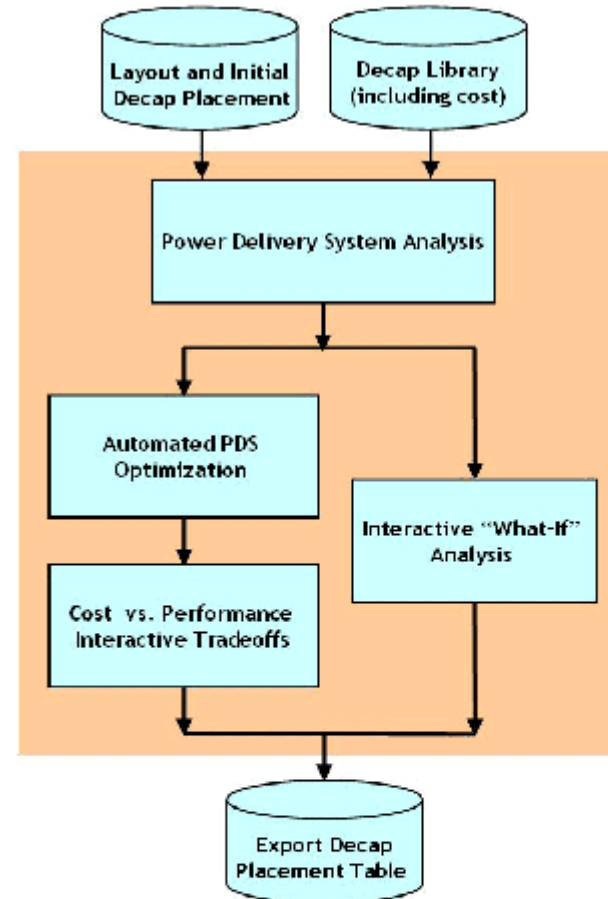


Even PI experts apply heuristic placement rules for larger PCB designs by applying more decaps than required to be certain their primary objective of assured PDS performance is reached. As time permits, PI engineers address low manufacturing cost through an iterative EDA-based virtual prototyping procedure. Experience and intuition drive the removal of decaps from the design; then, detailed numerical analysis of the PDS is performed to verify performance of the reduced-cost design. This can be a time-consuming process. Considering that most PI engineers have a single day for final design review turnaround time, many boards are delivered with unnecessarily robust – and expensive – PDS designs. Therefore, novel design practices are called for to help PCB designers and PI engineers overcome challenges and achieve cost-effective PDS designs with assured performance.

Novel PDS Design Practices

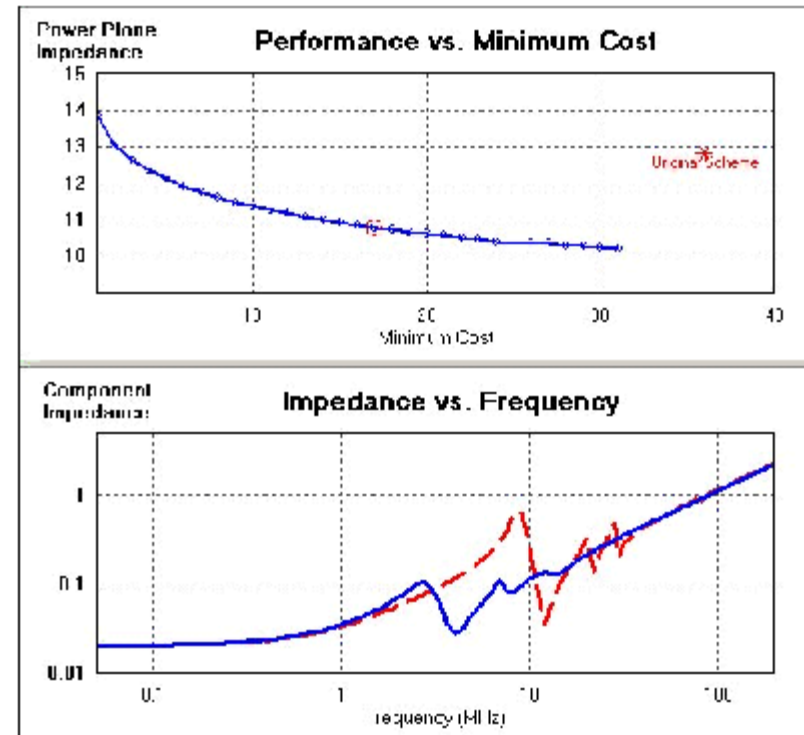
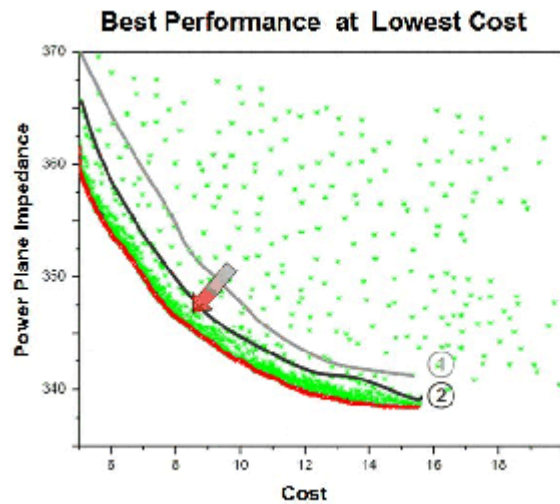
The fundamental requirement for such a novel PDS design solution is explicit, early consideration of manufacturing cost as a design-level objective. Cost also can be considered after product prototypes are completed, through validation of proper product operation as decaps are physically removed or replaced by lower-cost components. This process yields marginal cost reductions with a significant risk of product failure. This product failure risk mandates that another issue be addressed by a novel PDS design solution – the analytical assurance of PDS performance. This can be accomplished by applying the same underlying board-level simulation technology currently applied by PI experts. However, this analysis must be automated and available to average PCB designers, and the automation must apply to both small and large PCBs. A high level of PI expertise should not be required to successfully assure PDS performance and determine reasonable cost-efficient design alternatives. Therefore, an automated procedure is needed to consider a broad class of potential designs at varying levels of cost and performance. It can be viewed as an "optimization" procedure to complement the underlying "analysis."

Even with this high level of automation and ready access by average PCB designers, a novel PDS design solution must provide visual validation of system-level and component-level performance for design alternatives of varying cost. A PCB designer's quick examination of the optimization results provides analytical assurance of PDS performance, and enables rapid intuitive selection of the best design alternatives to meet high-level business needs. A final requirement for a novel PDS design solution is the ability to easily incorporate the final PDS design in the layout and schematic environment that created the original design database. **Figure 1b** summarizes a plausible flow for this novel PDS design solution.



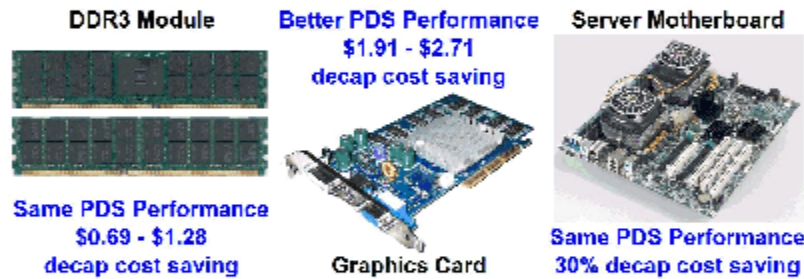
OptimizePI, a new PDS design solution from Sigrity, has implemented this new flow. This flow has been characterized for many PCB designs, including memory modules, graphics cards and computer boards. These products were optimized for both cost efficiency and assured PDS performance. The high-level requirement most often expressed for a PDS optimization procedure is that initial performance level must be maintained to consider a lower-cost design alternative. This PDS performance level can be judged both by power plane impedance and by power plane noise voltage, as seen by high-power components (DRAMs, ASICs, CPUs) looking into the PCB.

The automated PDS optimization procedure is driven by a composite power plane impedance, where lower impedance corresponds to higher system-level PDS performance. Many thousands of designs at various levels of cost and performance are considered. Only the best-performance design alternative at each cost is relevant to the PCB designer. To help visualize the optimization process, a green cross is plotted in Figure 2 to represent each design alternative considered. The convergence of the optimization process is observed as it progresses from state "1" to state "2" to the final results represented by the solid red trace. Figure 2 represents a best-performance versus lowest-cost set of design alternatives for the PDS design, information previously not available even to expert PI engineers using detailed analysis tools.

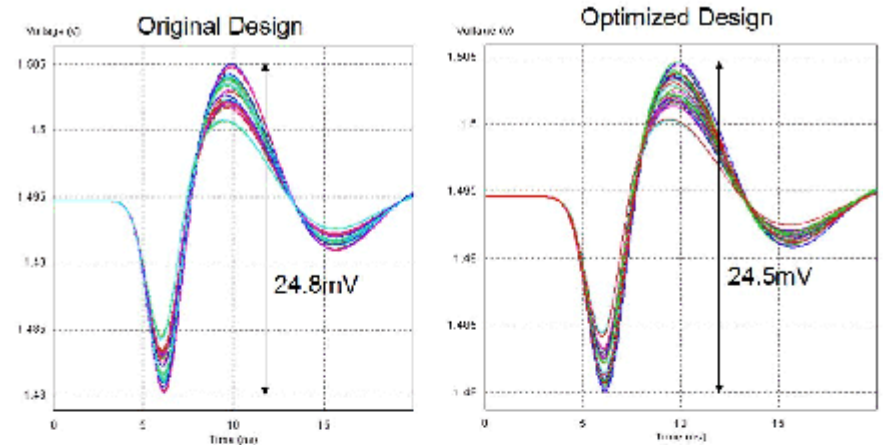


Cost versus performance tradeoffs must be made available for intuitive visualization at both system and component levels, as shown in Figure 3. The bottom component-level impedance plot provides a detailed view of PDS performance for the selected cost point on the top best-performance versus lowest-cost plot. It has been verified repeatedly that choosing a lower-cost PDS design alternative with the same component impedance level provides very similar PDS performance. This is true for both power plane impedance and power plane noise voltage.

Many PCB designs were examined to verify the benefits of applying this new PDS design procedure. It was repeatedly observed that PDS performance can be maintained at initial design levels while achieving significant cost reduction. Heuristic rules that constrain the PDS design of initial PCB layouts are not considered by the optimization procedure; therefore, novel decap configurations are considered, reducing or eliminating power plane resonances and significantly increasing PDS performance. Three PDS optimization examples and resulting improvements are cited in **Figure 4**.



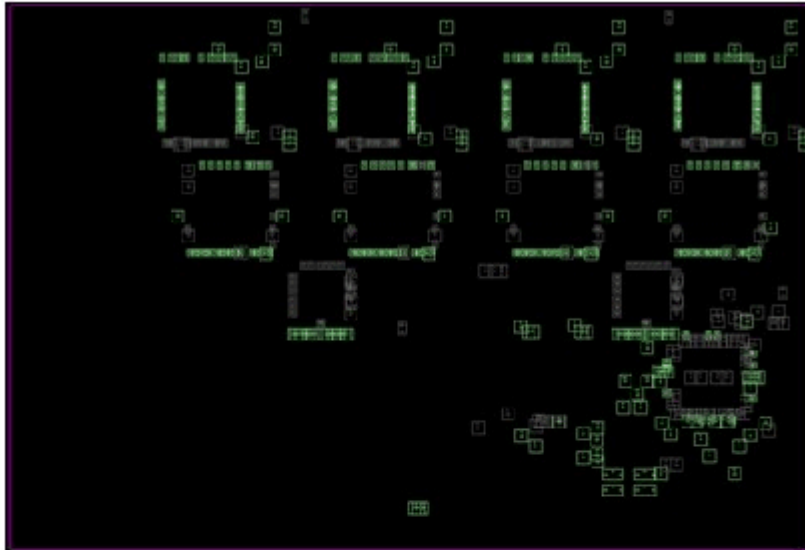
The DDR3 memory module optimization with 36 DRAMs resulted in \$0.69 savings per DIMM. A decap area reduction of 32% also was achieved while maintaining PDS impedance performance and marginally improved power plane noise performance (as shown in **Figure 5**). A high-speed graphics card was optimized for combined PCB-package PDS performance. A multi-domain package-board power plane resonance was reduced to yield significantly improved performance with nearly \$2 in manufacturing cost savings.



Despite careful initial PDS design, a dual-CPU high-performance server board with more than 1,000 decaps was optimized to maintain PDS performance at a constant level; this action resulted in a 30% PDS cost reduction. These examples are typical of high-volume boards to which the novel PDS design solution has been applied. At the volume levels of DDR3 memory modules, commercial graphics cards and computer server boards, these optimized designs represent substantial bottom-line cost savings and assured PDS performance.

A final example provides an intuitive view of PDS optimization results by examining the decap placement for a PCB layout. The PDS of a very large PCB – with eight FPGAs and three additional mounted components – was optimized. **Figure 6** shows the placement locations of the original PDS design (top) and the optimized PDS design (bottom). The original design had a PDS cost of \$24.65 and the final design a PDS cost of \$14.04, representing a 43% cost reduction. The optimized design was selected to have the same PDS performance as the original PCB layout.

Original PDS Decap Placements



These PDS optimizations were performed with access only to the initial PCB design database and specification of a small set of decaps from commercial vendors. Less than one hour of engineering time for design setup and optimization results post-processing was required. Typical engineering workstations perform small PCB optimization in an hour, and large designs (such as the eight-FPGA board) can require several hours of compute time.

Design complexity requires new ways to optimize PCB power delivery systems for maximum performance at minimum cost. This new PDS design solution has been implemented and characterized for many PCB designs, and has been proven to significantly reduce costs and improve performance for PDS designs. An average PCB designer with access only to the PCB design database and a library of decap components can, indeed, implement cost-effective and performance-assured PDS designs, with cost savings of 15 to 50%.

Brad Brim has product marketing responsibilities for Sigity in the area of package and PCB extraction. Brad previously worked for Ansoft in applications engineering and marketing roles. He has been involved with EM analysis tools and applications involving passive modeling for more than 20 years. Brad can be reached at bradb@sigity.com.



Optimized PDS Decap Placements