Modeling of the Electrical Performance of the Power and Ground Supply for a PC Microprocessor on a Card

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Abstract

The electrical characteristics of the power and ground supply of a PC microprocessor packaged in a Ball Grid Array (BGA) package mounted on a card are studied by dynamic electromagnetic field analysis. The effects of decoupling capacitors of different types and at different locations are investigated to achieve the objectives of low power and ground impedance and no or insignificant resonances inside the package.

Introduction

The objective in the design of a power and ground distribution system is to ensure the power and ground voltage fluctuations are within certain allowed margins. The electrical performance of a power and ground system can be characterized through its inductance, but a more effective way is through its impedance from DC to the upper frequency limit of the switching current spectrum. With the ever-increasing edge rates of CMOS devices, the assurance of power and ground fidelity has become a major challenge [1-2]. The impedance of a power and ground system typically increases with frequency, and can reach quite significant magnitudes if there are significant resonances inside the package. The faster the edge rates of devices, the wider the switching current spectrum, the more difficult it is to maintain low impedance of a power and ground supply system.

The power and ground distribution system considered here includes primarily the microprocessor chip carrier and a printed–circuit card, as shown in Figure 1. The major concern is to ensure the power fidelity for the core power supply of the microprocessor chip. Numerous design trade-offs can be made at various levels, including on-chip, on-package, on-card and on-board. The proper design of a power and ground distribution system includes issues such as the stack-up of power, ground, signal and dielectric layers, the placement of decoupling capacitors of right types at right locations, and the placement of vias connecting metal planes. Many of these design decisions first come from previous design experiences and from insights on what physically happens inside packages, followed by what-if analyses and optimizations through software simulations, and by verifications through hardware measurements.

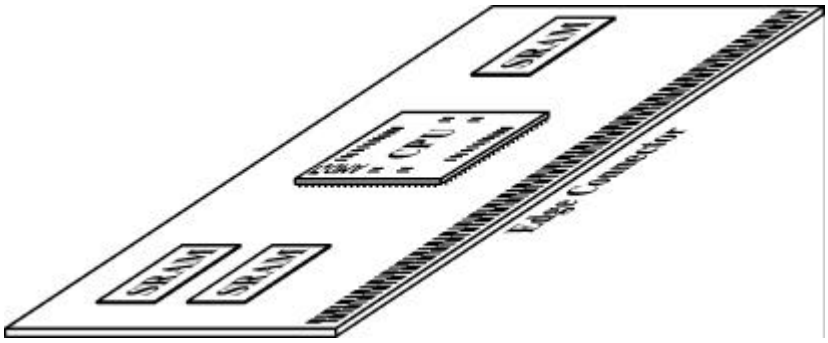

Figure 1. A microprocessor chip in a BGA package mounted on a printed-circuit card.

Simulation Methodology

Simulation of the electrical performance of power and ground distribution systems, especially at high frequencies, necessitates sophisticated electromagnetic (EM) field analysis. The EM field analysis should take into account effects of wave propagation, coupling between different components, as well as reflections from edges of metal planes that cause resonance inside packages. Unlike the analysis of signal distribution systems, where one or a few signal nets can be simulated separately, accurate analysis of the power and ground distribution systems often requires the inclusion of all the power and ground planes, a large number of vias and traces, and all the decoupling capacitors.

One simulation approach used before is to represent power and ground planes by a two-dimensional mesh of transmission lines or distributed RLC elements, and to simulate the circuit representation of the package using SPICE [1, 3]. As the number of components is increased, especially closely spaced vias, finer meshes have to be used, and simulation times increase dramatically. For the structure considered in Figure 1, due to the large number of via, trace and plane components involved, it is not practical to run SPICE simulation of the circuit representation of the entire package structure.

The simulation methodology used for this study is outlined in [4-5]. The software tool in which the methodology is implemented is SPEED97 [6]. With this approach, fields inside the chip carrier and the card are decomposed into the parallel-plate mode and the strip-line mode fields. The parallel-plate mode of fields are solved by the numerical solution of the corresponding partial differential equations, and the strip-line and microstrip line mode of fields are computed by transmission line analysis. The EM field simulation is run simultaneously with circuit simulation, and the interactions between the two modes of fields and between the package and circuit components (including drivers, terminations, and decoupling capacitors) are automatically taking into account. Due to the fast EM field computation of the software tool, the dynamic EM field analysis can be performed in a reasonable time for the entire chip carrier together with the printed-circuit card and all the decoupling capacitors mounted on the chip carrier and the card.

The frequency-dependent impedance of a power and ground distribution system is obtained by connecting a source circuit across the power and ground pads from which the impedance is to be measured. The source circuit usually contains a voltage or a current source with a source impedance. The time-domain waveform of the source is often chosen as a Gaussian pulse such that its spectrum contains the highest frequency of interest. During the time-domain simulation, the voltage across the output terminals of the source circuit and the current flowing into the power and ground supply system are recorded. Then the ratio of the Fourier transforms of the voltage and the current gives the impedance of the power and ground distribution system as a function of frequency.

Sample Results

Results displayed in Figure 2 are impedances of one candidate of printed circuit card for the microprocessor, under different test conditions. The impedance displayed in Figure 2 refers to the impedance, in the core area of the chip, between all the core power pads and all the core ground pads on the mounting

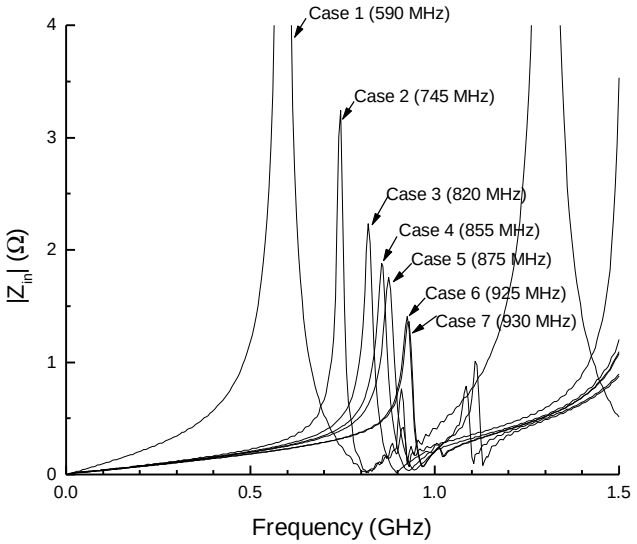

Figure 2. Impedances of the power and ground supply of the card for progressively more capacitors on the card.

surface of the card. The power and ground supply of the board, connected to the card through an edge connector, is modeled by a short-circuit or a low value impedance. Case 1 corresponds to no decoupling capacitors on the card, and it shows that the card under test has a resonant frequency at about 590 MHz. Cases 2 to 7 have progressively more decoupling capacitors (including small, medium and bulk capacitors) placed in the core area of the chip as well as at other places. It has been found that, through proper placement of decoupling capacitors, the resonance inside the card can become less significant, and the first resonant frequency can be increased to near 1GHz.

Each resonant frequency corresponds to an electromagnetic resonant mode inside the card. The software tool allows us to visualize the dynamic voltage wave propagation inside the card. The animation of the dynamic wave propagation helps us gain insights on what is happening in the card, identify resonances and select proper locations for the capacitors.

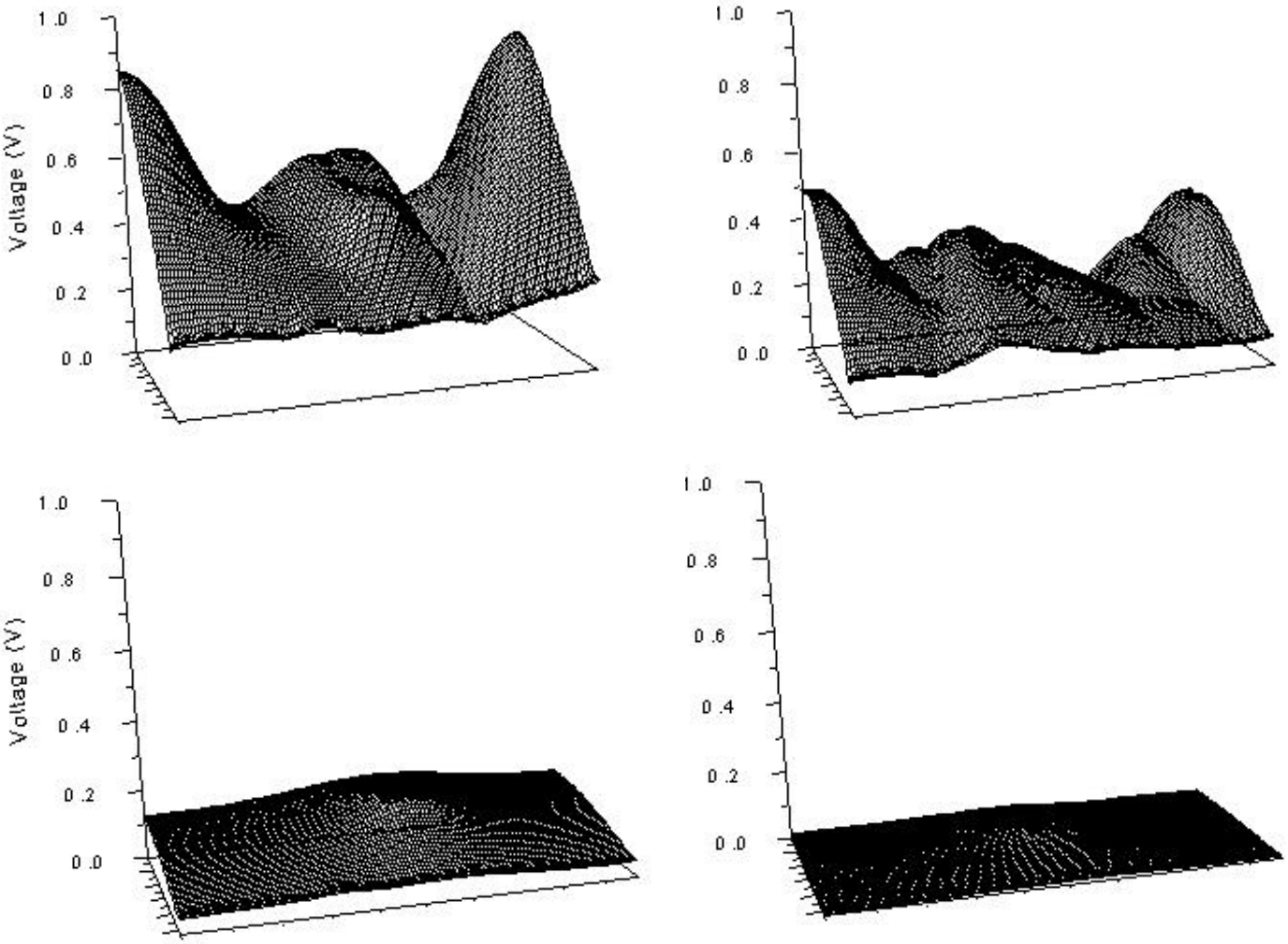

Figure 3. Peak spatial voltage distribution between power and ground plane. (a) Pulse width of 700 ps and no capacitors on the card; (b) Pulse width of 700 ps and with capacitors on the card; (c) Pulse width of 3.5 ns and no capacitors on the card; (d) Pulse width of 3.5 ns and with capacitors on the card.

Figure 3 shows the peak spatial noise voltage distribution between the power core metal plane and its adjacent ground plane. Figure 3 (a) and (b) are for a source waveform of a Gaussian pulse of 700 ps, while Figure 3 (c) and (d) are for a Gaussian pulse of 3.5 ns. The peak noise voltage value displayed is the maximum noise voltage value at that location during the whole simulation time. From these figures, we can assess the effects of decoupling capacitors at different locations and for transient currents having different frequency spectra.

Further Work

It is an on-going effort of seeking better and more cost-effective packaging structures for microprocessors of increasingly higher speeds. We are continuously exploring options of different layer stack-ups and lumped versus integral capacitors for reducing the power and ground supply noise, minimizing the coupling between signal nets and between power and signal distribution systems, and preventing electromagnetic resonance and radiation.

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Reference

[1] H. Hashemi and D. Herrell, "Power Distribution Fidelity of Wirebond Compared to Flip Chip Devices in Grid Array Packages," IEEE Trans. Comp., Packag., Manufact. Technol., Part B: vol. 20, Aug. 1997, pp. 272-278.

[2] L. D. Smith, "Packaging and Power Distribution Design Considerations for a Sun Microsystems Desktop Workstation," *IEEE 6nd Topical Meeting on Electrical Performance of Electronic Packaging, Conference Proceedings*, pp. 19-22, Oct.27-29, 1997, San Jose, CA.

[3] K. Lee and A. Barber, "Modeling of Analysis of Multichip Module Power Supply Planes," IEEE Trans. Comp., Packag., Manufact. Technol., Part B: vol. 18, Nov. 1995, pp. 628-639.

[4] Y. Chen, Z. Chen, Z. Wu, D. Xue and J. Fang, "A New Approach to Signal Integrity Analysis of High-Speed Packaging," *Proceedings of IEEE Fourth Topical Meeting on Electrical Performance of Electronic Packaging,* Portland, Oregon, Oct. 2-4, 1995, pp. 235-238.

[5] J. Fang, Z. Chen, Y. Chen, D. Xue and J. Zhao, "Integrated Electromagnetic and Circuit Simulation for Signal Integrity Analysis of High-Speed Electronic Packages," Proceedings of 1997 Government Microcircuit Applications Conference, pp. 347-350, March 10-13, 1997, Las Vegas, Nevada.

[6] www.sigrity.com.