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Model Extraction and Circuit Simulation Approaches For Successful SSO Analysis

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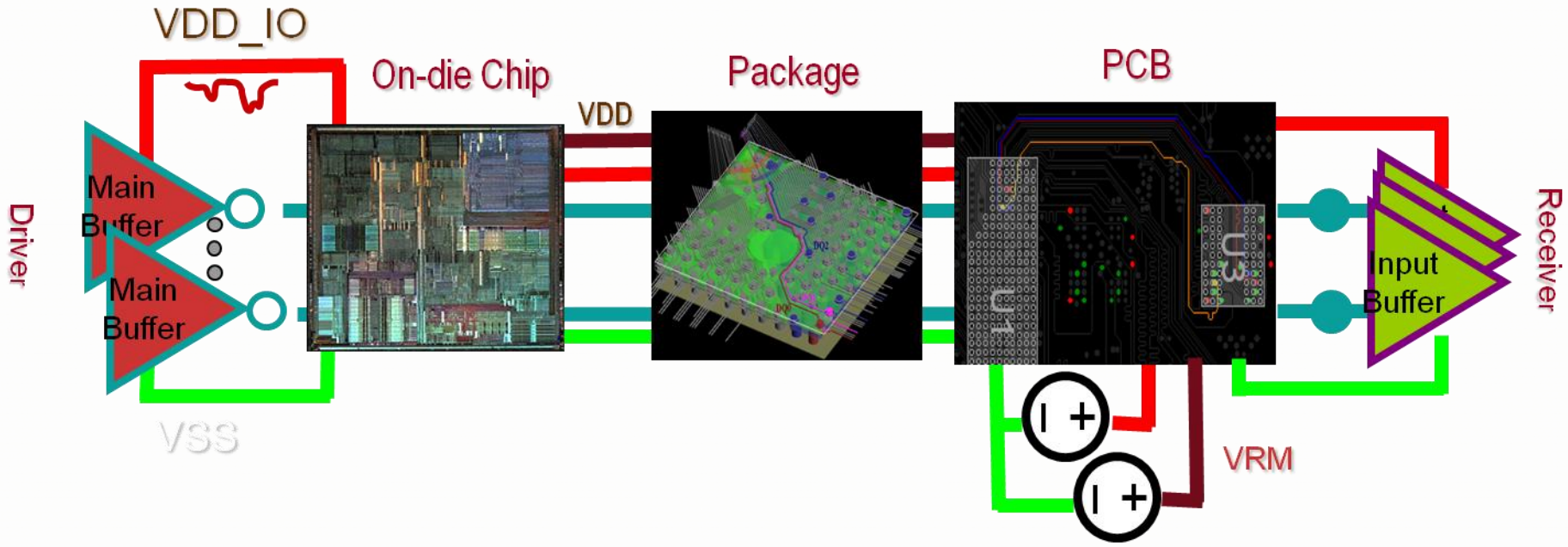
Simultaneous Switching Output

- For large parallel buses SSO can become a significant effect
  - root cause is often the PDN rather than proximity coupling amongst signals
  - PDN noise is signal noise
  - even if PDN noise is small, PDN-enhanced coupling amongst vias causes high signal coupling
  - even in the absence of noise levels high enough to cause unintended switching, timing/jitter is affected

System-level Modeling

- Must decide and verify how much of the system must be modeled from the accuracy of results desired



Bandwidth Considerations

- High frequency bandwidth
  - Tr = 100pS
  - 0.35/Tr = 3.5GHz
  - F_max = 6GHz
- Low frequency domain
  - R(freq) should be small
    - T_max = maximum metal thickness = 37um
    - frequency below when T_max is one skin depth (500MHz)
    - F_low = 100kHz

Extraction Issues

- Accuracy
  - general numerical noise
  - e.g. passivity
- Causality
  - e.g. material properties
- Numerical stability unique to **low frequencies**
  - AC solvers are generally illconditioned as $1/\omega^2$
- Consistency of AC results with DC results
- “DC extrapolation”

Circuit Simulation Issues

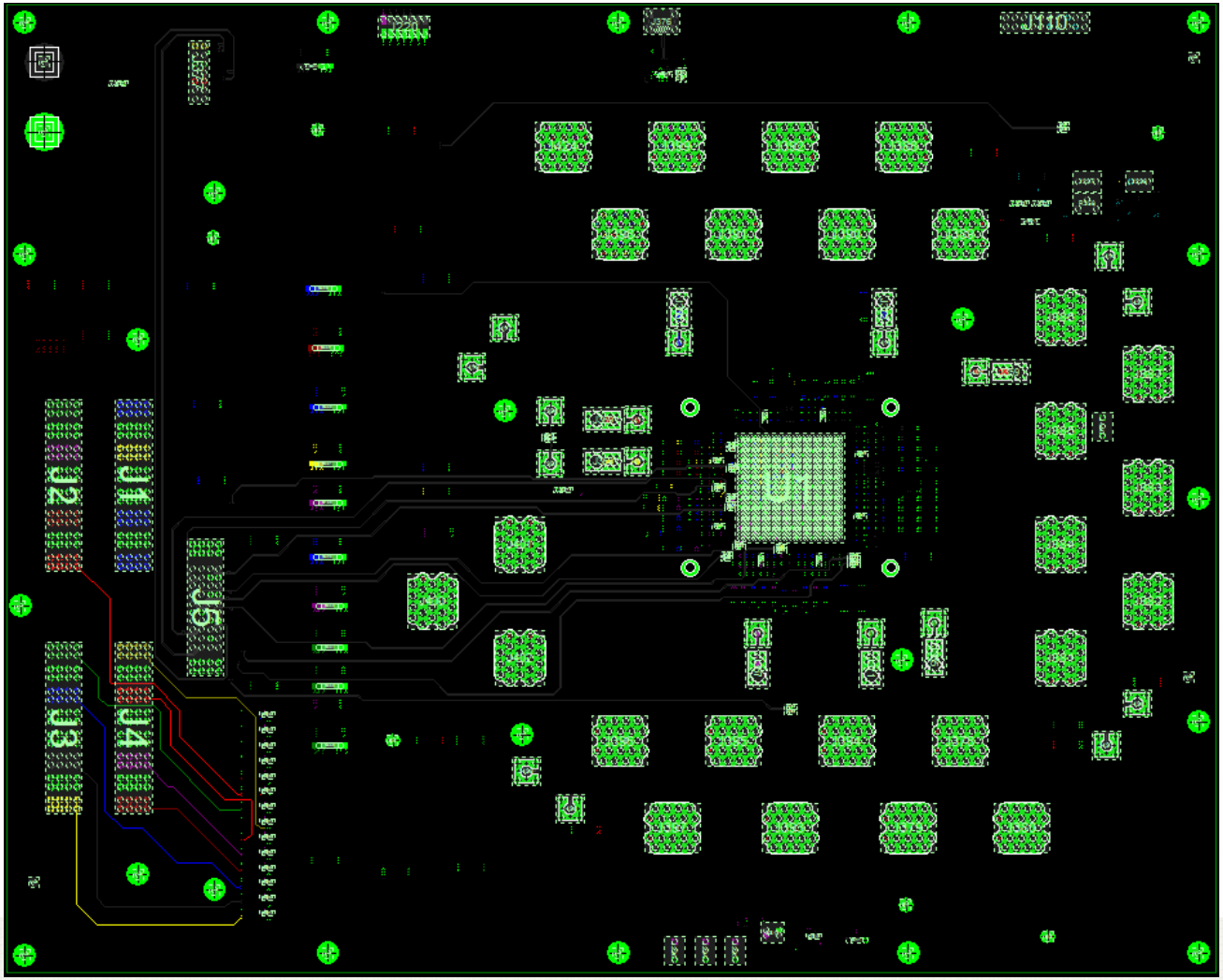
- Data formats supported
  - Touchstone, BNP
- Buffer element support
  - transistor level models
  - Power-aware IBIS models
- Frequency domain data elements available
  - controlled sources
  - direct usage
  - rational function fit (internal or external)
- Simulation control parameters

How to Assure Success ?

- One person is responsible for the netlist
- Many people contribute models
  - different expertise and language
  - different departments (companies)
  - different extraction tools
- Is there a way to assure success for SSO analysis?
  - too many heuristics
  - too many inconsistent failures
  - a cookbook flow or best-known-method is needed

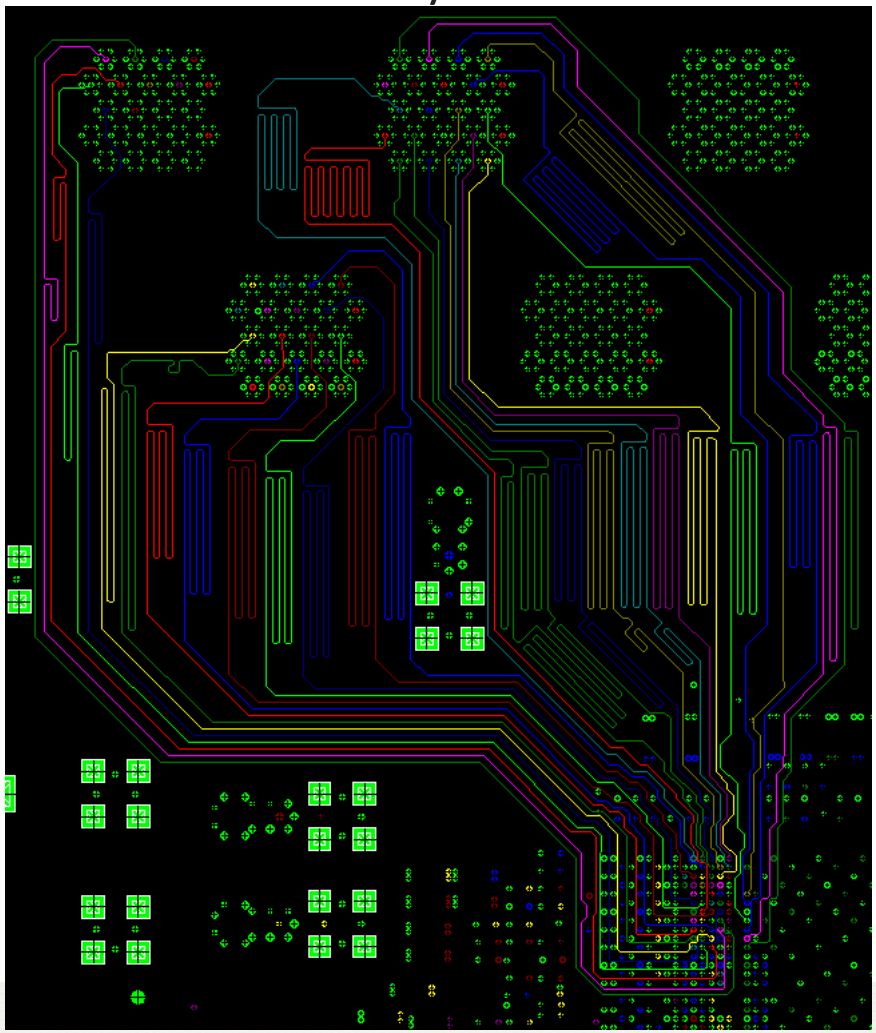
A Test Case

- Xilinx verification board

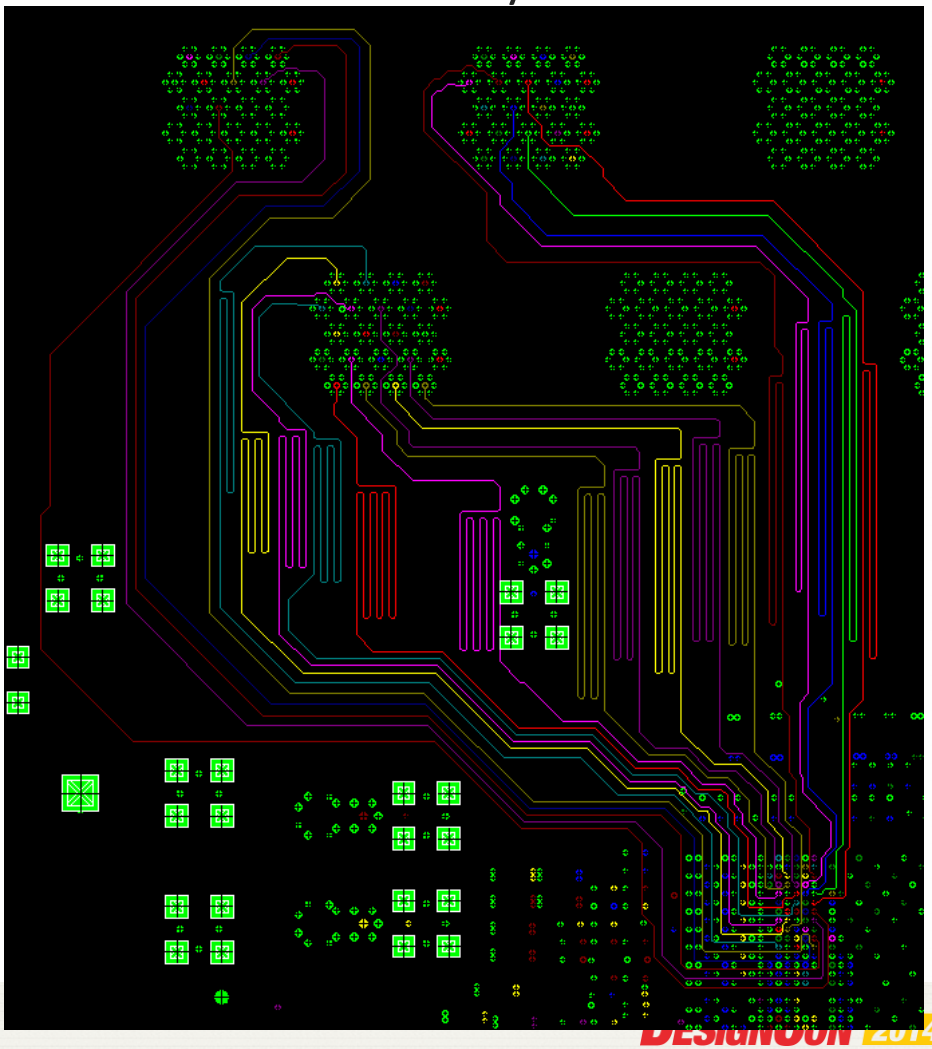


Routing

Layer 3



Layer 5

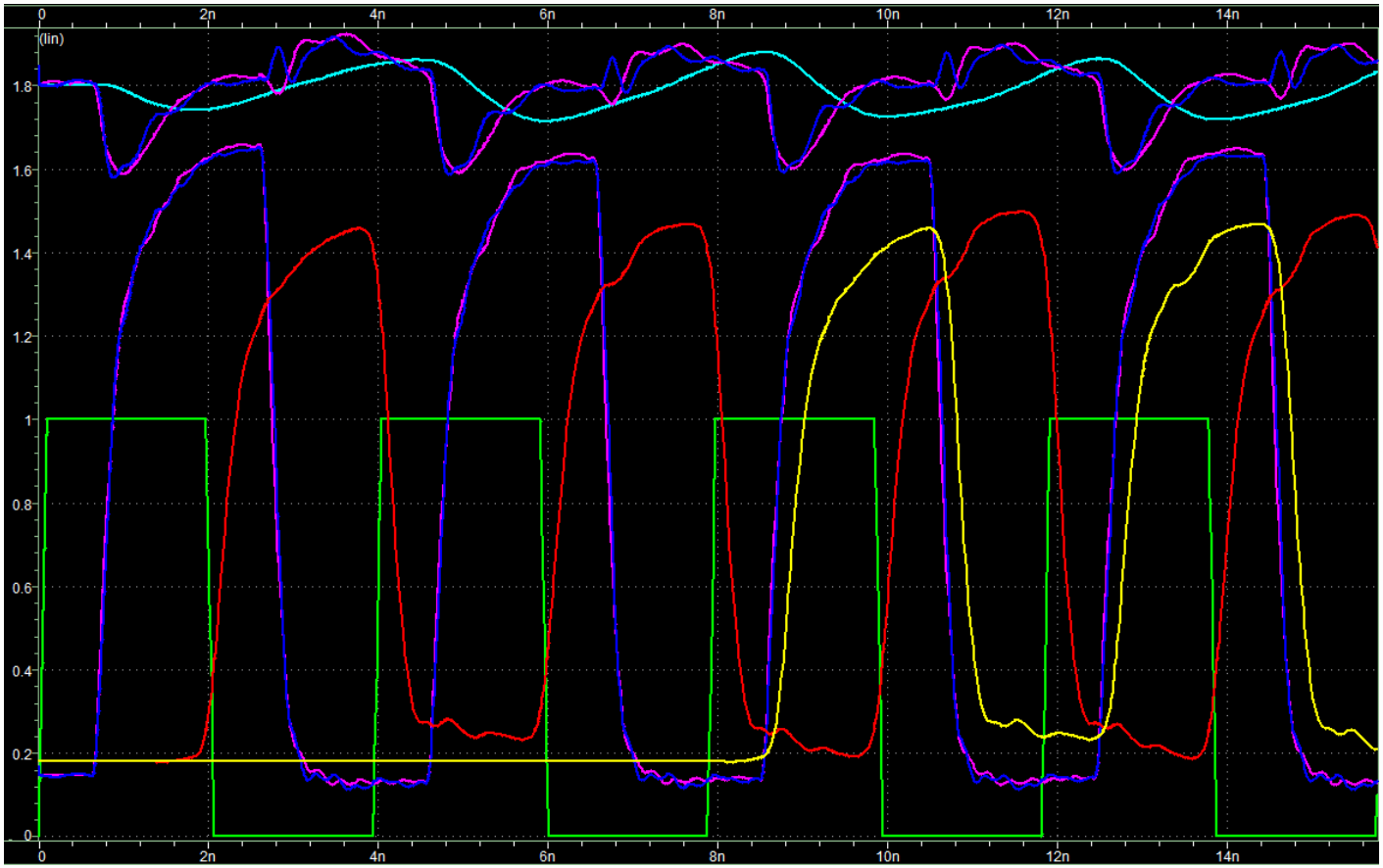


The System-level Model

- Power-aware IBIS drivers
- Simple RC on-die PDN model
- Known-good FD model for package
- Variable PCB model
- Simple cable and termination models
- Relevant package and PCB decaps
- 50 single-ended channels
- All other signal nets excluded from extraction
- All power domains included in extraction

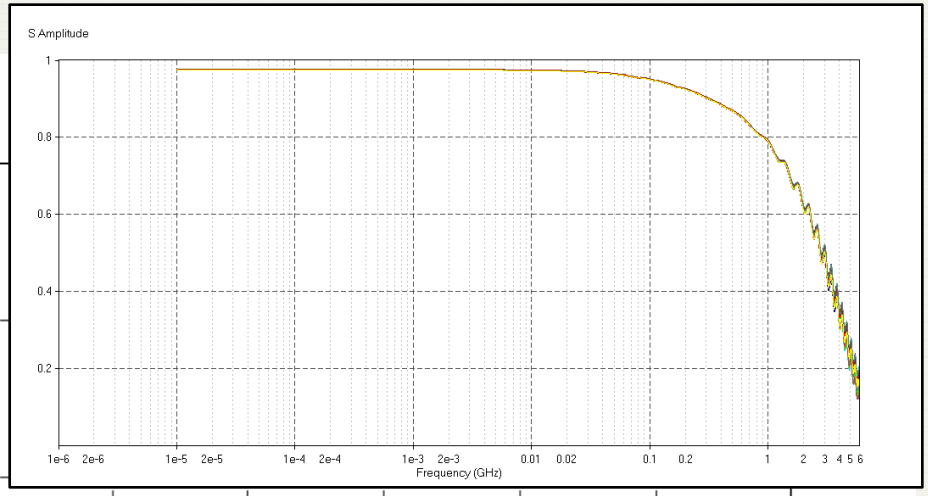
Transient Response

- Signal and power waveforms



VRM
Chip (binary)
Chip/Package
Package/PCB
PCB/Cable
Termination

PCB Channel Insertion Loss – S(i+1,i)



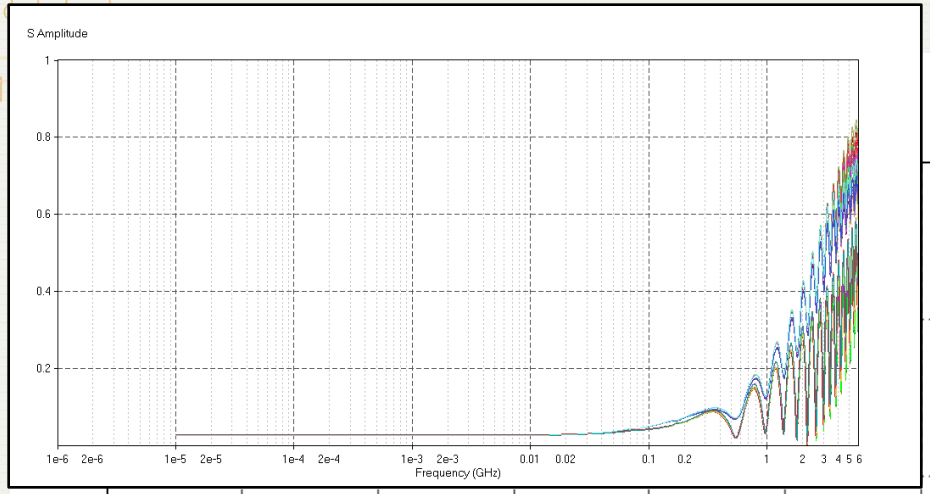
S Amplitude

1
0.8
0.6
0.4
0.2

500 1000 1500 2000 2500 3000 3500 4000 4500 5000 5500 6000

Frequency (MHz)

PCB Channel Return Loss – S(i,i)



Envisioned Approach

- Investigate extraction options
  - discrete vs. continuous data
  - lowest frequency of extraction
  - explicit DC data
  - postprocessing of data
    - precision versus passivity-assured macromodel
- Investigate circuit simulation options
  - direct vs. rational function application of frequenecy domain data
  - simulator options

Extraction Options

- Discrete data
  - fix high frequency sampling: linear and log
  - vary low frequency sampling: linear and log
  - vary lowest extraction frequency: 1KHz – 1MHz
  - consider explicit DC data: separate DC extractor
- Continuous data
  - vary lowest extraction frequency
  - consider explicit DC data
- Processed data
  - generate rational function model
  - consider passivity/causality

Circuit Simulation Options

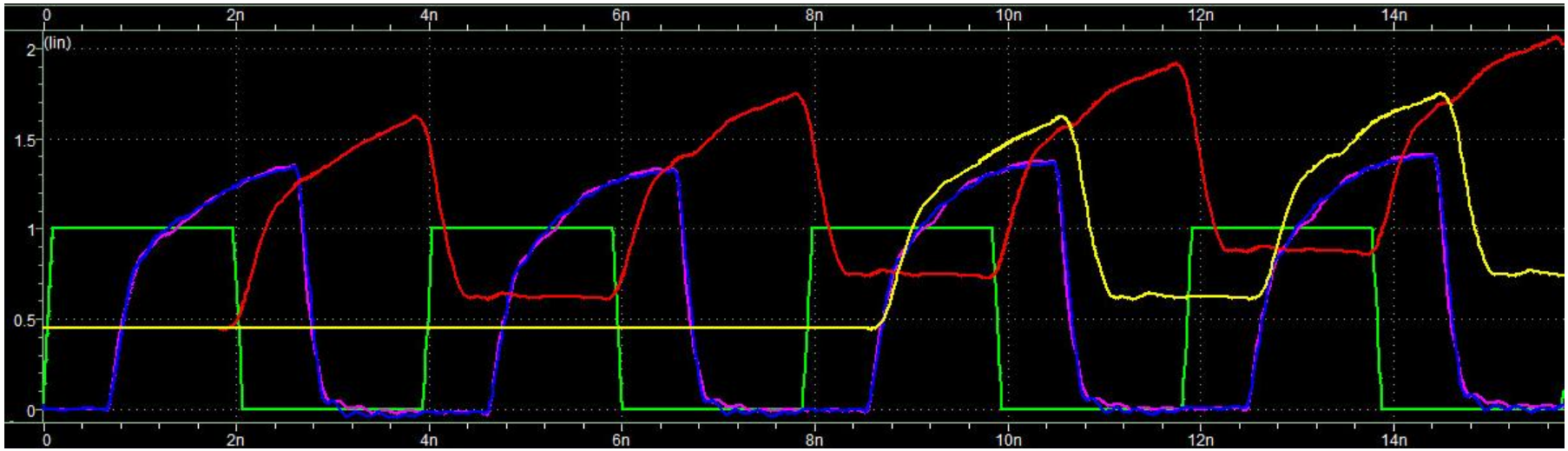
- Data formats supported
  - Selected Touchstone (discrete) and BNP (continuous)
- Buffer element support
  - Selected power-aware IBIS models
- Frequency domain data elements available
  - Tested direct usage and controlled sources
  - Focused on rational function fit (internal and external)
    - best general performance and success
- Simulation control parameters
  - Not explores in detail and not discussed here

Typical Failure Modes

- Rational function generation fails
  - hangs or takes forever
- Passivity/Causality fails to complete
  - iterative so it gets better
- Circuit simulation convergence issues
  - hangs or takes forever
  - illogical results
  - Ever-increasing DC offset

Typical Incorrect Waveform

- When DC extrapolation fails an ever increasing DC offset is observed



Observations

- Discrete data
  - fix high frequency sampling
    - considered linear and log
    - not much affect unless too sparsely sampled at F_max
  - vary low frequency sampling
    - considered linear and log
    - no observable systematic differences
    - indeterminate failures
  - vary lowest extraction frequency
    - considered 1KHz to 1MHz
    - highest end had more frequency failures
    - indeterminate failures

Observations

- Discrete data (continued)
  - consider explicit DC data: separate DC extractor
    - issues when difference between DC and AC extrapolated is larger
    - issues more common when the difference is larger
    - helps to "***adjust***" AC data to correspond to DC value
    - success sensitive to adjustment algorithm
- Continuous data
  - vary lowest extraction frequency
    - generally more frequent success relative to discrete data
    - same indeterminate failures observed
  - consider explicit DC data
    - same observations as for discrete

Observations

- Processed data
  - generate rational function model
    - performed externally to circuit simulator
    - doesn't affect previous observations significantly
  - consider passivity/causality preservation
    - performed after initial rational function generated
    - can be more time consuming that rational function generation
    - may require user interaction in some cases for successful passivity/causality preservation
    - seems to assure successful simulation
    - can results in a bit slower circuit simulation time relative to applying some of the other options … the price of success

Discussion

- Selected 1kHz lowest extraction frequency
  - highly dependent on the extraction tool, verify numerical stability
- Selected rational function model in circuit simulator
  - fastest, most reliable yet controlled source model is a backup
- Failures are indeterminate
  - failures at lower F_min when higher F_min succeeded
  - failures with more dense discrete sampling when lower density sampling succeeded
- Insensitive to LF data when circuit simulation succeeded
  - Extrapolated DC value not critical … if not illogical
- Must assure passivity/causality to assure success
  - may sacrifice efficiency, since success is possible without it

Best Known Method

To assure successful system-level SSO analysis …

- Apply an adaptively sampled frequency sweep in the extraction tool for continuous data. (preference)
- Minimum frequency should be specified below the lowest frequency at which frequency dependent resistance occurs.
- Minimum frequency should be specified high enough to avoid numerical noise in the extraction tool being applied.
- Do not apply explicit DC data that is inconsistent with the AC data.
- Generate a rational function model with assured passivity and causality.
- Apply this rational function directly in the TD circuit simulator.