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Measurement and Simulation of Simultaneous Switching Noise in the Multi-Reference Plane Package

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Abstract

A simplified laboratory experiment representing simultaneously switching circuits in a multi-reference plane package is described. Experimental data is compared to theoretical calculations and to simulated data from three modeling techniques of progressive complexity, including lumped element, hybrid lumped element / transmission line, and full wave solutions. The merits and limitations of each technique are presented.

I. Introduction

When digital integrated circuit (IC) chips are placed on a single-chip module (SCM), a multi-chip module (MCM) or a printed wiring board (PWB), the off-chip driver (OCD) circuits on one chip are connected to the receiver circuits on the other chips with interconnecting signal lines. High density IC chips with hundreds of signal I/O may require a SCM/MCM/PWB with many signal and reference/power layers. Often the signal lines on different wiring layers are connected by the via conductors formed by the plated-through-holes (PTH). When the output state of an off-chip driver circuit changes, the current on the interconnecting signal line, the via and the return path on the reference planes may cause transient voltage variation between the reference planes. This transient voltage can cause noise on quiet signal lines connected by vias at some distance from the active via. When there are many vias carrying active signals, the noise picked up by a quiet via in the package may become unacceptable.

This paper will describe recent experimental results designed to represent the noise generated by simultaneously switching circuits in a two-reference plane package or PWB. A simplified experiment was intentionally designed to highlight the challenges facing the system and package designers as circuit rise times become significantly shorter relative to the IC chip and package time of flight. Accurately modeling and simulating the significant time delays in the signal and power distribution networks as well as the discontinuities in the return current path introduced by the PTH present significant challenges.

The physics related to the generation of simultaneous switching noise in the multi-reference plane package are also described. A theoretically derived full wave solution is presented and applied to the laboratory experiment Calculated results compare favorably with experimental data for the cases within the limitations of derived equations. Three additional modeling techniques are then described and applied to the laboratory experiment.

A lumped element approach to modeling the experimental results is compared to a hybrid transmission line / lumped element technique. These are further compared with a numerical full wave technique. The lumped element technique has been shown to be accurate when the package dimension is small relative to the wavelength associated with the active signal rise time. As package dimension size increases and rise time decreases, it becomes necessary to model the transmission line or full wave behavior of signal and power distribution networks. This is evident as one observes the comparisons below. As model complexity increases from the lumped element to the full wave solution, correlation to experimental data improves dramatically both in noise amplitude and wave shape.

II. Laboratory Experiment

A simple experiment was designed to demonstrate the generation of noise as simultaneously switching circuits drive lines interconnected by vias in a two-reference plane structure. The experiment was also designed as a vehicle for verification of various techniques of modeling and simulating this noise.

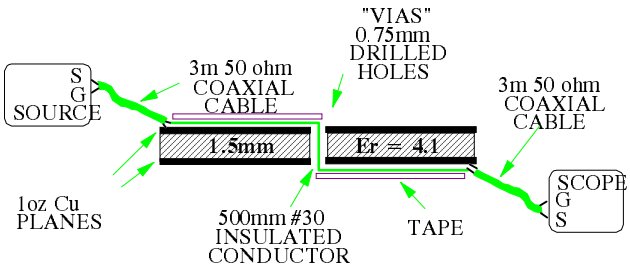


Figure 1. Cross-sectional View of Test Structure

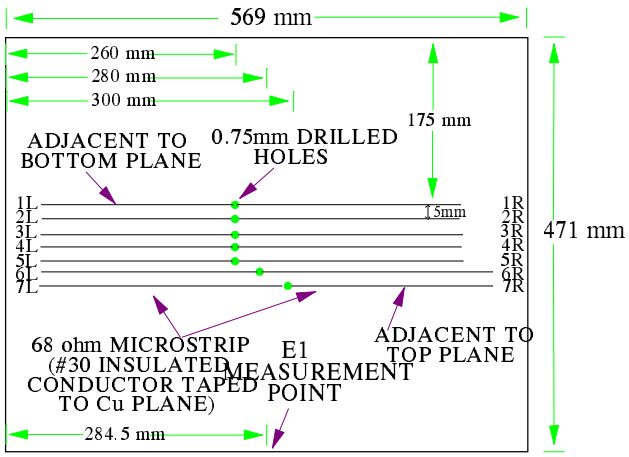


Figure 2. Top View of Test Strucure

A test structure was selected to serve as a large scale model of a structure common to many single- and multiple-chip modules and printed wiring boards. The structure is a 2S2P (two-signal/two-power) cross-section. A large (569x471mm) double-sided copper-clad board 1.5mm thick was obtained with 8212 glass/resin dielectric between the 1oz (0.035mm) planes of copper. Holes were drilled (0.75mm diameter) at 5mm intervals through the board near the center. Figure 1 shows a cross-sectional view while Figure 2 gives a top view of the test structure.

Signal lines were constructed by taping #30 insulated wires to the top and bottom surface of the board and running them through the drilled holes to simulate plated-through vias. The signal lines were later measured to have a characteristic impedance of between 65 and 70 ohms. Coaxial cables (50 ohms, 3M long) were then soldered to the ends of the #30

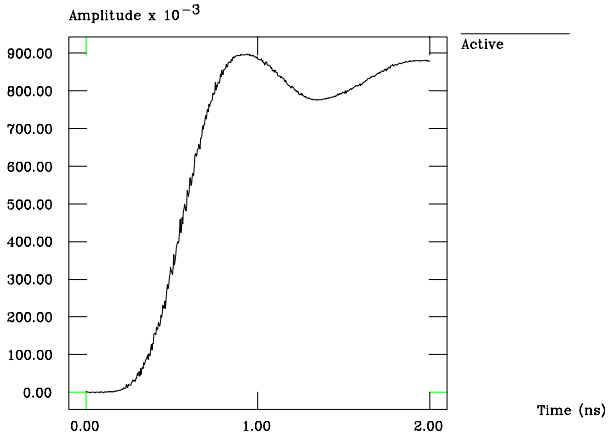


Figure 3. Active Signal Measured at Far End

wires with the ground of the cable soldered directly to the adjacent copper plane of the board. The ends of the coaxial cables were left open circuited except when the line was

	Measured	Theoretical	Lumped	Hybrid	Full Wave
Case I					
3R	11mV	n/a	9mV	16mV	13mV
7R	4.9	n/a	7	17	5.4
Case II					
3R	44	64	34	40	45
7R	23	25	27	41	22
E1	37	46	*	33	43
Case III					
3R	-1.4	n/a	-1.2	8.9	-0.2
7R	-2.7	-2.6	-4.3	12.5	-2
E1	-5.9	-7.8	*	8	-7.7

* no significant high frequency response was observed.

Table A. Comparison of Noise Pulse Amplitudes

being driven or noise was being measured with an oscilloscope.

The dimensional features of the board, drilled holes, coaxial cables and signal lines were selected for the following reasons. First, a high frequency response void of reflections was desired. This included reflections from the edges of the board as well as reflections from impedance mismatches at the generator/coaxial cable and coaxial cable/signal line interfaces. These reflections were pushed out beyond the time frame of study with large board, cable and signal line dimensions relative to the generator's risetime. Additionally, crosstalk between signal lines was minimized by spacing the lines at 10mm intervals. This was accomplished by alternatively running lines adjacent to the top and bottom copper planes to mesh with the 5mm drilled hole interval.

A pulse generator was then connected to the coaxial cable(s) at either the left or right side of the board depending on the measurement case. It was possible with this configuration to drive current through the "vias" with equal or opposite polarity, thereby causing the noises generated at each via to either add together or effectively cancel. The pulse generator was configured to deliver a 0.9V signal with a 0.5ns risetime (10-90%) as measured at the far-end of the coaxial cable/signal line/coaxial cable conductor. The pulse width of the generator was set to several hundred nanoseconds so the response to a single risetime could be observed.

Noise was measured at several locations including the near-end and far-end of quiet via/lines and at the edge of the board between the two copper reference planes. A sampling oscilloscope with a high-impedance probe was used and measurements were always made across a 50 ohm terminator. This terminator was only in place for a measurement, otherwise the board edges and coaxial cable ends were left open-circuited. A two-nanosecond time window was selected to focus on the high-frequency, incident response.

Several tests were conducted. In Case I, only line 2L was driven and noise was measured at the left and right ends of quiet lines 3 and 7, or 3L, 3R, 7L and 7R respectively. In Case II, four lines were driven to generate additive noise, lines 1R, 2L, 4L and 5R, and an additional measurement point at the edge of the board across the top and bottom reference planes was added. Case III was conducted with four lines driven, 1R, 2L, 4R, and 5L to observe the noise cancellation effect.

Results have been tabulated by amplitude and compared to theoretical and simulated results described in Table A. Figure 3 shows the experimental active signal as measured at the far end of the active line across the terminating resistance.

II. Theoretical Background Using Radial Transmission Line Theory

Consider a driving current entering the signal line at t=0, at 2L on the left-hand side of the experimental set-up shown in Figures 1 & 2. A return current will be induced on the top side of the top reference plane, underneath the signal line, flowing in the opposite direction, i.e. to the left. When the driving current reaches the via at t=1.5 ns, it will follow the signal conductor, thus making a 90 degree turn and flow downward in the negative z-direction. At the end of the via, the current will make another 90 degree turn, and flow to the right to point 2R at t=3 ns. From t=1.5 to 3.0 ns, there will be an induced current, flowing to the left, on the bottom surface of the bottom reference plane, right above the signal conductor. When this induced return current reaches the via, it is not connected to the top surface of the top reference plane. Instead, this current will continue to the top side of the bottom reference plane, and flowing out in concentric wave on the top side of the bottom reference plane. Of course, there will be induced current on the bottom side of the top reference plane, flowing inward to the via location, where it continue to the top side of the top reference plane. This current on the top side will be confined underneath the signal line and flow to the left. Eventually, it will reach the driving source at location 2L, thus completing a closed loop of current path.

The concentric wave, formed by the outward flowing current on the top side of the bottom reference plane, and the inward flowing current on the bottom side of the top reference plane, is the wave in the well known radial transmission line [1] provided the separation between these two surfaces, h, is much less than the wavelength at all frequencies of interest. We shall use a cylindrical coordinate, with r=0 at the center of the via conductor. The top surface of the bottom reference conductor is at z=0, with current flowing in the +r-direction. The bottom surface of the top reference conductor is at z=h, with current flowing in the negative r-direction. In using the radial transmission line theory, the electric field has only the z-component, E_z, and the magnetic field has only the ϕ-component, $H\phi$. And E_z and $H\phi$ are independent of the z- and ϕ-coordinate. The wave equation in the cylindrical coordinate is, [1]

$$\partial^2 EZ/\partial r^2 + (1/r)\partial EZ/\partial r + k^2 EZ = 0 \quad (1)$$

where $k = 2\pi f(\mu\varepsilon)^{0.5} = 2\pi f\tau = 2\pi/(\text{wavelength})$, which is a real value.

Note that the wave equation is the zero-order Bessel equation. We shall assume that the size of the board with two reference planes shown in Figure 2 is very large so that we have only the positively traveling wave. The electric and

magnetic fields may be expressed in Bessel functions as follows: [1]

$E_{Z(kr)} = B[J0(kr) - jN0(kr)]$ (2)

$H\phi(kr) = (1/j2\pi f\mu)\partial EZ/\partial r = (k/j2\pi f\mu)B[J0'(kr) - jN0'(kr)]$

$= (\varepsilon/\mu)^{0.5} B[N1(kr) + jJ1(kr)]$ (3)

When $kr < 0.2$, i.e. $(kr/2)^2 < 0.01$, we may neglect the higher-order terms in the power series expansion of the Bessel functions. Therefore, we have,

$EZ(kr)\ B\{1 - j (2/\pi)[0.5772 + \ln(kr/2)]\}$ (4)

$H\phi(kr) \quad -(\varepsilon/\mu)^{0.5} B (2/\pi kr)$ (5)

Note that $kr = 2\pi f\tau r$. If we want to take care of all frequency spectrum up to 3 GHz, $kr < 0.2$ is assured when $\tau r < 0.0106$ ns, or $r < 1.59$ mm (assuming $\tau = 6.67$ ps/mm). For the via conductor in the board used as shown in Figure 1, the above condition is satisfied. Therefore, we have,

$IVIA = 2\pi a\ H\phi(ka) \quad -(\varepsilon/\mu)^{0.5} B (4/k)$ (6)

$B = - IVIA (k/4)(\mu/\varepsilon)^{0.5} = - IVIA (2\pi f\mu/4)$ (7)

Hence, we have the solution for the positively traveling wave as follows:

$EZ(kr) = B[J0(kr) - jN0(kr)] = - IVIA (2\pi f\mu/4) [J0(kr) - jN0(kr)]$ (8)

$H\phi(kr) = - IVIA (k/4) [N1(kr) + jJ1(kr)]$ (9)

The asymptotic form for the Hankel function of the second kind is, [1]

$J0(kr) - jN0(kr) \quad (2/\pi kr)^{0.5} \exp[-j(kr - \pi/4)]$ (10)

To put a bound on the applicability of the above asymptotic form, we shall set $kr = 2\pi f\tau r > 0.5$ and a frequency spectrum of 100 MHz or higher. This requires a time-of-flight, $\tau r > 0.8$ ns. If we are allowed to neglect the frequency spectrum below 300 MHz, we may apply the above approximation for $\tau r > 0.267$ ns. The error in using the asymptotic form will increase at smaller distance from the via or for the lower frequency spectrum, when the value of kr decreases. For example, the asymptotic form gives a magnitude higher than the exact value by 8.7%, 11.1%, 14.9%, 21.7%, and 37.9% at $kr = 0.5$, 0.4, 0.3, 0.2, and 0.1, respectively.

Note that $k \quad 2\pi f\tau$, and we shall substitute s for $j2\pi f$. That is, $k = -js\tau$, which is combined with Eqs. (8) and (10). Then, we have,

$EZ(r) \quad = - IVIA (-js\mu/4)(-2/j\pi s\tau r)^{0.5} \exp[-s\tau r + j\pi/4)]$

$= - IVIA (s\mu/4)(2/\pi\tau r)^{0.5}(1/s)^{0.5}\exp(-s\tau r)$ (11)

$V(r) = EZ(r)h$ (12)

Note that the voltage between these two parallel plates is linearly proportional to the dielectric thickness, h, and the current in the via, IVIA, and inversely proportional to the square root of r, which is the distance between the current carrying via and the location of interest.

Case I. The via current is a step function of magnitude I0. That is, $IVIA(s) = I0/s$. We have,

$V(s) = - I0h(\mu/4)(2/\pi\tau r)^{0.5}(1/s)^{0.5}\exp(-s\tau r)$ (13)

Note that the inverse Laplace transform of $(1/s)^{p+1}$ is $t^p/\Gamma(p+1)$, where $\Gamma(p+1) = p\Gamma(p)$, and $\Gamma(0.5)=\pi^{0.5}$. [2] Therefore, we have,

$V(t) = - I0h(\mu/4\pi)(2/\tau r)^{0.5} (t-\tau r)^{- 0.5} u(t - \tau r)$ (14)

Case II. The via current is a ramp of magnitude I0, and a rise time of T. That is,

$IVIA(t) = (I0/T)[tu(t) - (t-T)u(t-T)]$ (15)

$IVIA(s) = (I0/s^2T)[1 - \exp(-sT)]$ (16)

$V(s) = -I0h(\mu/4)(2/\pi\tau r)^{0.5}(1/T)(1/s)^{1.5}[\exp(-s\tau r)-\exp(-s\tau r - sT)]$ (17)

$V(t) = -I0h(\mu/2\pi)(2/\tau r)^{0.5}(1/T) \quad [(t-\tau r)^{0.5}u(t-\tau r) - (t-\tau r-T)^{0.5} u(t-\tau r-T)]$ (18)

Case III. The via current is a function of time, but can not be expressed in a closed form. One may approximate it as a composite of many finite step functions, one following the other with appropriate time shift. Or one may approximate it as a composite of many finite ramp functions following each other. From the solution shown in Eq. (14) for Case I, the step function response has a discontinuity at $t=\tau r$. The superposition of responses with discontinuities is prone to error. The response to ramp function as shown in Eq. (18) for Case II is a continuous function. Using composite of

successive ramp functions to approximate a general time-varying function is strongly recommended.

With a driving input signal voltage from a 50-ohm coaxial cable, VDR(t), the voltage across, and the current delivered to a signal line with Z0' = 70 ohms are VNE(t) = VDR(t) x [2x70/(50+70)] and IVIA(t) = 2VDR(t)/(50+70), respectively. The voltage across the 50-ohm termination at the far-end is VFE(t) = VDR(t)[1 - (20/120)^2], which can be measured easily as shown in Figure 3. Here, we have neglected the skin effect and dielectric loss of the signal line

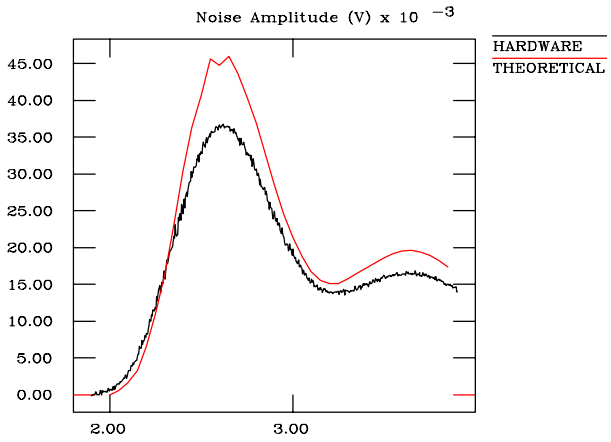


Figure 4. Theoretical Calculation of Case II for E1 Measurement

and cables used in the measurement set-up. IVIA(t) can be derived from the active line far-end voltage data, VFE(t). We may then take the Case III approach, using Eq. (18) shown in Case II as the basis. Note that the voltage so obtained is the voltage between the two reference planes[3] in any interior location, except a region very close to the via where the asymptotic form for the zero-order Hankel function shown in Eq. (10) may have unacceptably large error.

When a via is located at an interior position, the voltage between the reference planes is divided into two parts, one between the top reference plane and the via, another between the via and the bottom reference plane. If the characteristic impedance of the signal line connected to the top end of the via is identical to that connected to the bottom end of the via, these two parts will be equal, being half of that shown in Eq. (18). This is usually referred to as the via coupling noise. [4] In our experimental set-up, Z0' is different from 50 ohms. The voltage across the 50-ohm termination is [100/(Z0'+50)] times one half of the voltage between the two reference plane. On the other hand, at the edge of the board, the boundary condition requires that the normal component of current vanishes, and the voltage between the two reference planes is doubled to that shown in Eq. (18).

If there are several via conductors with driving current, we may use the superposition principle with direction of current flow taken into consideration. The time-of-flight, τ_{rj}, between via #j and the location of interest, enters Eq. (18) in both the magnitude and the delay. The noise due to an active current in a farther away via conductor will arrive later with

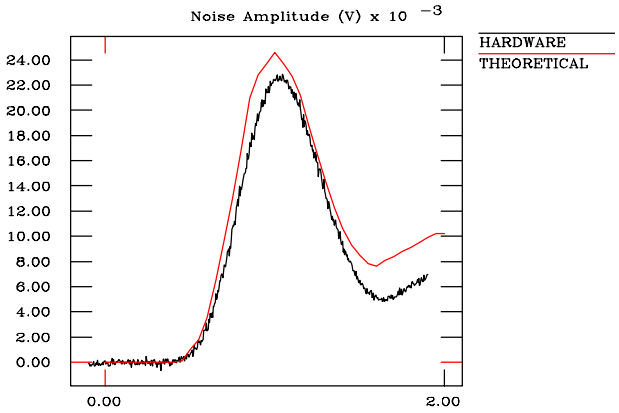


Figure 5. Theoretical Calculation of Case II for 7R Measurement

a magnitude inversely proportional to the square root of the distance.

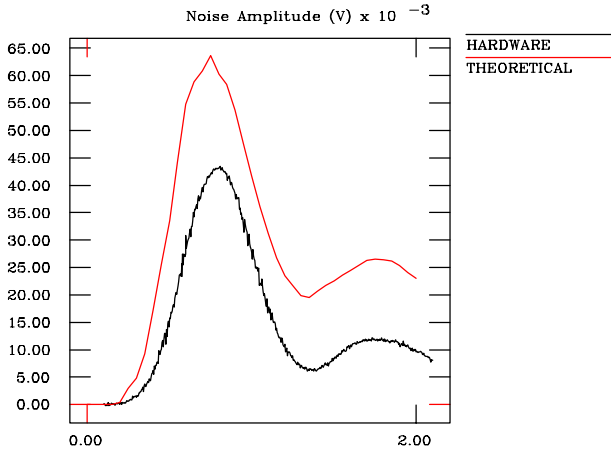


Figure 6. Theoretical Calculation of Case II for 3R Measurement

Figure 4 shows the calculated result for the noise at the edge of the board at location E1 with active signal at four via conductors. The time-of-flight between E1 and the four via conductors ranges from 1.56 to 1.99 ns. The calculated result is close to that obtained by the finite difference time domain full wave solution to be discussed later in this paper, but higher than the measured result by 26%. Further investigation is needed to understand the discrepancy.

Figure 5 shows the calculated result for noise across the terminating resistance at 7R. The time-of-flight between this quiet via and the four active via conductors ranges from 0.27 to 0.33 ns. They are compared with results from different simulation techniques.

Figure 6 shows the calculated result for the noise pulse across the terminating resistance at 3R. The time-of-flight between this quiet via and the four active via conductors ranges from 0.0334 to 0.0667ns. Note that 0.0334 is only one eighth of 0.267ns, which is considered as the limit in the applicability of the asymptotic form of the zero order Hankel's function as discussed in the paragraph after equation (10). The magnitude of the asymptotic form is larger than the exact value by a significant percentage. It is observed that the peak value of the noise pulse is 64mV from the asymptotic approximation calculation. The measurement indicates that it is really 44mV. Another significant error in the calculated noise pulse in Figure's 4,5 and 6 is the long tail. This is due to the low frequency spectrum of the ramp function.

III. Lumped Element Model and Simulation

A lumped element modeling technique currently used for first level chip carriers was employed to model the lab experiment. The lumped element model consists of an inductance matrix with capacitance connected to various nodes of the matrix. The type of model used correlates very well (often within 10%) with hardware measurements of simultaneous switching noise on few layer quad flat packs and ball grid arrays when rise times are greater than 0.5ns.

The inductance matrix was created using the IBM programs L3D* and LEQCKT [5] about which numerous papers have been written. The board was modeled with a matrix of bars or current elements that are used by L3D* to calculate the inductance matrix. Near the vias, signal lines, and probe points, the matrix elements are 1 to 5mm in length while matrix elements for the rest of the board are 10 to 20mm in length. The signal lines, including vias, are modeled with three elements each: one for the trace on each side of the board and the third for the via. The total number of elements used for the inductance model was 5760, producing a 5760x5760 inductance matrix from L3D*. Then, LEQCKT was used to reduce this large matrix to a smaller 67x67 inductance matrix with nodes for connecting capacitors. The combination of L3D* and LEQCKT required 67Mb of DASD, 740Mb of memory, and 3.9 hours to produce the matrix on a RS/6000 model 580.

The capacitance values connected to each node between the two planes were calculated by determining the distance that a voltage wave would propagate through the board within the rise time of the input waveform. Given a rise time of 0.5ns and relative dielectric constant of 4.1, the wave should travel

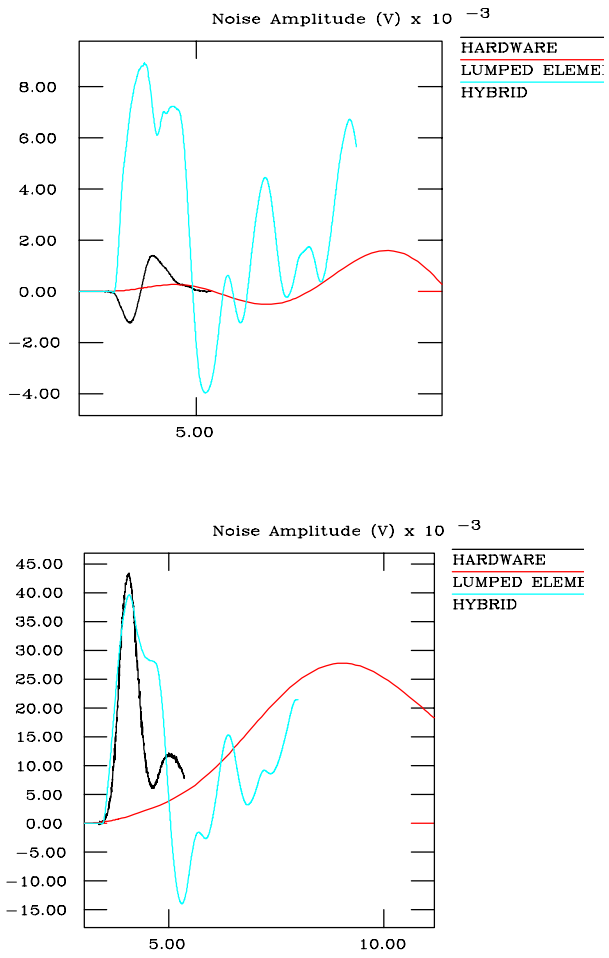


Figure 7. Case II 3R Measurement vs Lumped and Hybrid Simulations

74.1mm in 0.5ns. Using this as the radius of the capacitor, the capacitance value seen by a wave originating from a point at the middle of the board is 440pF. A capacitor at a board edge node was given half of this value and a node at a corner of the board was given 1/4 of 440pF. Nodes closer than 74.1mm were given capacitance values scaled down accordingly. A total of 31 capacitors were used to model the plane to plane capacitance. Finally, the capacitance for the signal lines was calculated using a 2-D capacitance program. This capacitance was divided between the four available

signal line nodes. One node was at each end of the lines and a node was on each end of the via.

The LC model was connected to sources and transmission

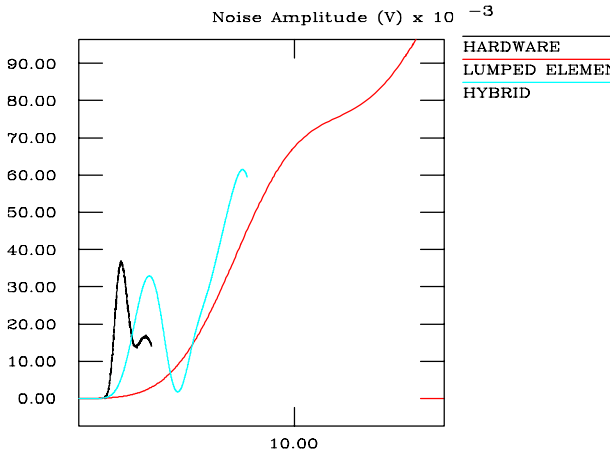


Figure 8. Case II E1 Measurement vs Lumped and Hybrid Simulations

lines in AS/X and the various test cases were simulated. The signal source was a sine-squared waveform with a 0.5nS rise time, a 0.9V amplitude, and an impedance of 50 ohms. Simulation times ranged from 2-5 minutes.

Figures 7, 8, and 9 show the waveforms of three of the test cases. Each figure depicts the actual hardware waveform and the waveforms predicted by both the lumped element model and by the hybrid model described in the next section. In each figure, the darkest and shortest wave is the hardware measurement, only 2ns of data was measured, and the wave with the lowest frequency components is from the lumped element model. Figure 7 depicts Case II, 3R. Figure 8 depicts Case II, E1, and Figure 9 shows Case III, 3R.

It is clearly evident from the figures that the lumped element model does not correctly model the frequency response of the experiment. The lumped element model is basically an LC circuit and it filters the high frequency components. Not shown is the far end active waveform from this model which has a rise time of only 2ns.

The model does predict the peak noise at the quiet vias within 20% when the noise is above 8mV and within a few mV when the noise is less then 8mV. The general wave shape trend is also observable, though the noise pulsewidth has terrible correlation. Thus, the model does predict the canceling effect of Case III. The predicted noise at the board edge is dominated by low frequency components and the model breaks down for this case.

As stated, this modeling technique does correlate well with predicted simultaneous switching noise on few layer SCM's. The dimensions of these packages are typically 40mm or less and the rise times are typically 0.5ns or greater. Hence, the package circuits do not act as transmission lines. However, as the results in this section show, the lumped element model begins to lose accuracy as the current path lengths approach the wavelength of the signal, and the accuracy grows worse as the wavelength grows shorter than the signal path length.

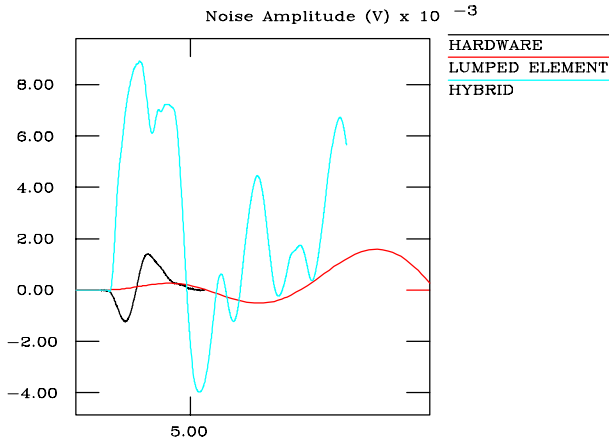


Figure 9. Case III 3R Measurement vs Lumped and Hybrid Simulations

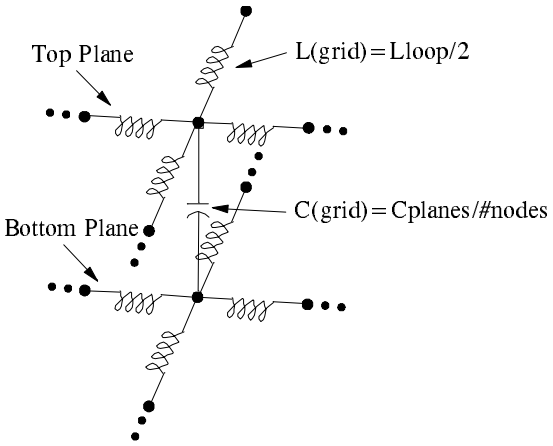


Figure 10. Distributed Grid Reference Plane Model

IV. Hybrid Lumped Element / Transmission Line Model and Simulation

A technique combining the traditional lumped element approach with that of the transmission line model was

applied to the laboratory test described above. This technique is an approximation designed to allow for fast model development and simulation time, while providing additional accuracy beyond the lumped element model. The model is based on a few simple laboratory measurements or readily available material characteristics including signal line characteristic impedance (Z0), relative dielectric constants (Er), signal risetime (tr) and geometric features of the structure.

In principle, a model of the power distribution (or reference planes in this case) and a model of the signal distribution systems are developed independently and married in the circuit simulator to predict the behavior of the test structure.

The double-sided copper-clad board in the test structure is representative of internal power, ground or reference planes in the multiple reference plane package. These two planes can be modeled at various levels of complexity. At the most simple level they form a large parallel plate capacitor. At a more complex level, the plane pair exhibits radial and planar transmission line behavior with factors such as skin-effect resistance and dielectric losses proving significant at high frequencies. [1, 6]

It is first established that the transmission line behavior of this plane pair is not negligible based on the rule of thumb relationship between signal risetime (t_r) and time of flight delay (tf). [7]

$$t_r < 2.5\ t_f$$

The pulse generator risetime of 0.5ns is significantly less than 2.5 times the time of flight delay, in this case about 3.84ns for the 569mm dimension of the plane pair.

The equivalent circuit shown in Figure 10 representing a distributed inductive and capacitive grid was selected to model the plane pair. This grid model is nothing more than an extension to two dimensions of the n-section lumped element equivalent of a transmission line. [8] This model can be seen to orthoganally approximate the radial wave expansion from a point source as well as the uniform planar transmission characteristics of the rectangular plane pair structure.

A key element to the grid model is the determination of the size of the individual grid units which comprise the total model. This was established based on consideration of both the signal risetime and the density of the drilled hole or "via" pattern, clearly the smallest feature of interest in this structure.

The minimum spacing between drilled holes in the structure was 5mm. Time of flight delay for 5mm in this dielectric medium (Er=4.1) is about 34ps. In order to have a model with distinctly addressable nodes representative of this 5mm spacing, the grid model must have nodes separated by an electrical delay of 34ps.

Consideration of the signal risetime provides additional verification of this grid size, as the well known relationship between risetime and frequency, [7]

$$f_c = 0.35 / t_r$$

where fc is the upper half power point of the signal, is applied. It is good practice to construct a network capable of responding to 10-20 times this 3dB frequency limit, in this case suggesting a grid unit delay of about 71ps. The limiting grid unit delay of 34ps was selected.

Once the grid unit delay is established, calculation of the model parameters Ls and Cm is based on the per unit time delay td of the ideal uniform transmission line

$$t_d = (LC)^{1/2}$$

where L and C represent the per unit inductance and capacitance of the ideal lossless transmission line respectively. Several assumptions are apparent here, including the independence of inductance and capacitance with frequency. Series DC resistances are ignored hereas well as the AC frequency-dependent effects such as dispersion introduced by dielectric losses and skin resistance.

Initially, it was attempted to construct a grid model of the entire 569x471mm structure with the 5mm or 34ps grid density. This resulted in a grid model of 114x95 nodes. Unfortunately, a grid model this size proved too large to obtain a solution for on the available RS/6000 workstations. An alternate solution was then developed which employed a variable grid density. Since the 5mm via grid was clustered in the center of the board, it was determined that a fine grid of 34ps would be used in the via area and a less dense grid would be employed on the balance of the structure. This reduction in circuit elements and nodes was adequate to obtain a solution on the available computer resources.

The modeling of the signal distribution system, including coaxial cables, #30 signal wires and "vias" again involved a combination of lumped element and transmission line modeling techniques. The 50ohm coaxial cables and 68ohm #30 signal conductors were modeled as lossless transmission lines. IBM's AS/X circuit simulator implementation of the ideal transmission line was applied. Per unit time delay was calculated based on assumed dielectric constants. A four-terminal model with separate input and output reference nodes was created for the top- and bottom-referenced signal

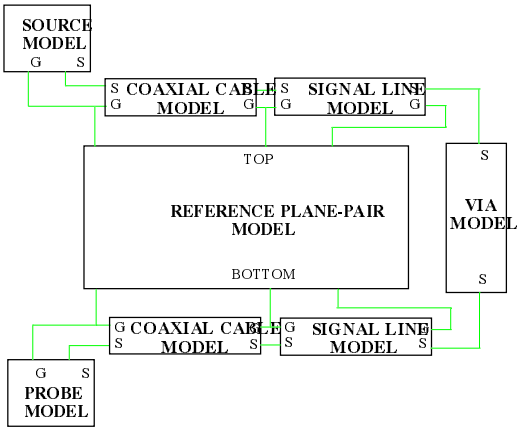


Figure 11. Block Diagram of Hybrid Model Simulation

lines. This allowed signal return current to be injected at the appropriate point in the reference plane pair model.

The "vias" or sections of #30 conductor which ran through the drilled holes from the top to the bottom of the board structure were modeled in IBM's three-dimensional inductance calculator, L3D*. [5] A matrix of self and mutual inductances for the seven vias was calculated.

These models were then interconnected in the circuit simulator. A pulse input function of sine-squared characteristics with a series 50 source impedance was selected to simulate the laboratory pulse generator. The amplitude and risetime of this source were adjusted until they matched the laboratory active measurement at the far end of line 2L. Figure 11 shows a block diagram of the circuit simulated. Noise was simulated for the various conditions of active lines. Amplitude and pulsewidth comparisons with the laboratory measurement are shown in Table A.

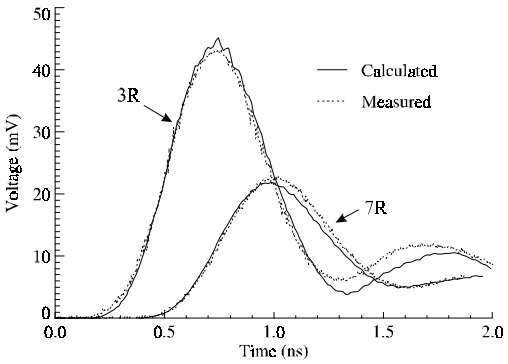
Representative waveform comparisons are shown in Figures 7-9. The hybrid model wave shape results compare favorably to lab measurements. Amplitude correlations are not satisfactoy except for Case II, 3R and E1. The 7R observation points consistently yielded significantly higher results than hardware. It is suspected that the transition from fine grid to coarse grid is causing undue reflections and increasing the amplitude of simulated results. A 10:1 ratio fine:coarse grid was used. A larger fine grid area or smaller ratio of transition from fine to coarse grid should improve correlation significantly.

It is obvious that the attempt to include radial and planar transmission line behavior in the model resulted in a higher frequency response than the lumped element model. However, inconsistencies in amplitude and waveshape correlation suggest further refinement is required. The model also is rather cumbersome to refine and requires significant simulation time as the grid is made finer. Simulation times ranged from 3-25 minutes on a RS/6000 Model 560.

V. Full Wave Numerical Solution

The electrical simulation software, developed at the State University of New York at Binghamton, is for the signal integrity analysis of electronic packages [9]. The main feature of this program is the integration of circuit and transmission line solvers with an electromagnetic field solver that simulates electromagnetic field propagation inside packages. Circuit analysis is carried out simultaneously with electromagnetic field analysis. In this tool, power and ground planes are not treated as ideal power and ground planes with fixed potentials. Voltage variations at any points on power and ground planes are computed. Interactions between circuit and package as well as electromagnetic interactions inside packages, such as resonance and coupling between vias, are taken into account in the simulation.

Electromagnetic fields inside packages are decomposed into several modes according to special geometric features of packaging structures. Special field computation algorithms developed for such modes enable very rapid simulation of electromagnetic wave propagation inside packages. In the computation of power and ground voltage fluctuations, numerical meshes are used for the discretized model of the



power and ground planes. It has been found that the numerical errors resulted from the discretization of power

Figure 12. Measurement and Numerical Simulated Voltages for Case II 3R and 7R

and ground planes can be virtually eliminated by an impedance transformation technique. [10,11]

For circuit analysis, distributed circuit solvers instead of one single circuit solver are used [9]. If two circuit networks are connected by package interconnects, then they are solved by two separate circuit solvers. The interconnections between

the two circuit networks are through the transmission line solvers and/or electromagnetic plane solvers. With the distributed circuit solver approach, each circuit solver deals with a relatively small size of circuit network, resulting in much more efficient and stable circuit analysis than the approach of using only one circuit solver for all the circuit

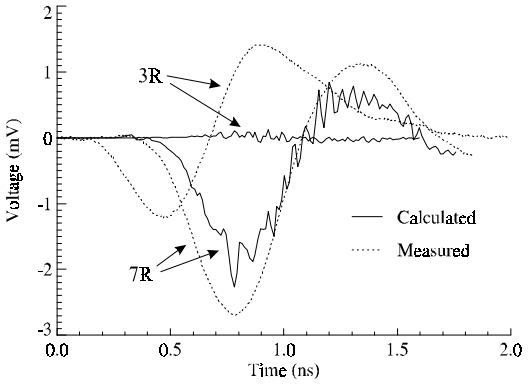


Figure 13. Measurement and Numerical Simulated Voltages for Case III 3R and 7R

networks.

The software tool takes a text input file which describes geometry and material information of package components as well as circuit networks connected to a package. The program .

computes signal and noise waveforms in the package. Simulation results can be stored in data files, and/or displayed on a screen, for example, to animate the ground and power bounces at various package layers.

Figure 12 and 13 show the comparison between the measurement and the full wave numerical simulation. Figure 12 is for the additive case, Case II, when 1R, 2L, 4L and 5R are each driven by a source of the same waveform. The measured data of the source waveform is used as the source in the numerical simulation. Responses shown in figure 12 are at 3R and 7R. It can be seen that, at both observation points, numerical simulations agree with measurements very well in both magnitude and waveform. Figure 13 is for the case when 1R, 2L, 4R and 5L are each connected to a source of the same waveform, Case III. Currents in vias of line 1 and 2 are in opposite direction with the currents in vias of line 4 and 5. Numerically simulated voltage at 3R is virtually zero while the peak measured voltage is about 1.4 mV. The voltage at 7R from the numerical simulation resembles that obtained from the measurement with a magnitude difference of about half millivolt.

Simulation time for each case is about 5 minutes with the display of graphics animation of the voltage fluctuation, and about 40 seconds without the graphics animation.

IV. Conclusion

A simplified laboratory experiment designed to demonstrate noise generated by simultaneously switching circuits on a multi-reference plane package with vias has been described. Measurements of various swithcing events are described and presented.

A theoretical full wave solution of the experiment and three modeling techniques are also presented and discussed along with predicted results. The theoretical solution agrees very well with experimental results. The equations derived provide valuable insight into the behavior of the multi-refernce plane structure with vias. The modeling techniques of increasing complexity from lumped element to hybrid to the numerical full wave solution provide increasingly accurate results.

The lumped element method predicts general waveshape trends and peak noise at quiet vias but fails to correctly predict frequency response of the circut and noise at the edge of the board. The lumped element technique does not work well when the package wavelength approaches the wavelength of the circuit rise time frequency components. The hybrid modeling technique does predict frequency response well compared to the lumped element technique. It's predictions of noise amplitude agreed favorably for the additive test cases but the model needs a finer grid to correlate for the case where via currents were canceling.

The numerical full wave solution yields exceptional agreement with experimental results in noise amplitude and waveshape. This technique offers the accuracy of the theoretical solution in an integrated model/simulation package with dramatic reductions in solution time compared to the other techniques.

As circuit risetimes continue to decrease relative to package and chip time-of-flight, it becomes necessary to utilize full wave solutions to accurately model the behavior of the signal and power distrbution systems.

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