How to Efficiently Analyze a DDR4 Interface

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MemCon 2015

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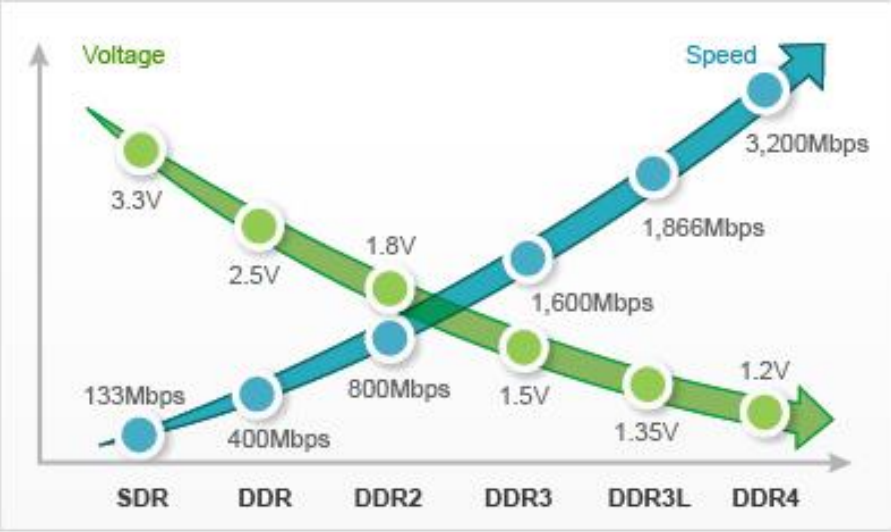
Agenda

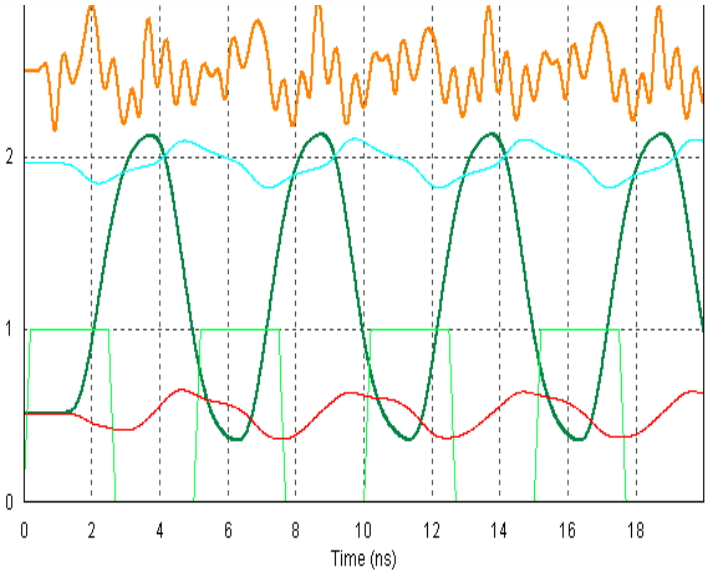
- Power-aware signal integrity (SI) in memory bus design and analysis
- Modeling methodology for integrated core and power-aware parallel bus system with Cadence-Sigrity tools
- Building an integrated core and power-aware parallel bus system in Cadence-Sigrity tool environment
- Case study
  - A virtual reference design based on the Cadence DDR4 IP test chip, package, and PCB
  - Simulation and measurement correlation

Parallel Bus Analysis at System Level

Challenges to classic SI tools

- As clock rate goes up and design density increases, memory design faces more challenges
  - Data rates increase
  - Core voltage and I/O voltage decrease
  - Impact of power noise on signal increases
  - Noise budget decreases
- SI tools need to provide solutions to meet new design requirements





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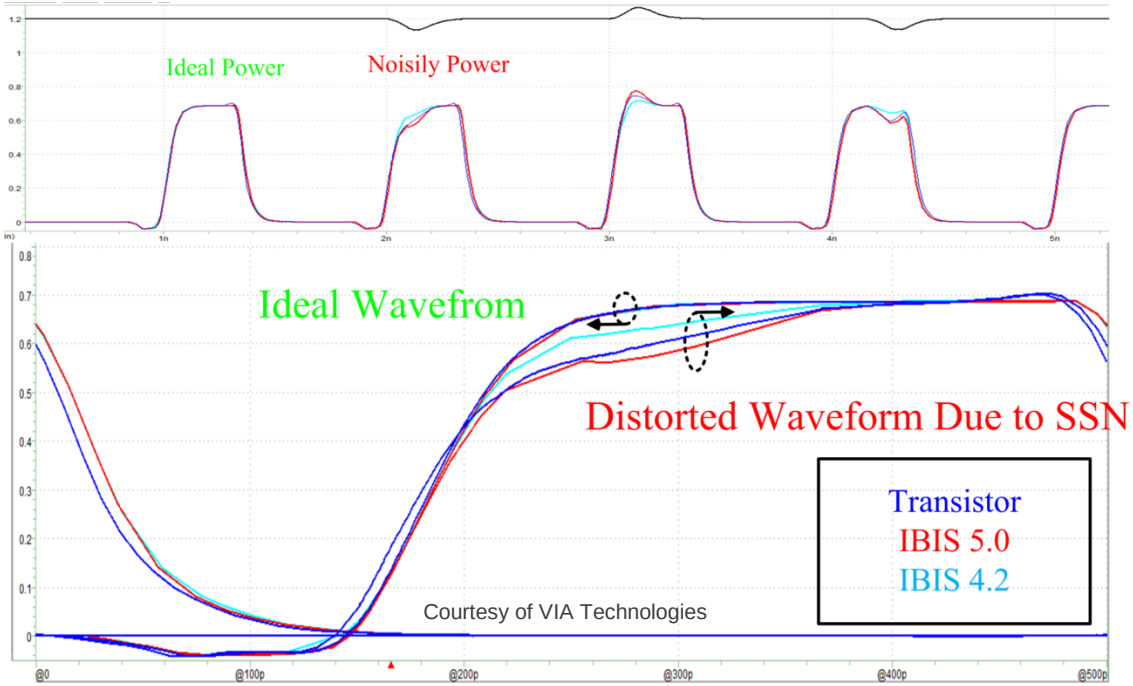
SSO/SSN impact on design

- Design problems caused by SSO
  - False triggers due to power/ground level changes
  - Reduced timing margin due to SSO induced skew
  - Reduced voltage margin due to power/ground noise
  - Slew rate variation



DDR4 technology demands

- Increasing data rates
- Shrinking design margin
- Decreasing power
- Introducing serial link design methodologies
  - JEDEC standard specifies BER for data signals
- Design and analysis need to consider core and system at the same time

Modeling methodology for integrated core and power aware parallel bus system with Cadence-Sigrity tools

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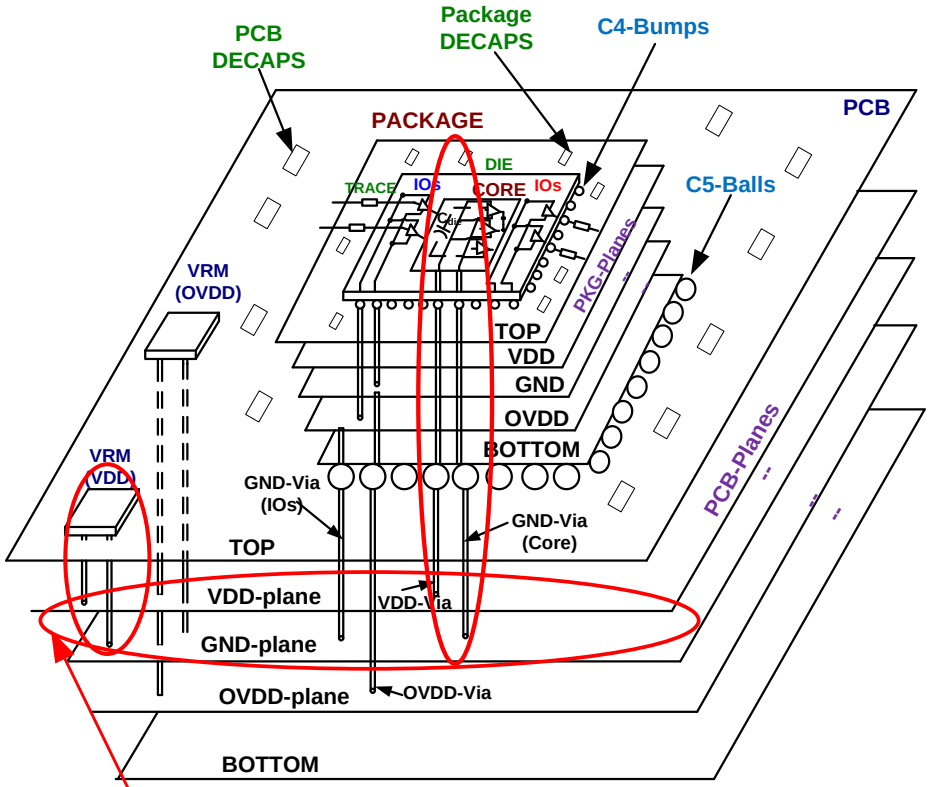
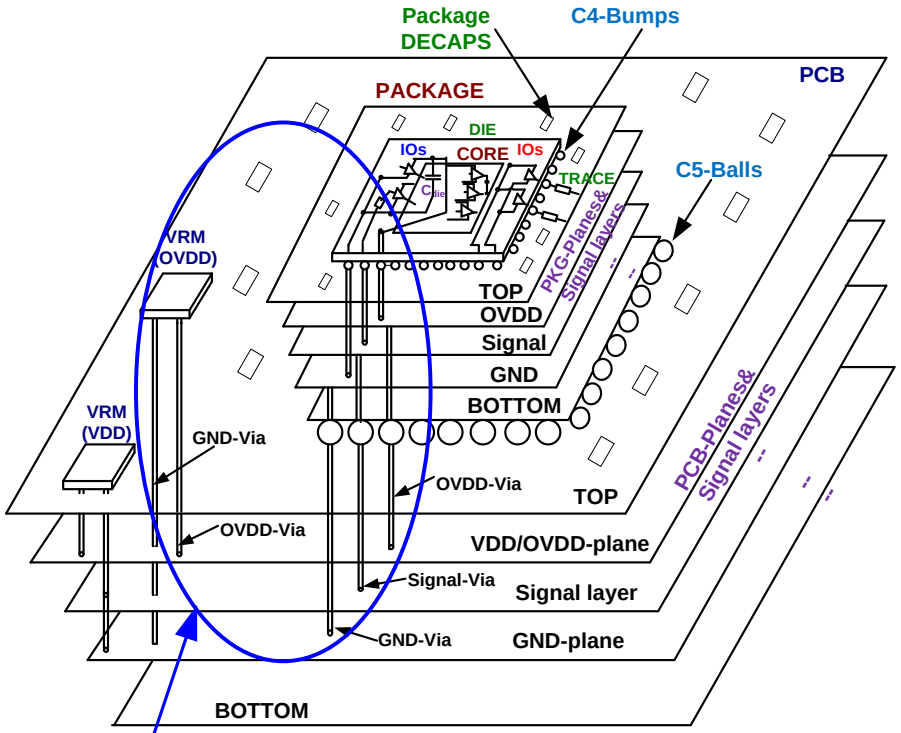
Core and power-aware parallel bus systems

- Core System



Core Power Distribution Path for POWER-INTEGRITY (PI)

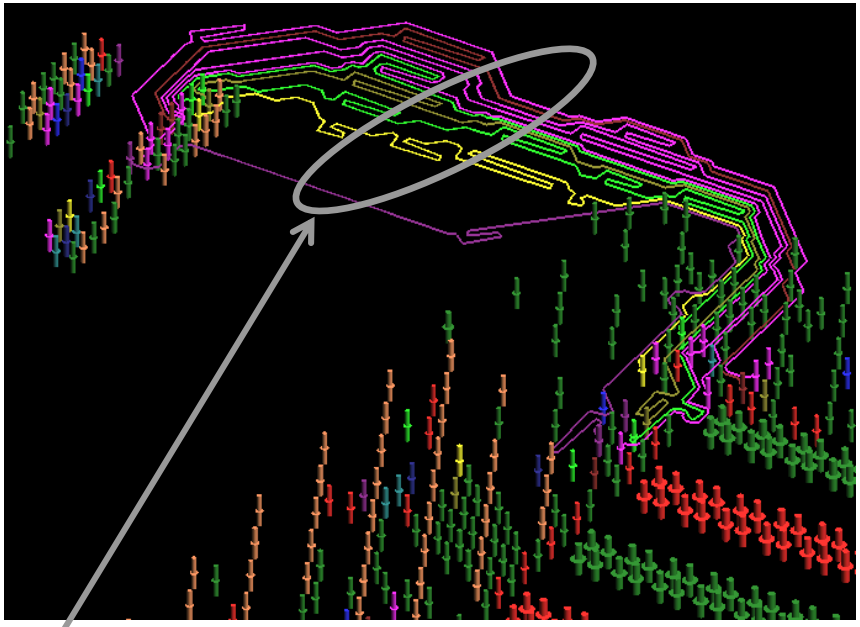
- Power-Aware Parallel Bus System



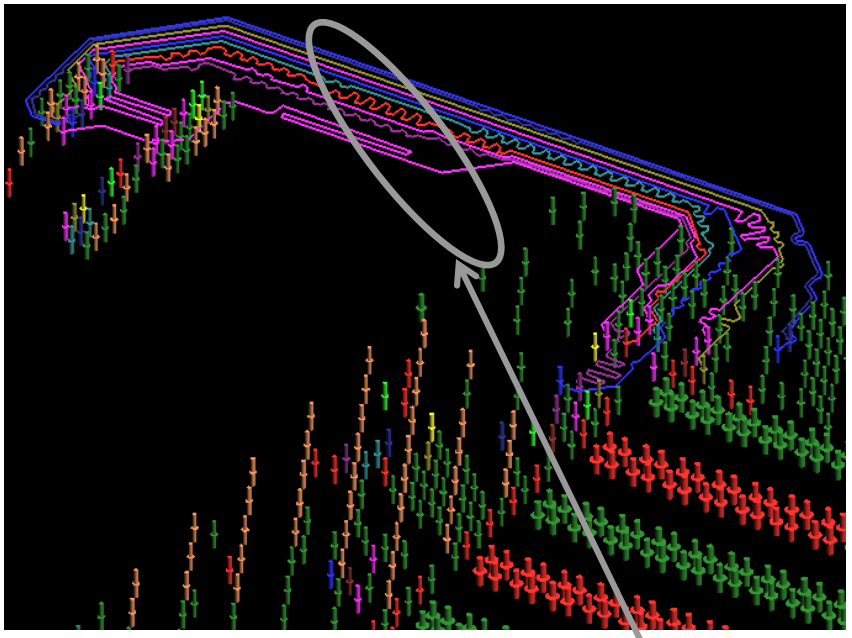
SIGNALS Switching through power and ground references

Power-aware parallel bus

- PCB parallel bus consists of data and strobe signal nets and power distribution network (PDN)



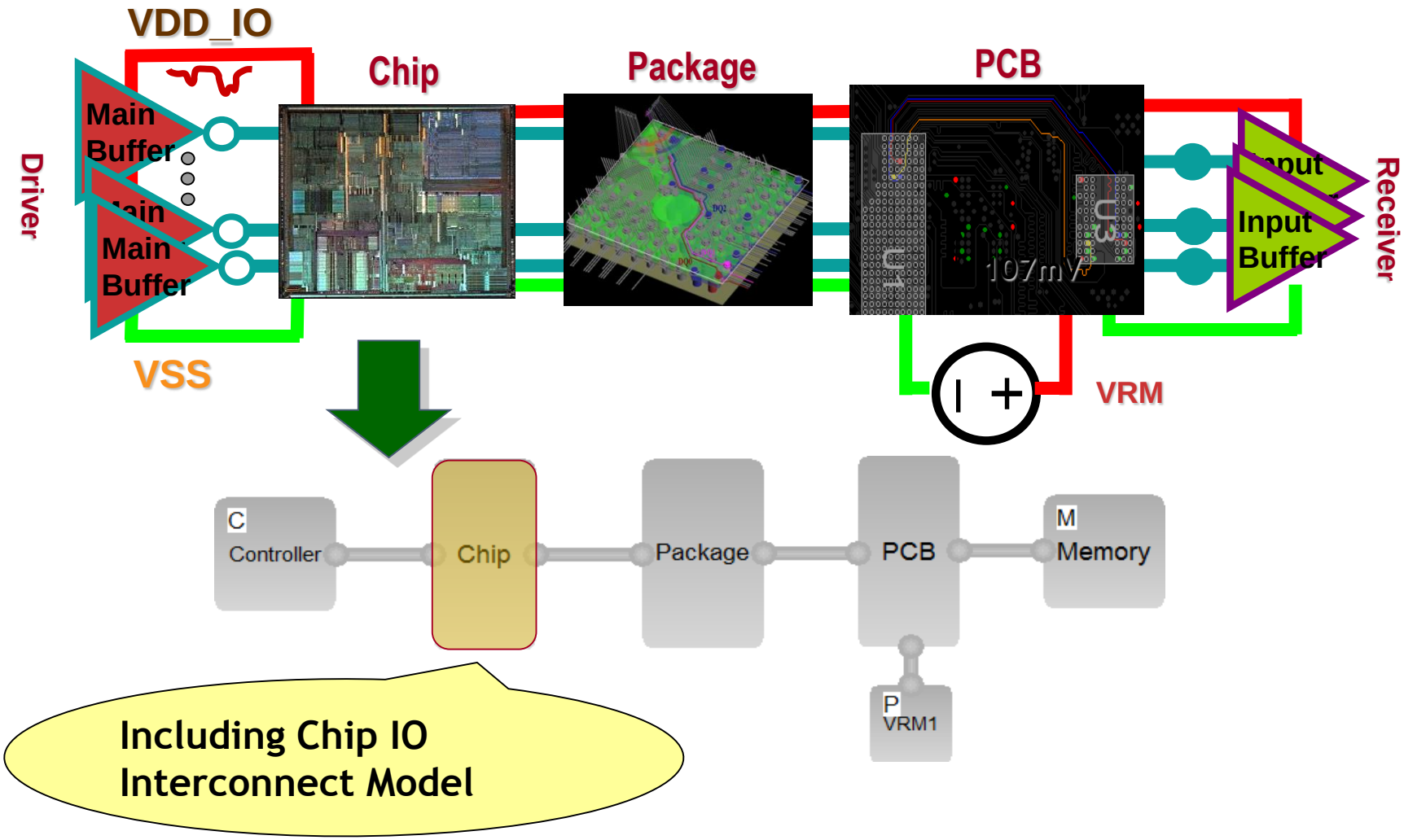
1st-byte lane of
- DATA (DQ<0>-DQ<7>) and
- STROBE (DQS_N<0> & DQS_P<0>)



2nd-byte lane of
- DATA (DQ<8>-DQ<15>) and
- STROBE (DQS_N<1> & DQS_P<1>)

- PDNs consists of PWR and GND planes of PCB (packages)

Cadence IO SSO Chip-PKG-PCB Co-Simulation



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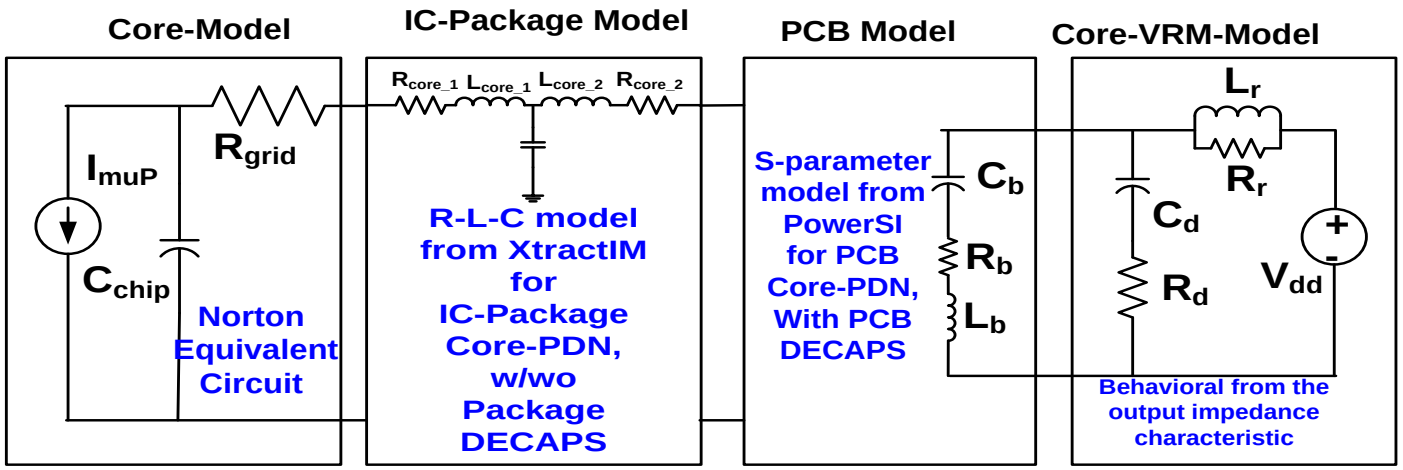
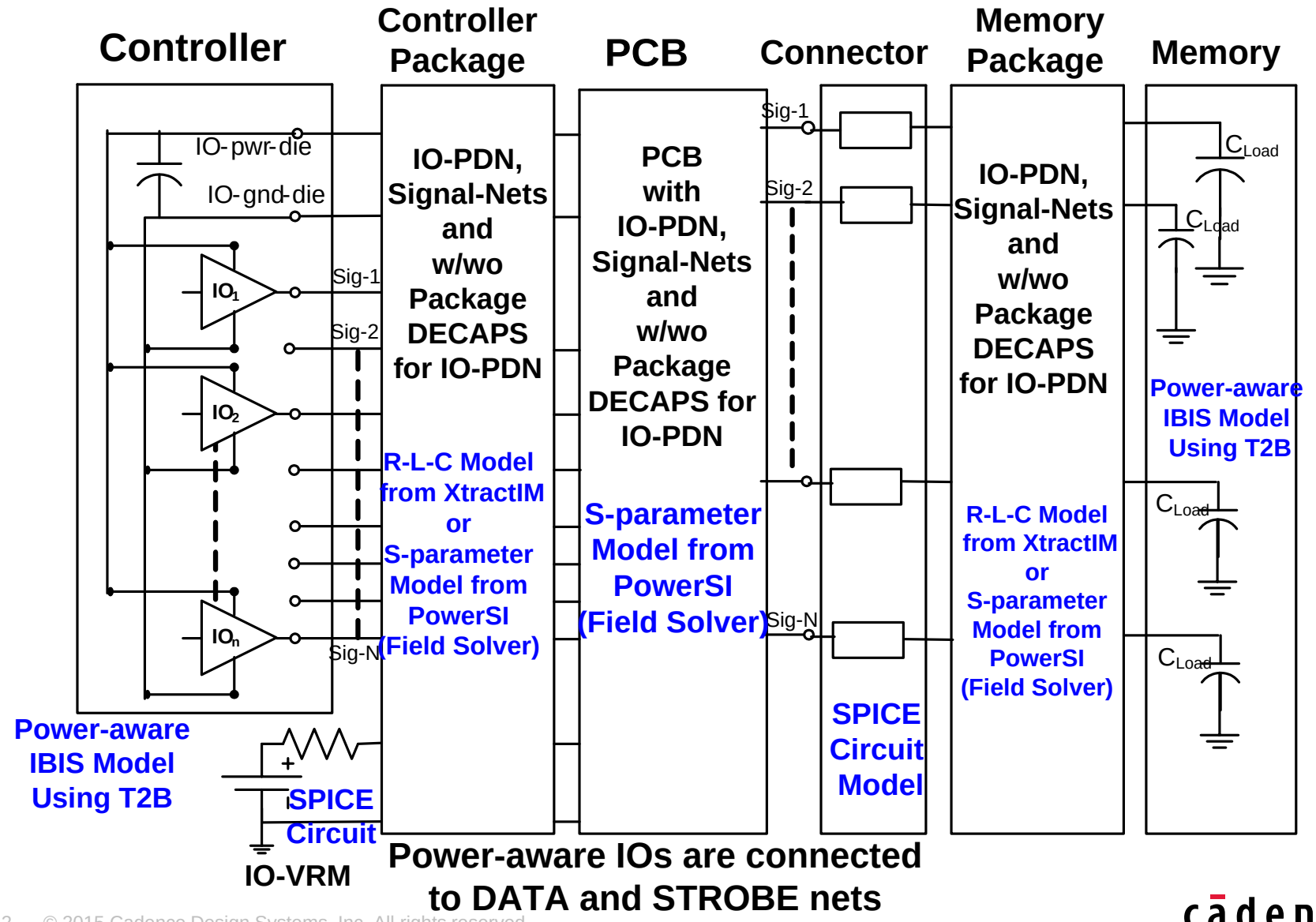
Core-system model

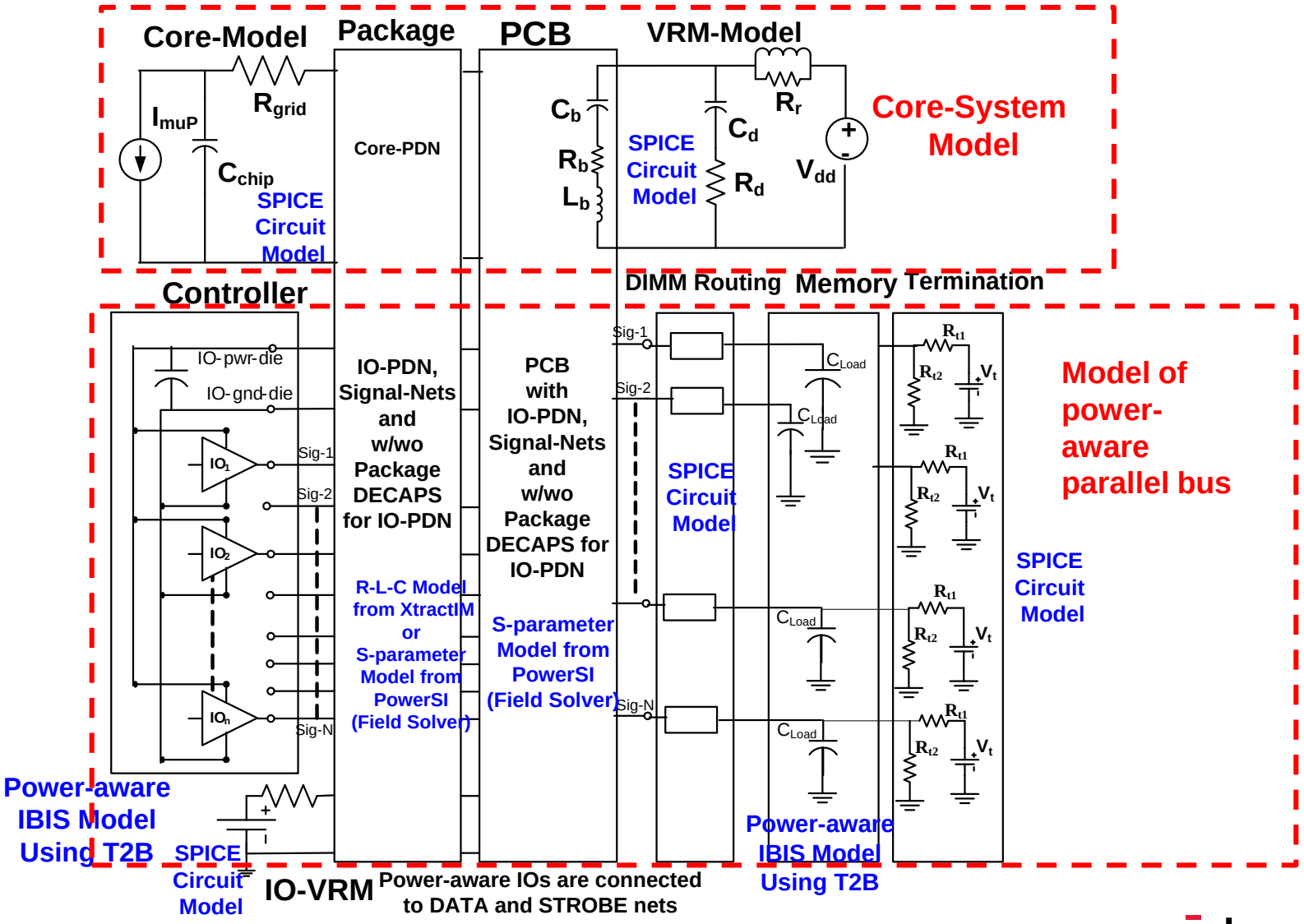


- R_{grid}, C_{chip} values and current profile are critical for optimizing power integrity performance of Core-PDN
- Minimizing transient voltage drop at the core is critical to guarantee the specified core-operating frequency

A model of power-aware parallel bus system



Integrated core and power-aware parallel bus system



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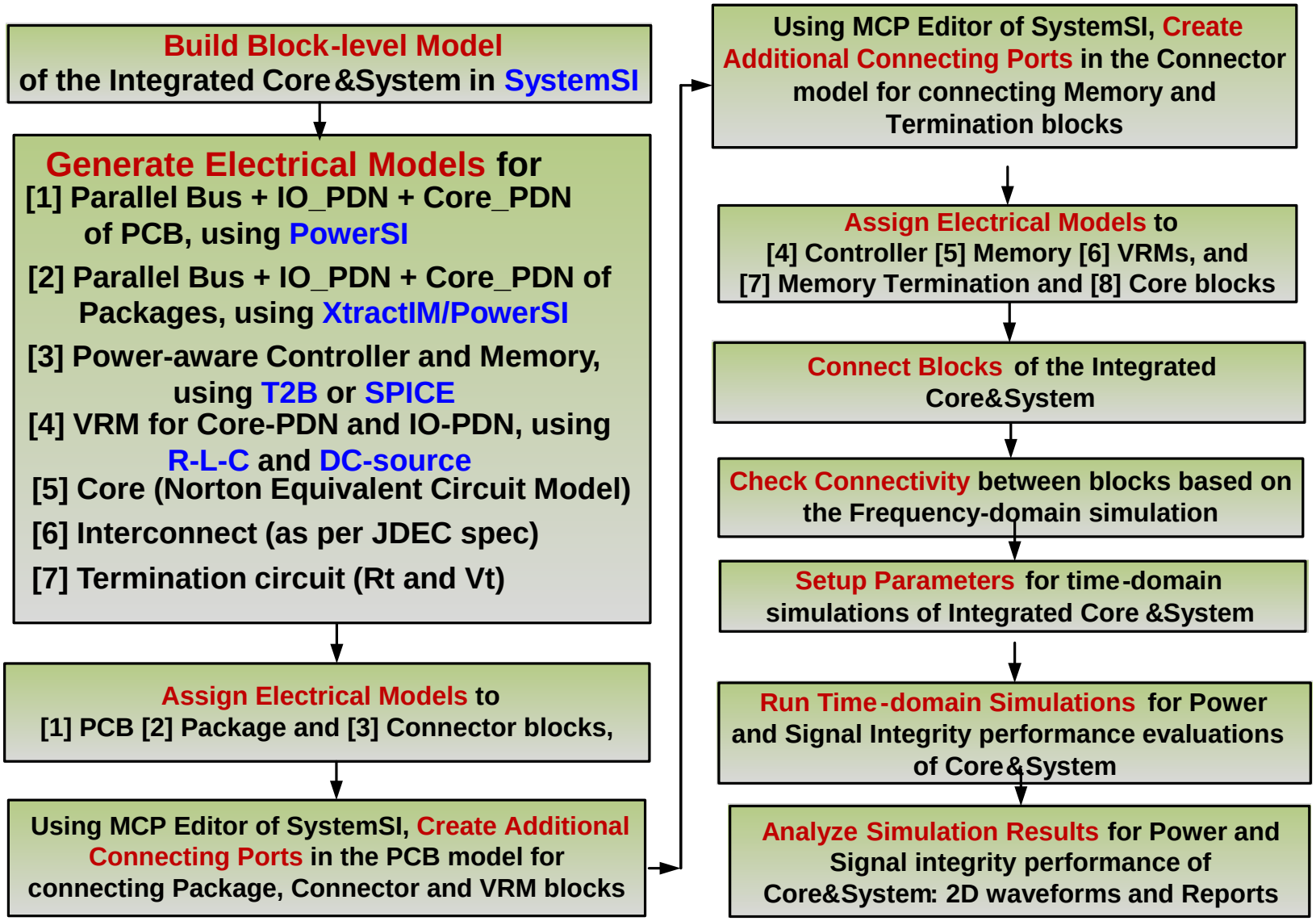
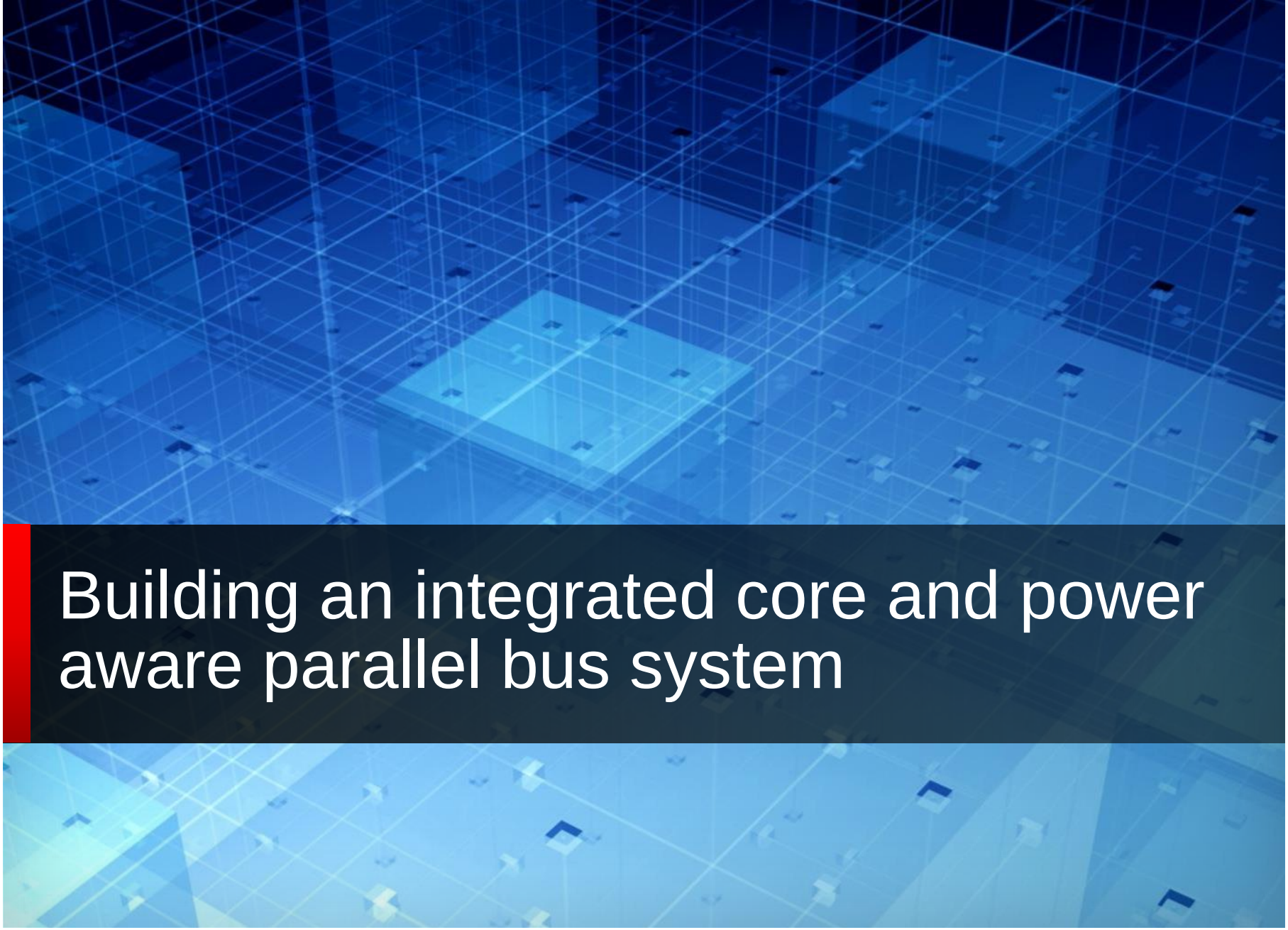
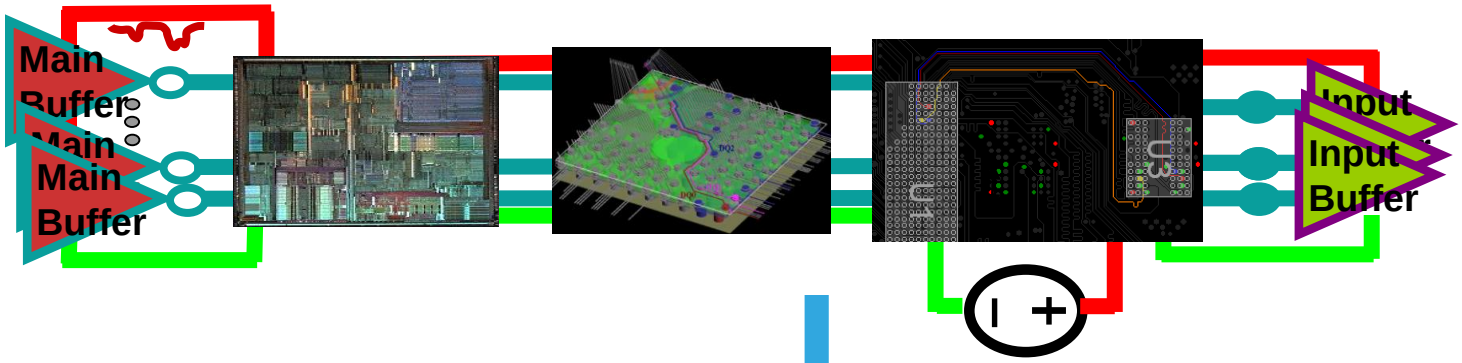
Efficient modeling simulation and analysis process for core and system

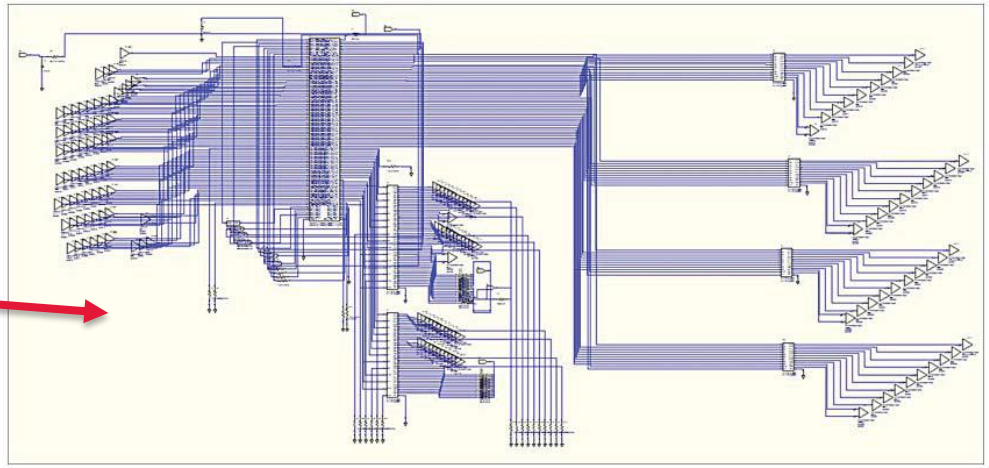




Today's parallel bus design needs new functions for system level design and verification

- Traditionally, all connections of sub-systems have to appear in topology editor
- The complexity of power-aware system makes setup and connection very difficult





Impossible/impractical to connect all sub-system representations, S-parameters and Spice circuits with many ports, in a topology-editing-only environment

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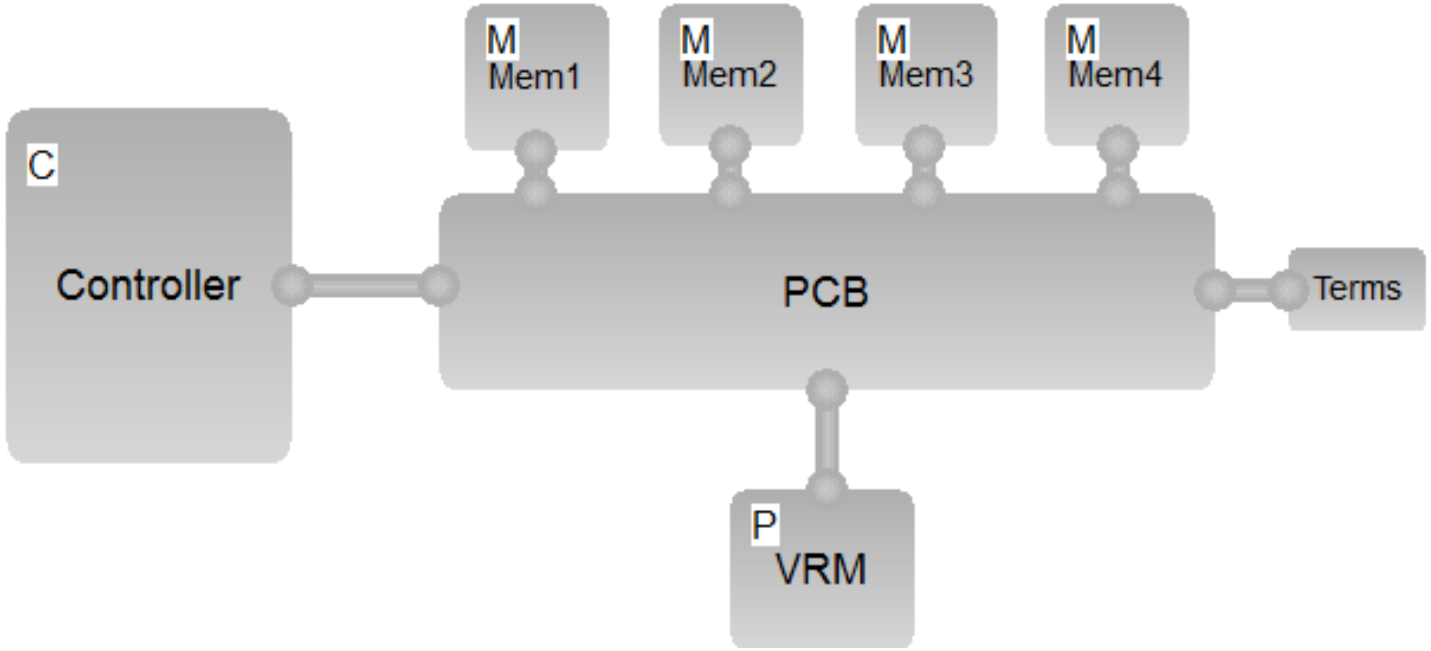
Power-aware SI: Cadence® Sigrity™ SystemSI™ technology

- An evolution from topology based environment and physical layout
  - Keeping the advantage of topology editing
  - Providing a clear view of system connection



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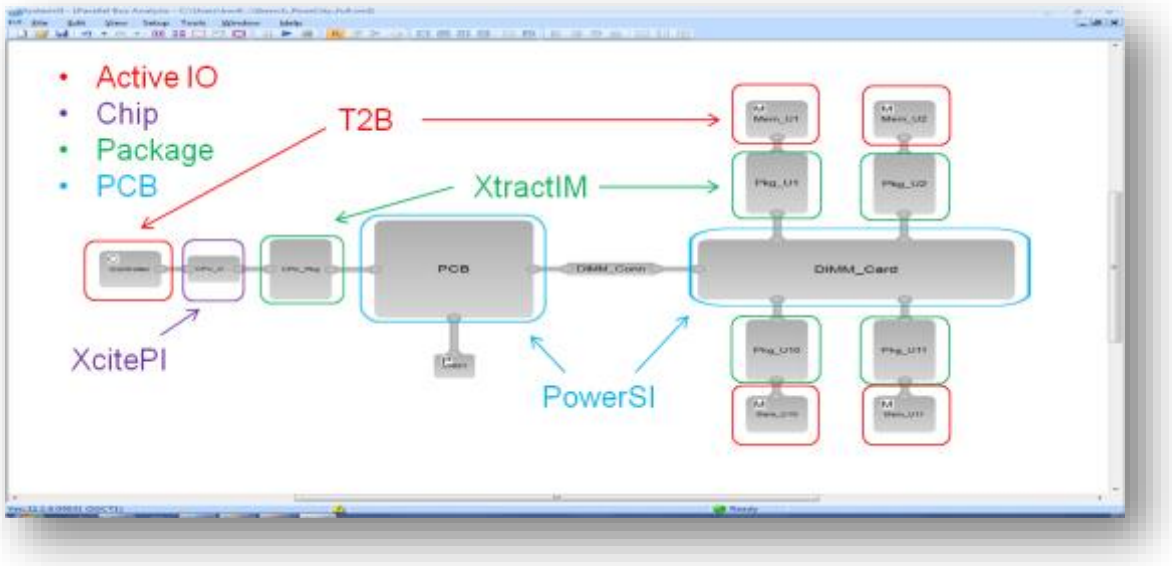
Power-aware SI: Cadence® Sigrity™ SystemSI™ technology (cont')

- Hierarchical bus topologies
  - As simple and direct as in topology environment for pre-layout exploration
  - As efficient and complete as in physical layout for sub-system connections



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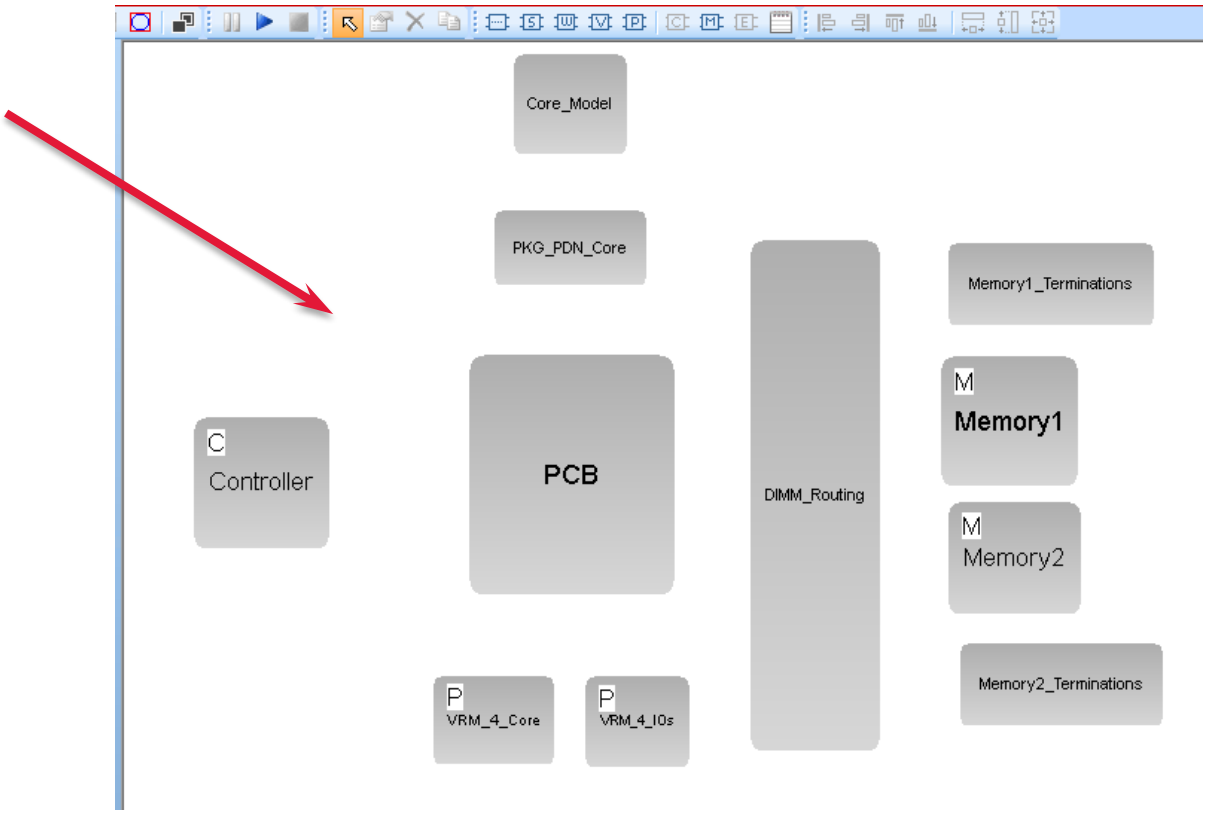
SystemSI™ as the design platform

- Blocks represent each sub-system for the integrated core and power-aware parallel bus system
- Built-in, application-specific blocks for
  - Controller
  - Memory,
  - VRM and
  - Add blocks



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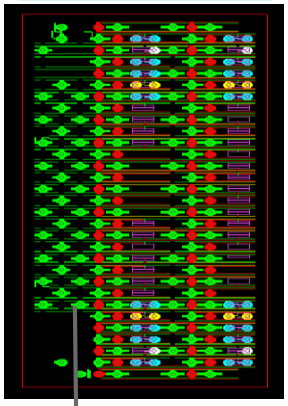
Electrical model generation

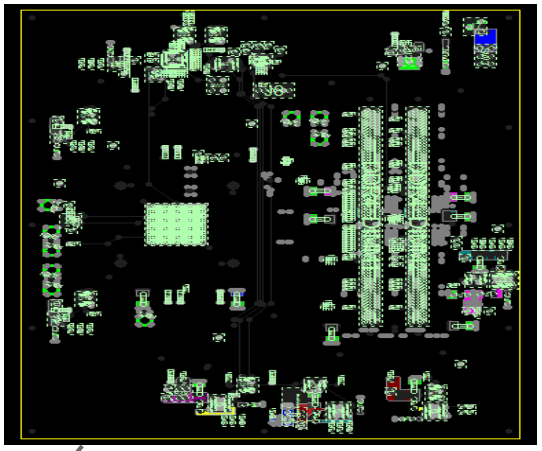
T2B™

```
|**********************************************
| IBIS file created by T2B Version 12.0.8.0513
| Cadence Design Systems, Inc. 2011
|**********************************************
[IBIS ver] 5.0
[File name]  ddr4.ibs
[File Rev]  1.0
[Date]   Thu Sep  5 08:59:40 2013
[Notes] For use with data-rates >= 1.2G the si
|
|**********************************************
|
|**********************************************
|
[Component] DDR4
[Manufacturer] cadence
[Package]
| variable       typ                min
R_pkg   0.0              0.0
L_pkg   0.0H             0.0H
C_pkg   0.0F             0.0F
|
[Pin]  signal_name          model_name
1      DQ                   ocd
4      power                Power
5      gnd                  Gnd
```

XcitePI™

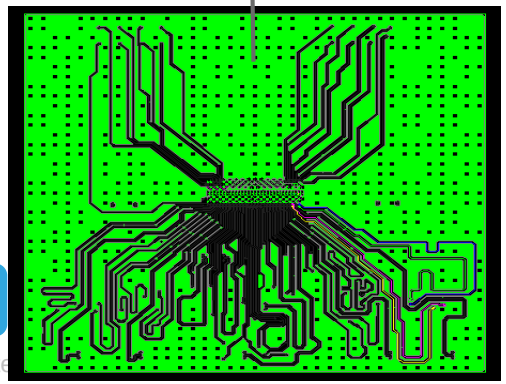


PowerSI™

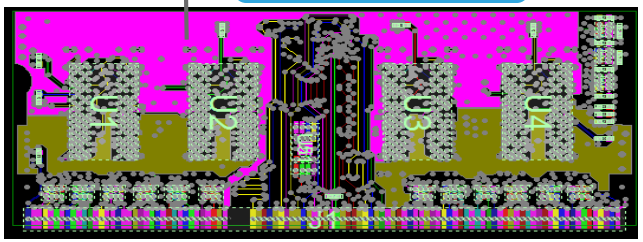


T2B™

XtractIM™



PowerSI™



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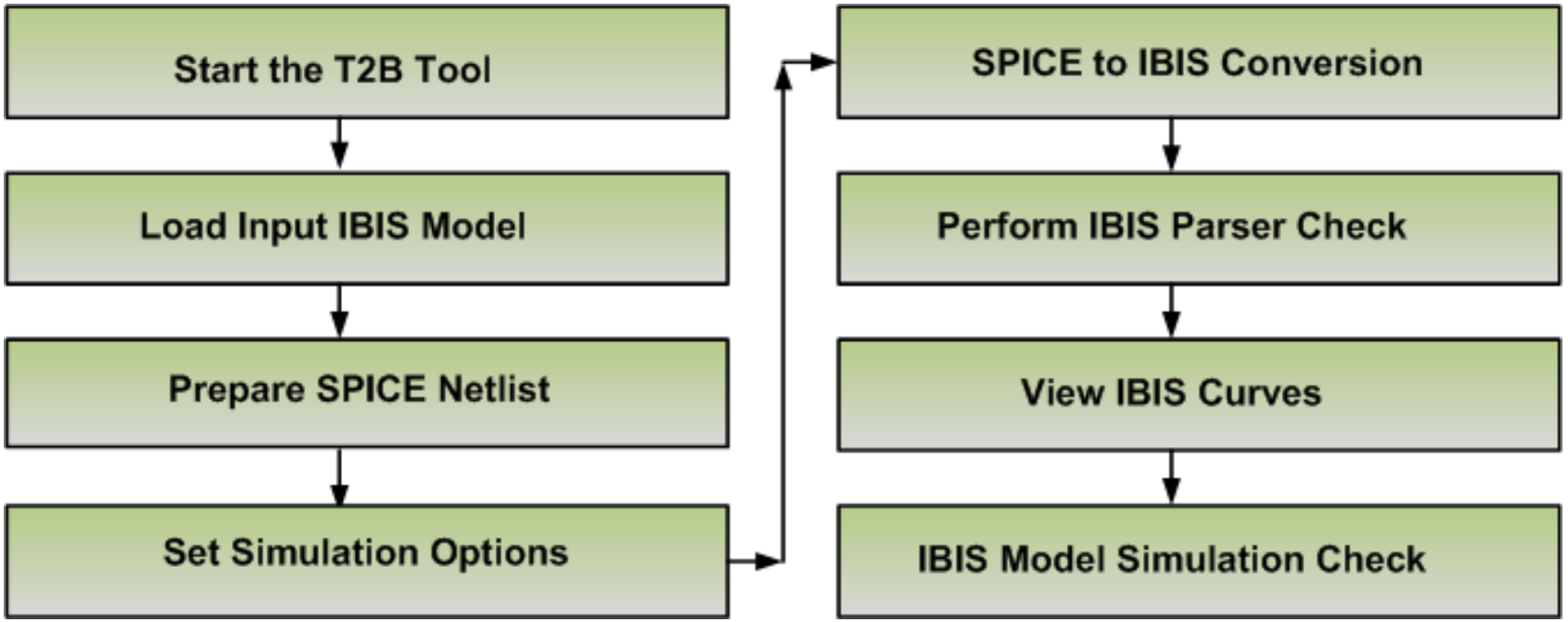
Power-aware IBIS I/O models

- Power-aware I/O buffer models for the controller and memory devices are “must have” for time-domain SSN simulations
  - IBIS 5.0 standard provides power/ground current details
    - Pre-driver current, crow-bar current, and on-die decap current information
  - Simulation with IBIS 5.0 models is efficient and proven-accurate
- Sigrity™ T2B (transistor-to-behavioral) tool generates the power-aware IBIS models in 5.0 standard

Power-aware IBIS model generation using T2B™ tool

- Sigrity™ T2B™ model conversion utility tool can be used for efficiently converting
  - SPICE-Transistor I/O models to power-aware IBIS I/O models, standard v5.0



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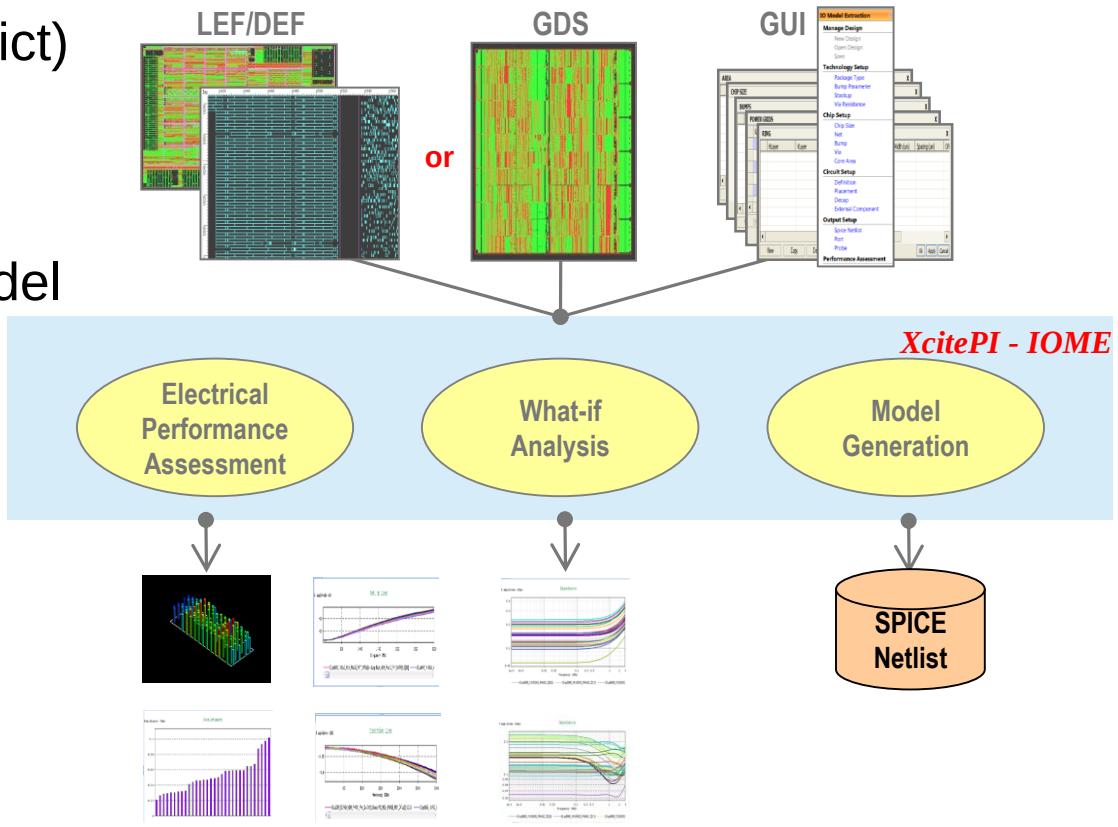
Core model extraction using XcitePI™

Inputs

- LEF/DEF or GDS
- Cadence technology file (.ict)
- XcitePI configuration file

Outputs

- Core / IO interconnect model
  - SPICE netlist
- Model results
  - Power pin RL
  - Power net capacitance
  - Power net impedance
  - Signal net RLC
  - Signal net return and insertion loss



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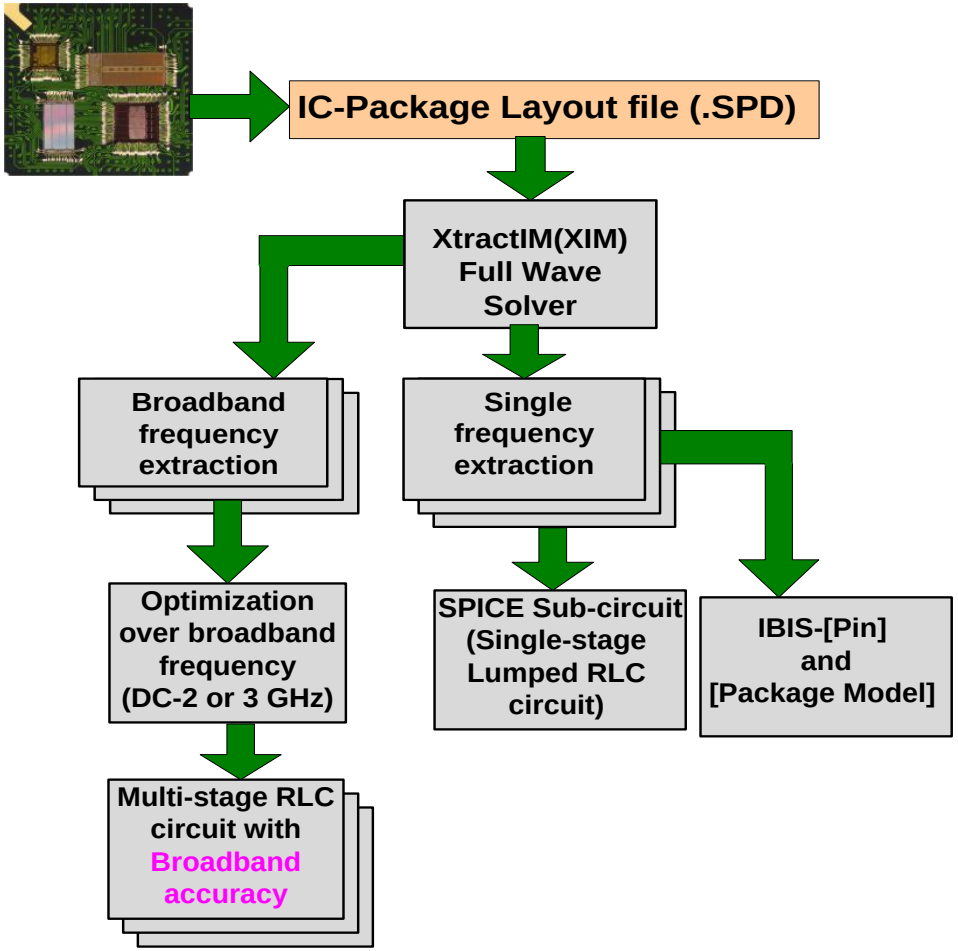
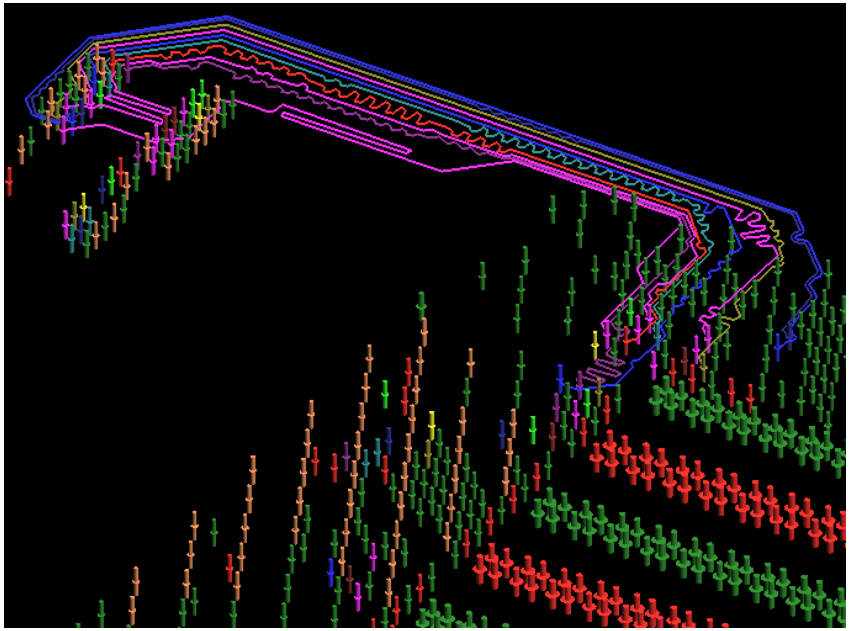
Package model generation using Sigrity™ XtractIM™ tool

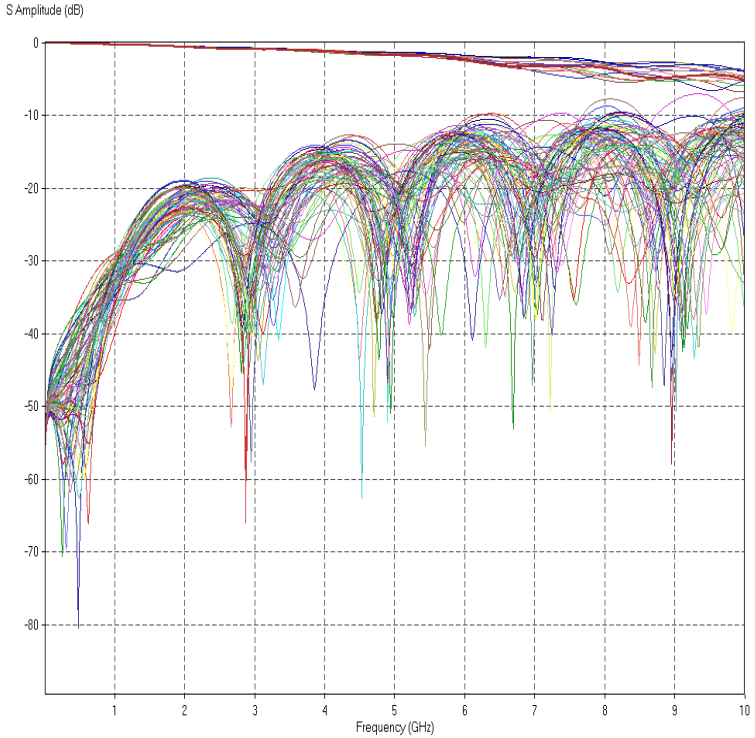
- Package model for core and system can be extracted using Sigrity™ XtractIM™ tool



PCB model generation using Sigrity™ PowerSI™ tool

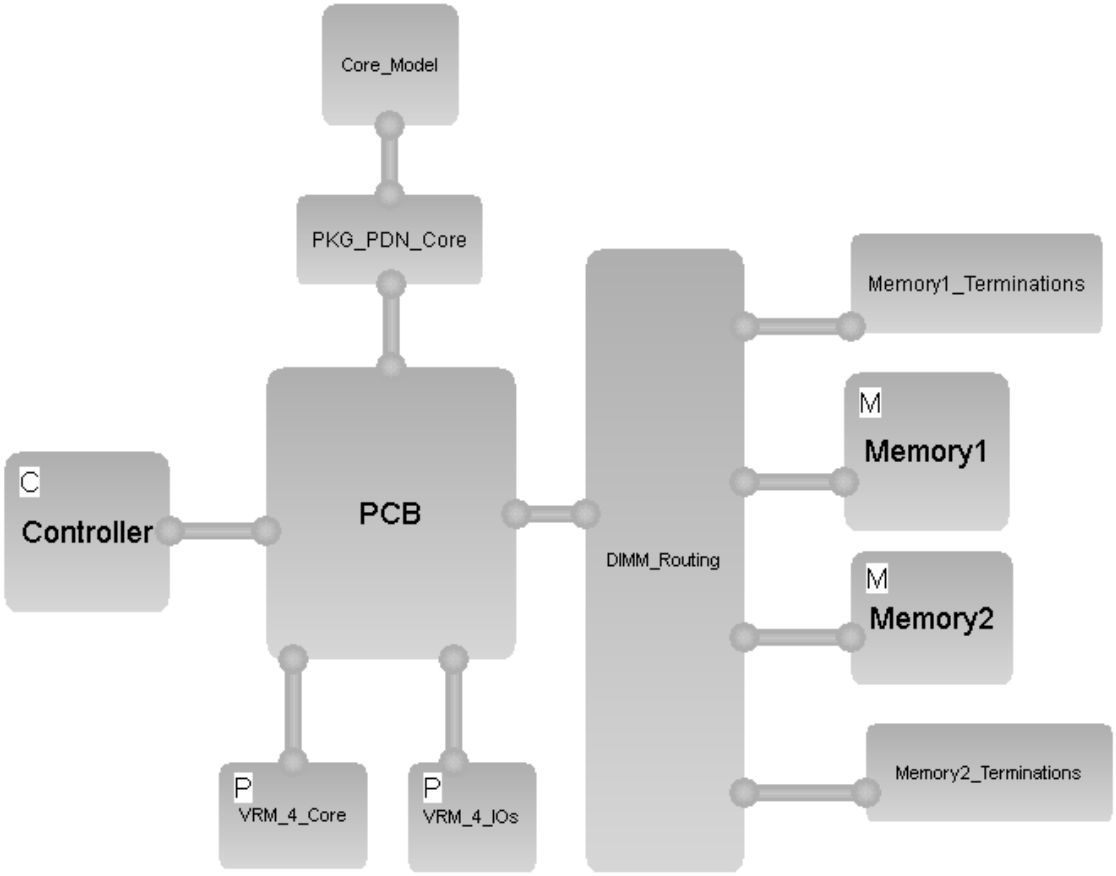
- S-parameter model of PCB contains couplings between signals and power nets, with true return path represented





Connecting blocks in SystemSI™

- Blocks of core and power-aware parallel bus system are connected through MCP (Model Connection Protocol)



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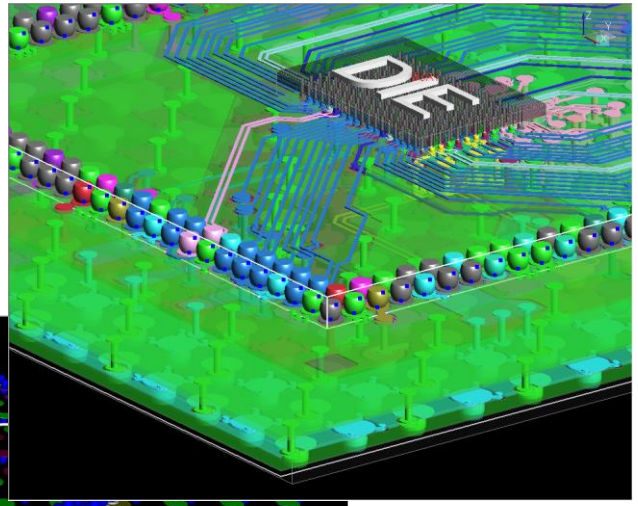
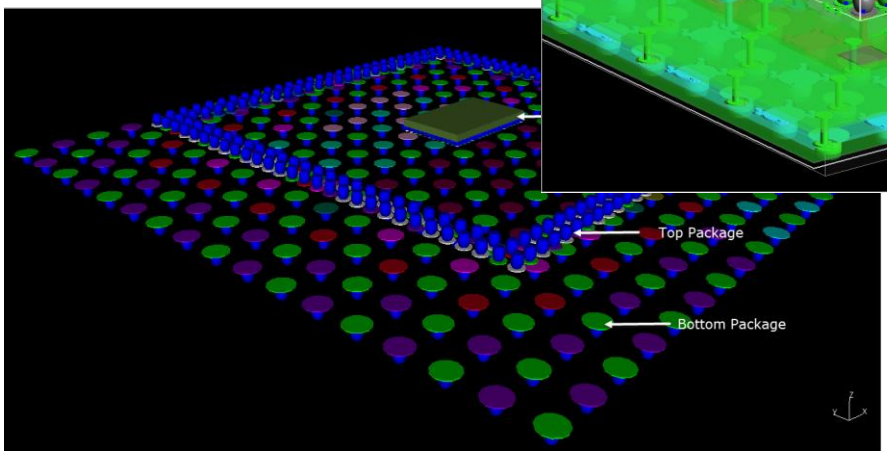
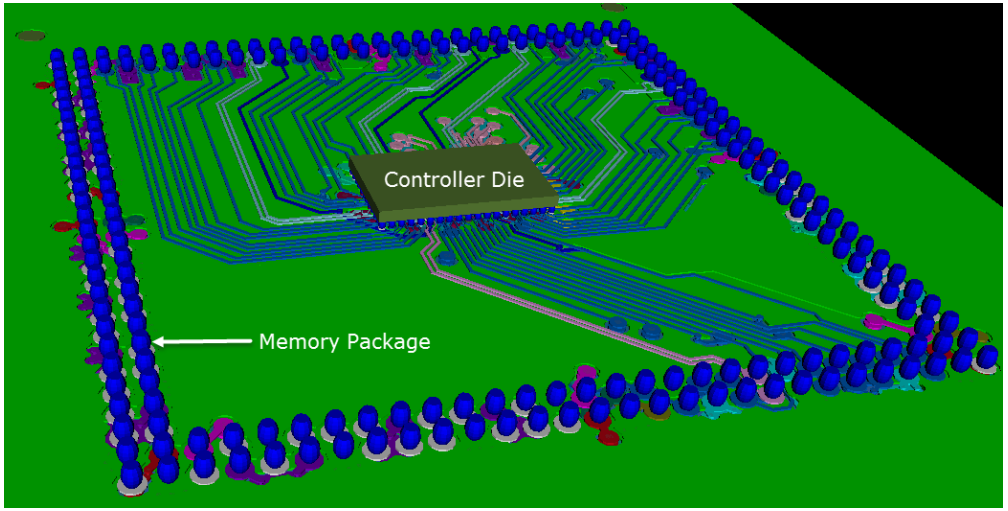
Solution demonstration: An LPDDR4 design

LPDDR4 package-on-package

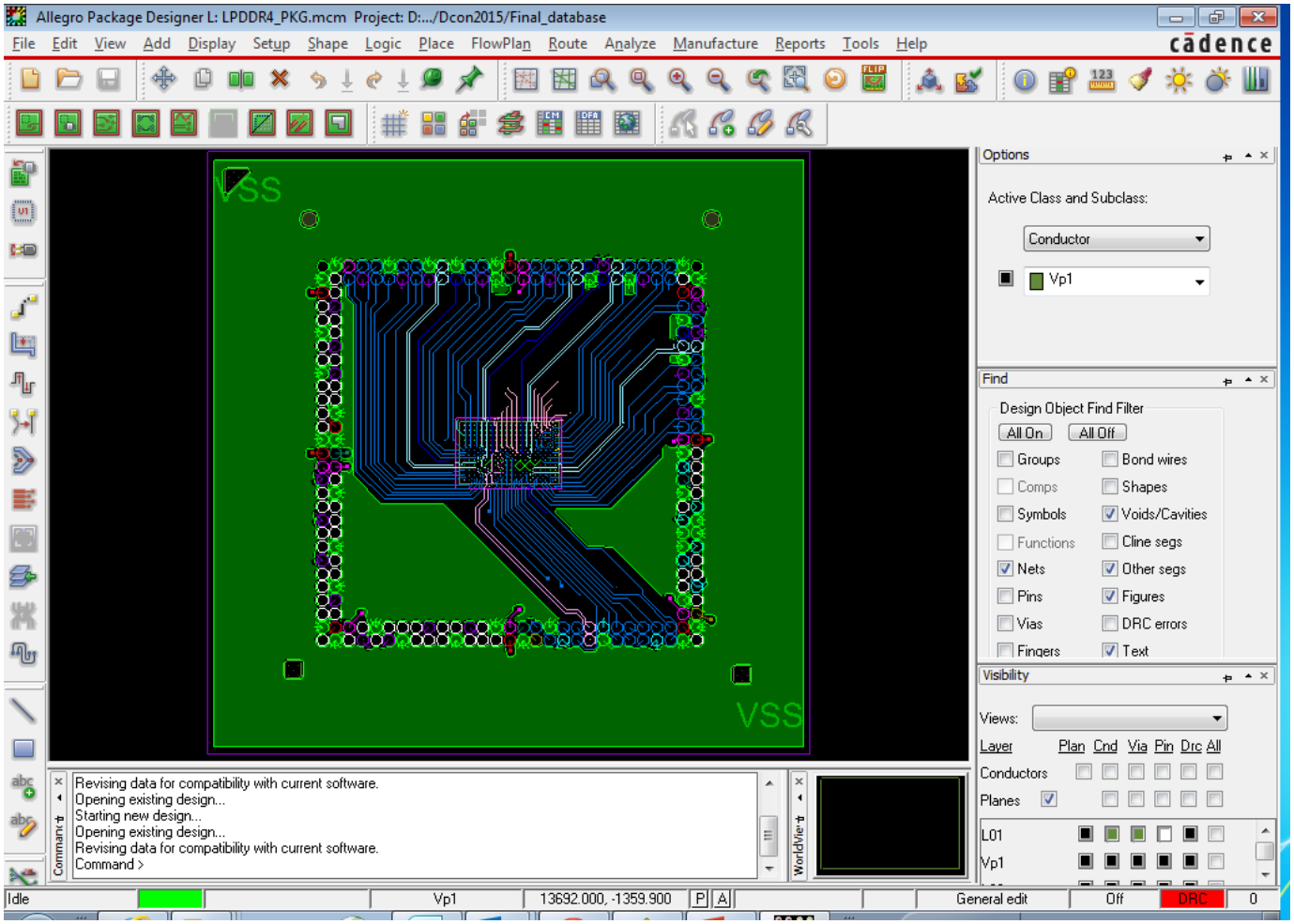
- Low-power parallel designs in mobile applications
  - Controller die
    - 12X12mm BGA
    - Pin count = 216
  - Memory package
    - 12X12mm BGA
    - Pin count = 216
  - Bottom package
    - 18X18mm BGA
    - Pin count = 289
    - 4 layers



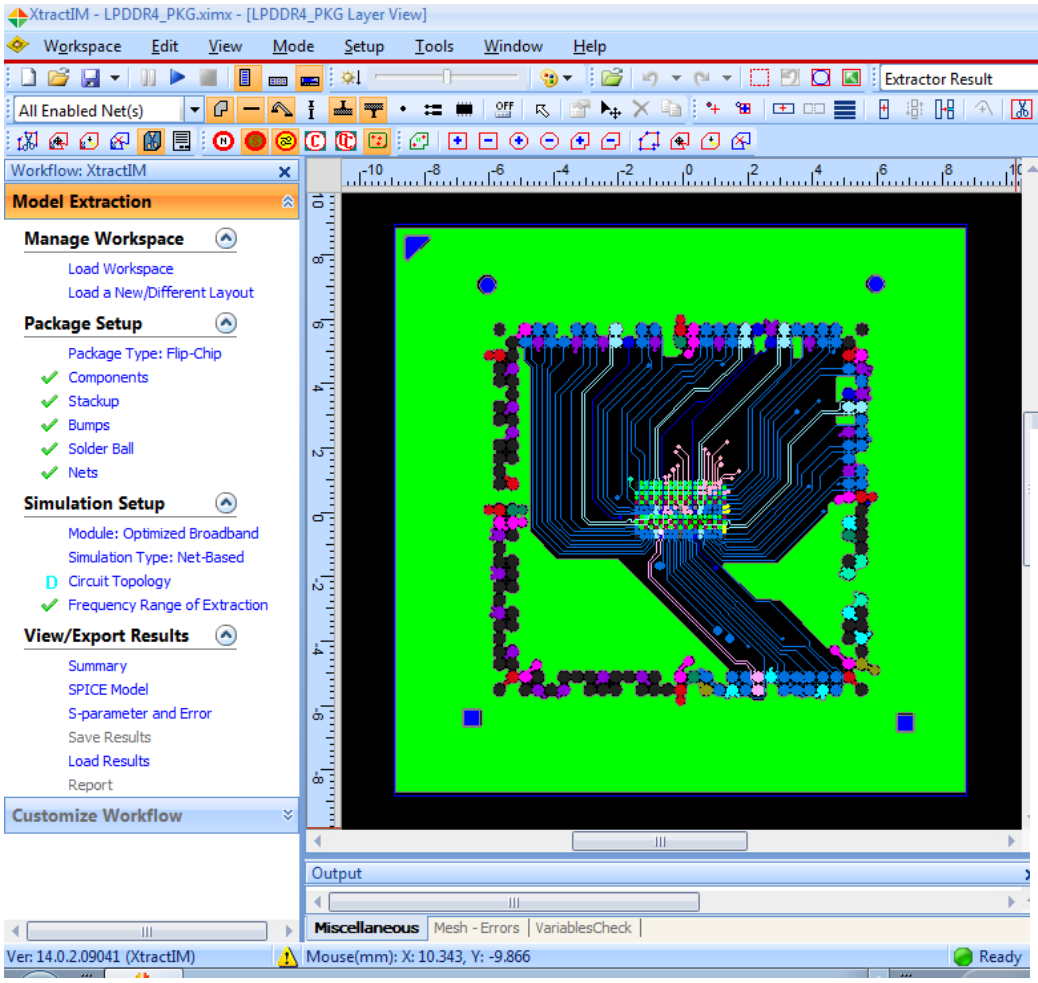




Package design in Allegro Package Designer

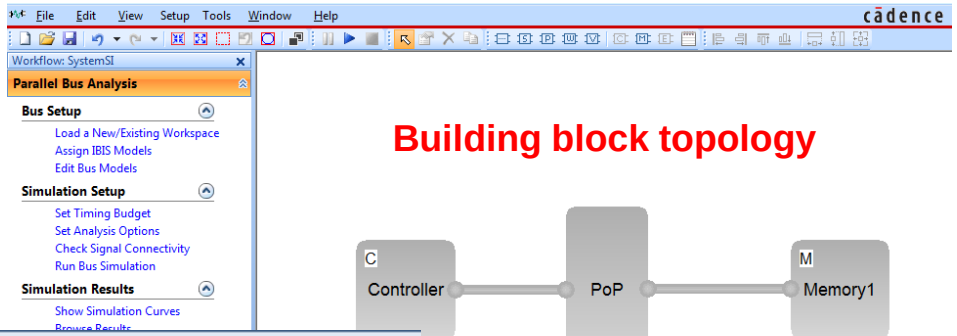


Extracting package interconnects using Sigrity XtractIM technology

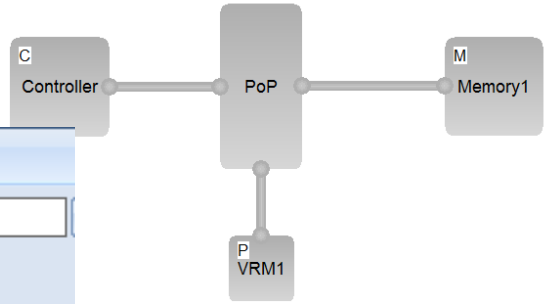



```
.SUBCKT LPDDR4_PKG_LPDDR4_PKG_NetBaseSPICE
+                BGA_C4          BGA1_A15
+                BGA_D5          BGA1_A3
+                BGA_K17         BGA1_AC28
+                BGA_A2          BGA1_A22
+                DIE_C8          BGA1_AB29
+                                    BGA_E6
+                DIE_B2          BGA_H11
+                DIE_L7          BGA_G9
+                DIE_A5          BGA_J6
+                DIE_C1          BGA_G11
+                DIE_A3          BGA_H10
+                DIE_E1          BGA_F10
+                DIE_E3          BGA_E11
+                DIE_F3          BGA_D10
+                DIE_D3          BGA_G13
+                DIE_C2          BGA_F12
+                DIE_C3          BGA_H12
+                DIE_E2          BGA_D12
+                DIE_D2          BGA_G10
+                BGA_P9          BGA1_AH16
+                BGA_K15         BGA1_U28
```

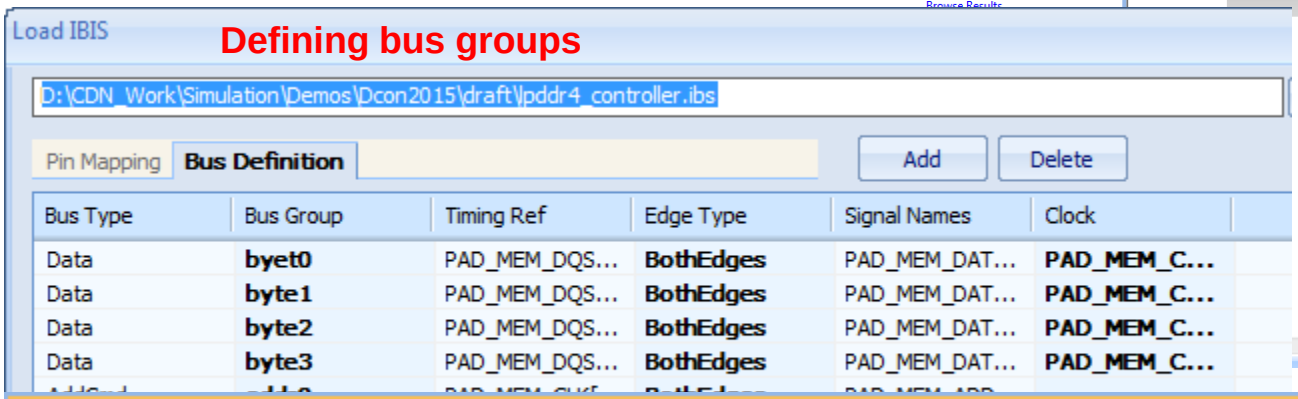
Simulating LPDDR4 design using Sigrity SystemSI technology

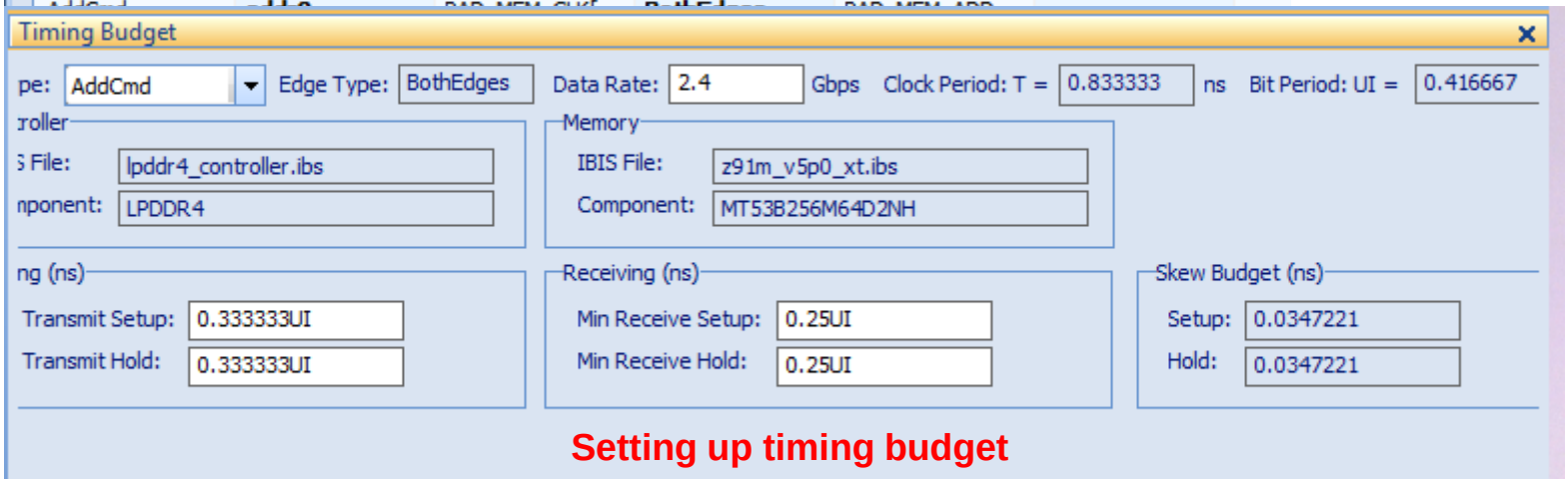


Building block topology



Defining bus groups





Setting up timing budget

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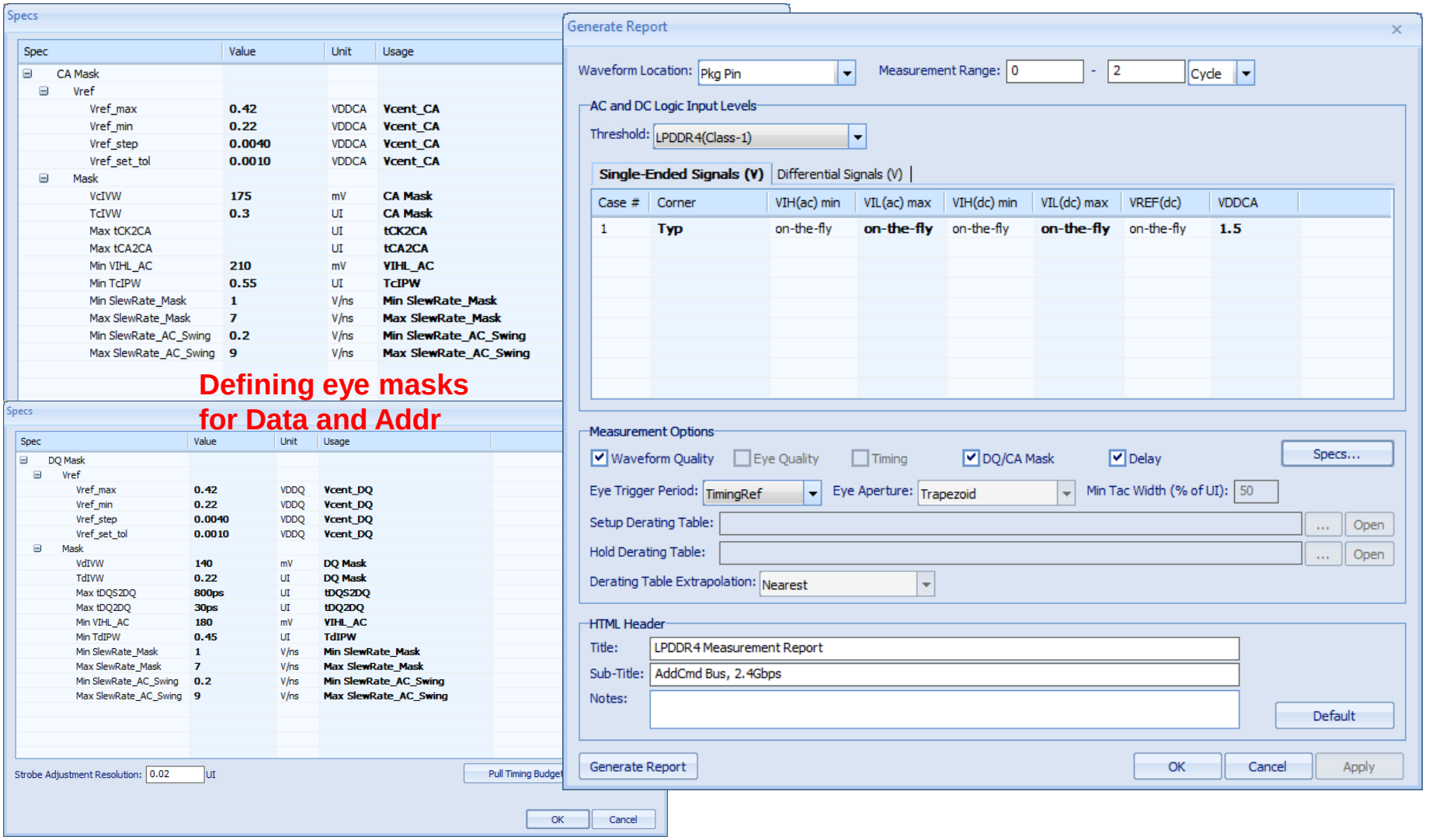
Reporting measurements of a LPDDR4 design using Sigrity SystemSI technology



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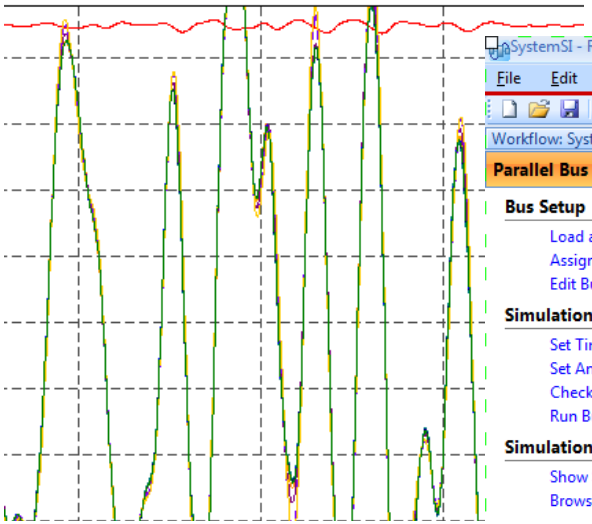
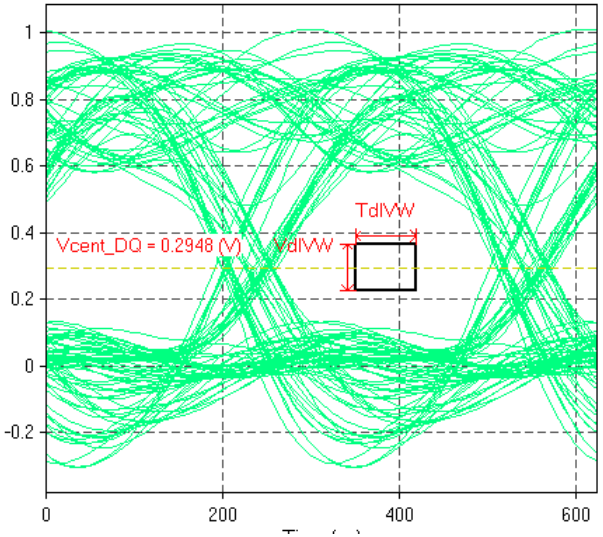
Generating measurement report for timing and signal quality





SystemSI - Report4

File Edit View Setup Tools Window Help

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Workflow: SystemSI

Parallel Bus Analysis

Bus Setup
- Load a New/Existing Workspace
- Assign IBIS Models
- Edit Bus Models

Simulation Setup
- Set Timing Budget
- Set Analysis Options
- Check Signal Connectivity
- Run Bus Simulation

Simulation Results
- Show Simulation Curves
- Browse Results

nent Report
- eport
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- surement Results

Report4

Report4

LPDDR4 Measurement Report

- Data Bus, 3.2Gbps, Write

Generated by Cadence SystemSI, 15.0.a0.01051
January 19, 2015

Useful Links:

- **Cadence website:** http://www.cadence.com
- **LPDDR4 SDRAM Specification:** http://www.jedec.org/standards-documents/docs/jesd209-4

Table of Contents

Data_Write_Typ_Ty
Tx: Controller
Rx: Memory1
Die Pad
Power &

Loaded Curves

Time (ps)

DQ1_D

Measurement Type
Waveform Quality Criteria
Eye Quality Criteria
Timing Criteria
Delay Criteria

e Quality Criter
Timing Criteria
Delay Criteria

SystemSI - PBA II)

Ready

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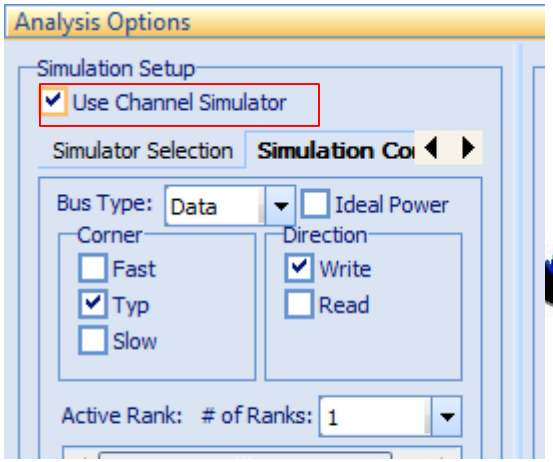
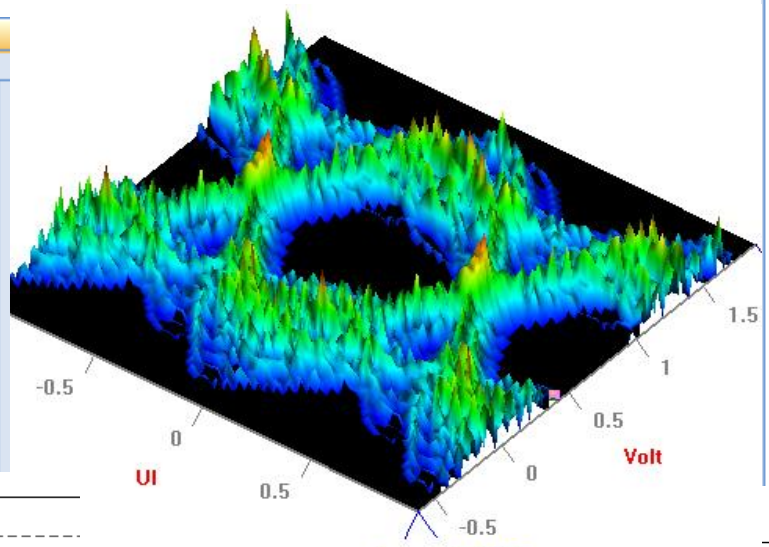
Signal quality reported by simulating the design with channel analysis option



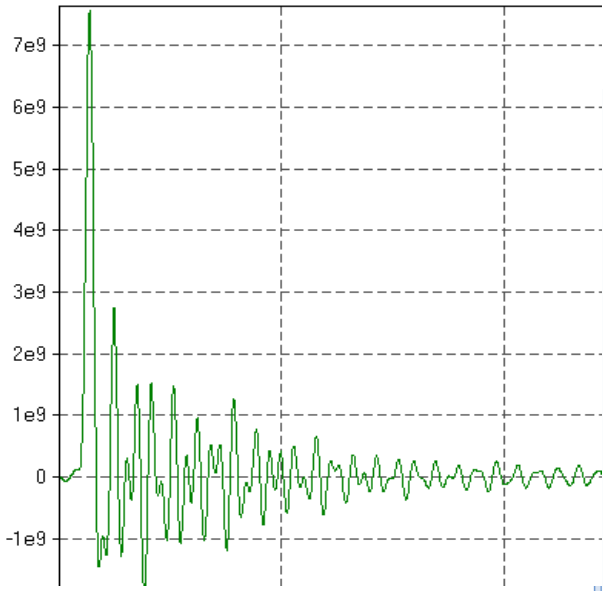


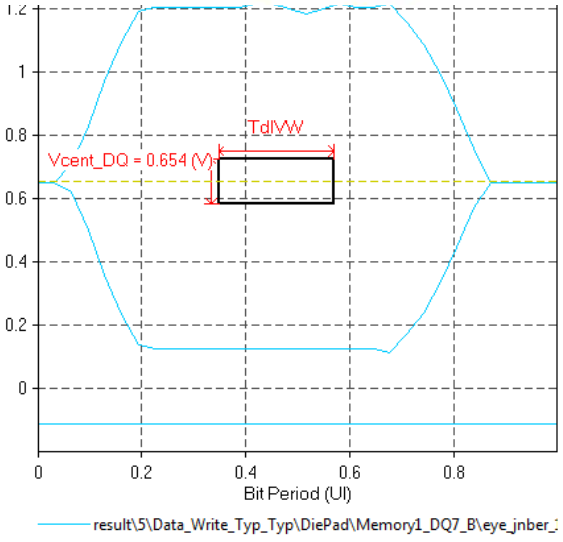

```
                Channel Report

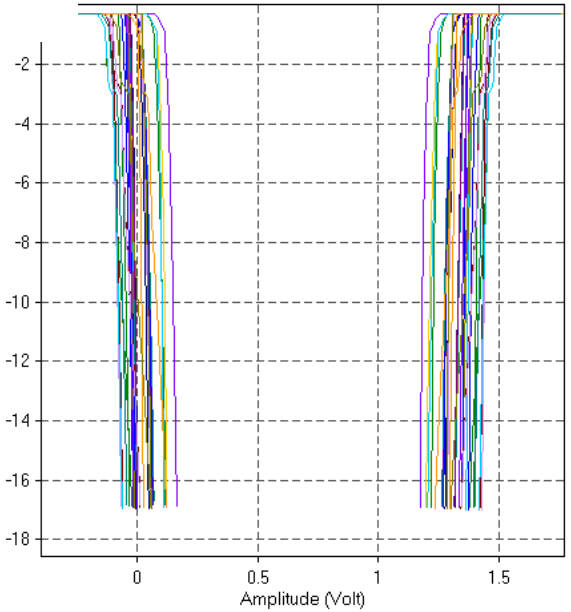
Tue Jan 13 17:02:50 2015

General:

        Data Rate
        Number of Bits
        Ignore Time
        Channel Coding
        Primary Driver
        Data Pattern
        Number of Aggressors
        Characterization Data
```







Case study: Simulation and measurement correlation of a DDR4 design

Topology

T2B

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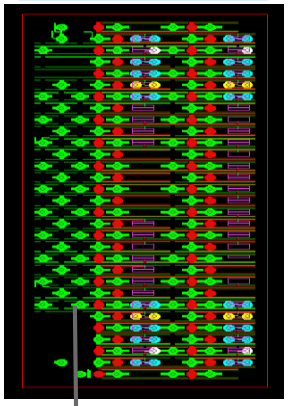
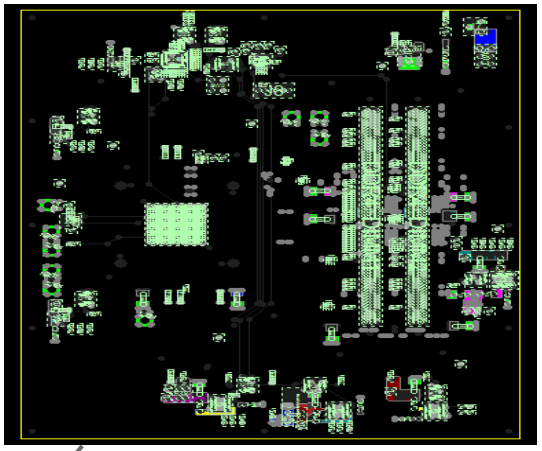
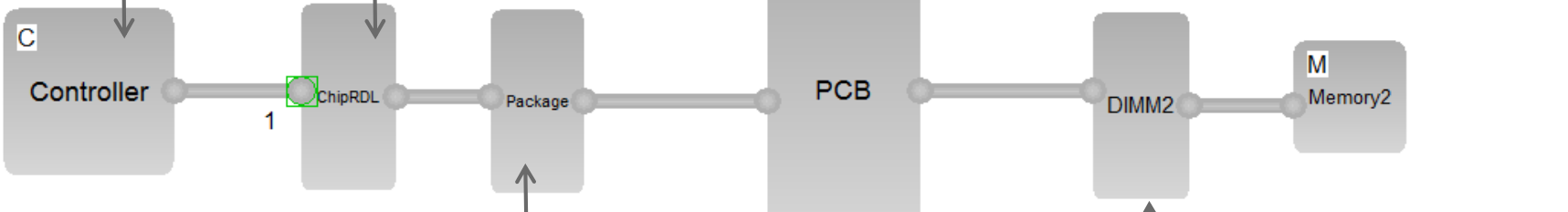
| IBIS file created by T2B Version 12.0.8.0513
| Cadence Design Systems, Inc. 2011
[IBIS ver] 5.0
[File name]  ddr4.ibs
[File Rev]  1.0
[Date]   Thu Sep  5 08:59:40 2013
[Notes] For use with data-rates >= 1.2G the si
[Component] DDR4
[Manufacturer] cadence
[Package]
| variable      typ          min
R_pkg   0.0          0.0
L_pkg   0.0H         0.0H
C_pkg   0.0F         0.0F
[Pin]  signal_name      model_name
1      DQ               ocd
4      power            Power
5      gnd              Gnd
```

XcitePI

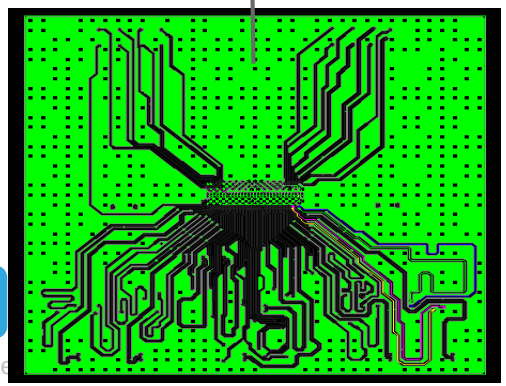


PowerSI

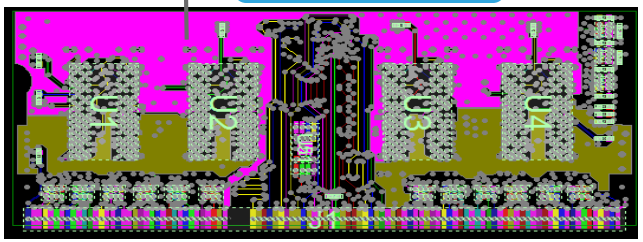




XtractIM

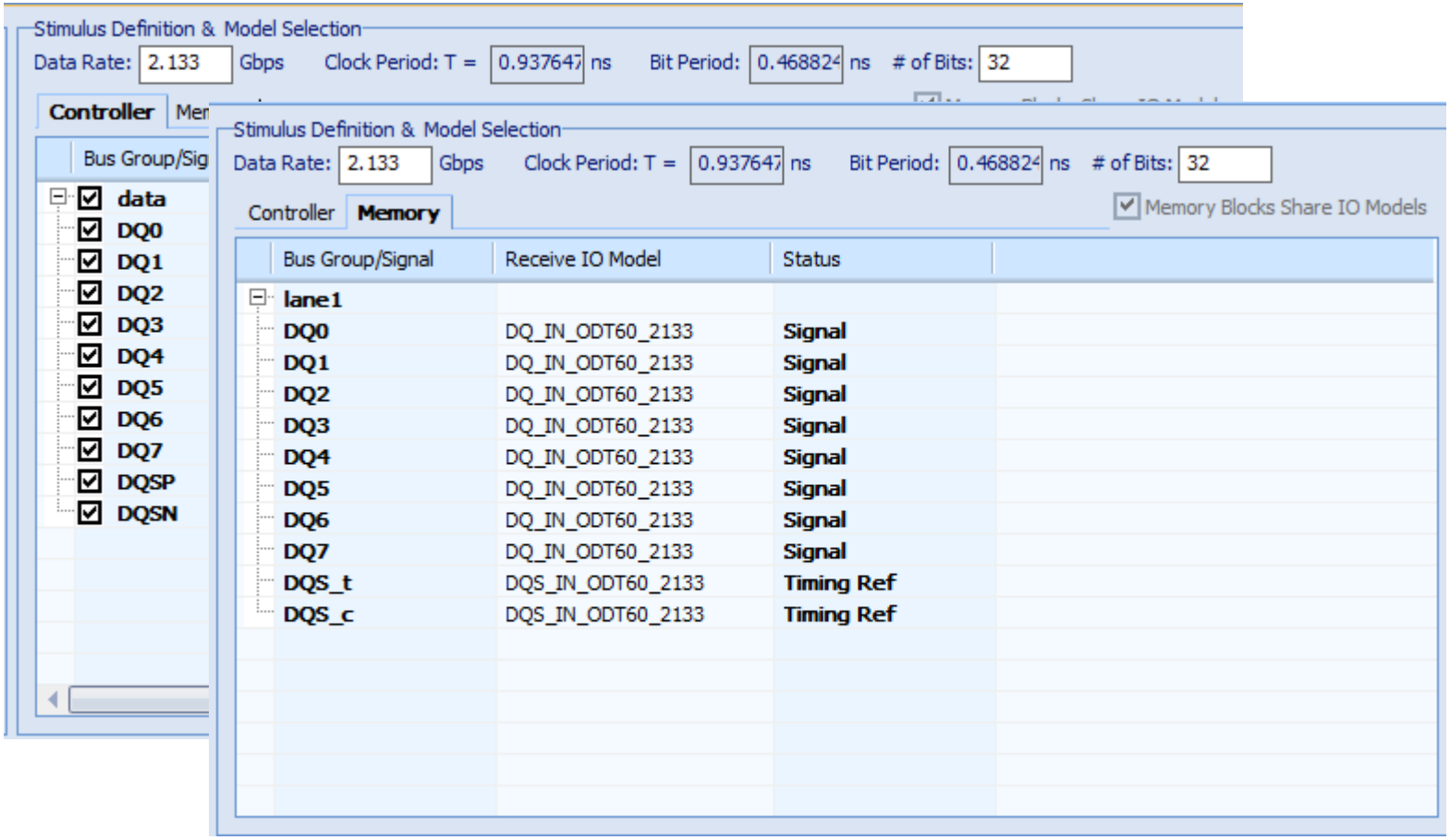


PowerSI

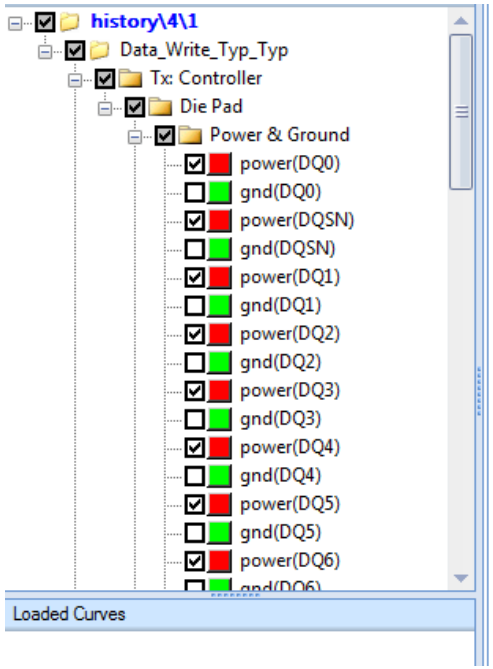


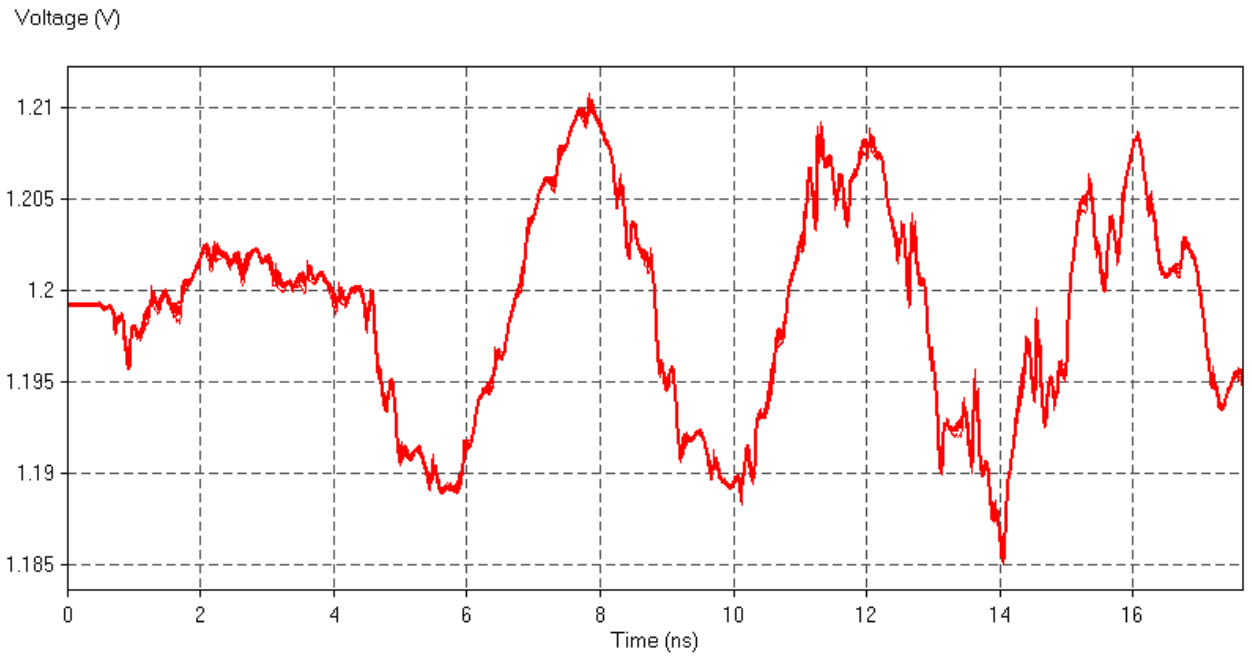
cadence

Stimulus settings

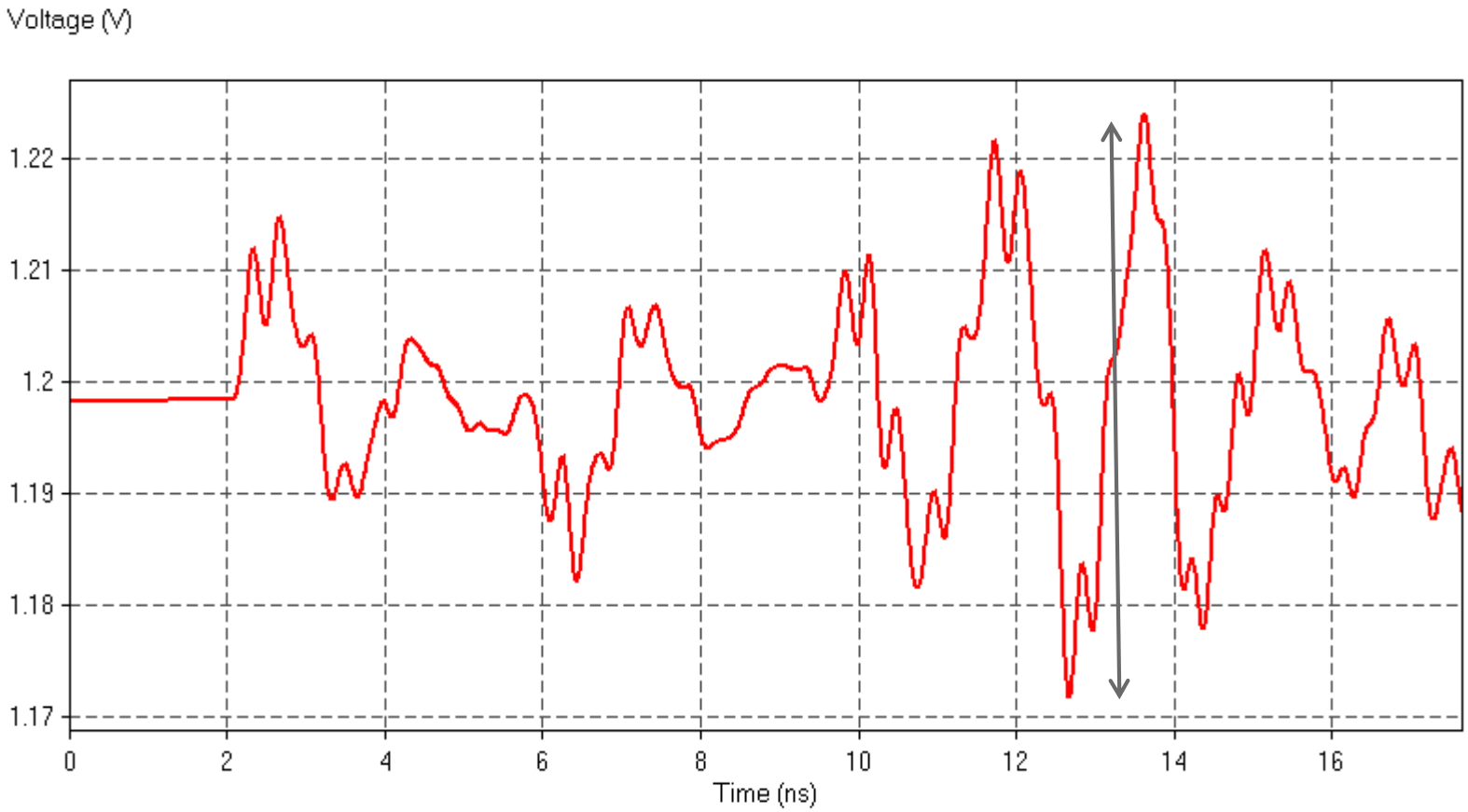


Distributed power network at controller





Power at the memory side (ripple +/- 0.02 V)



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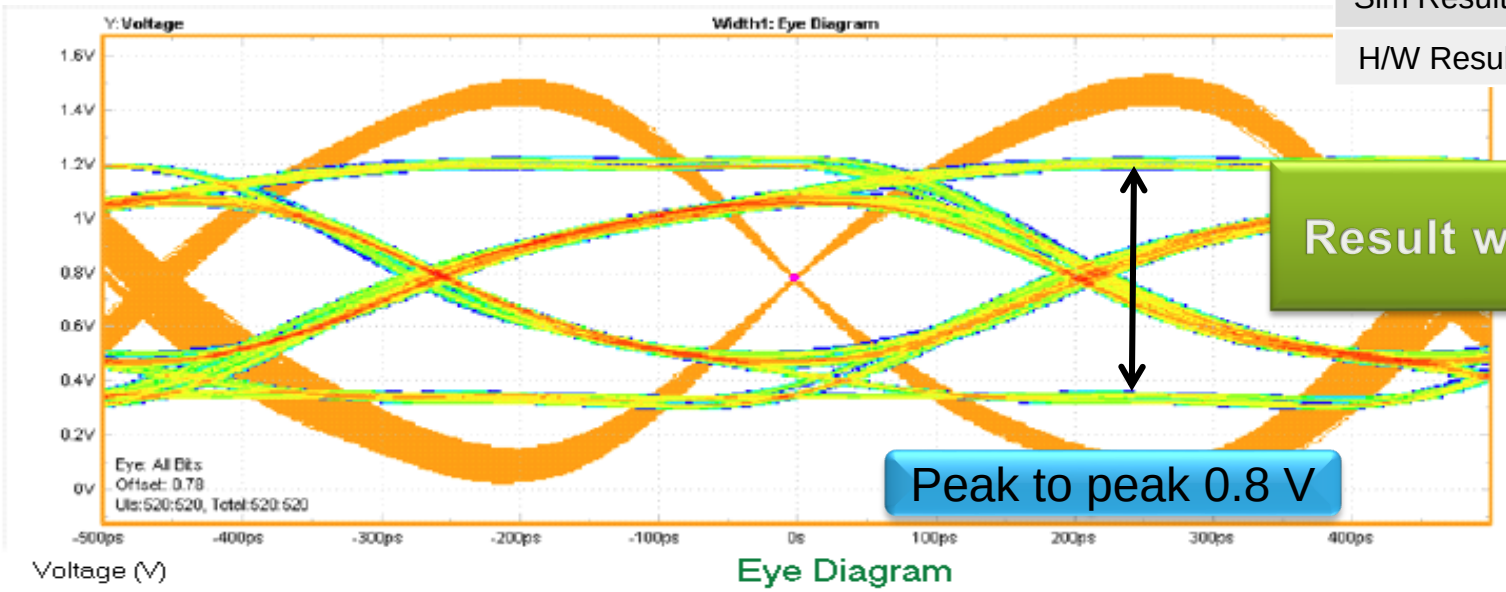
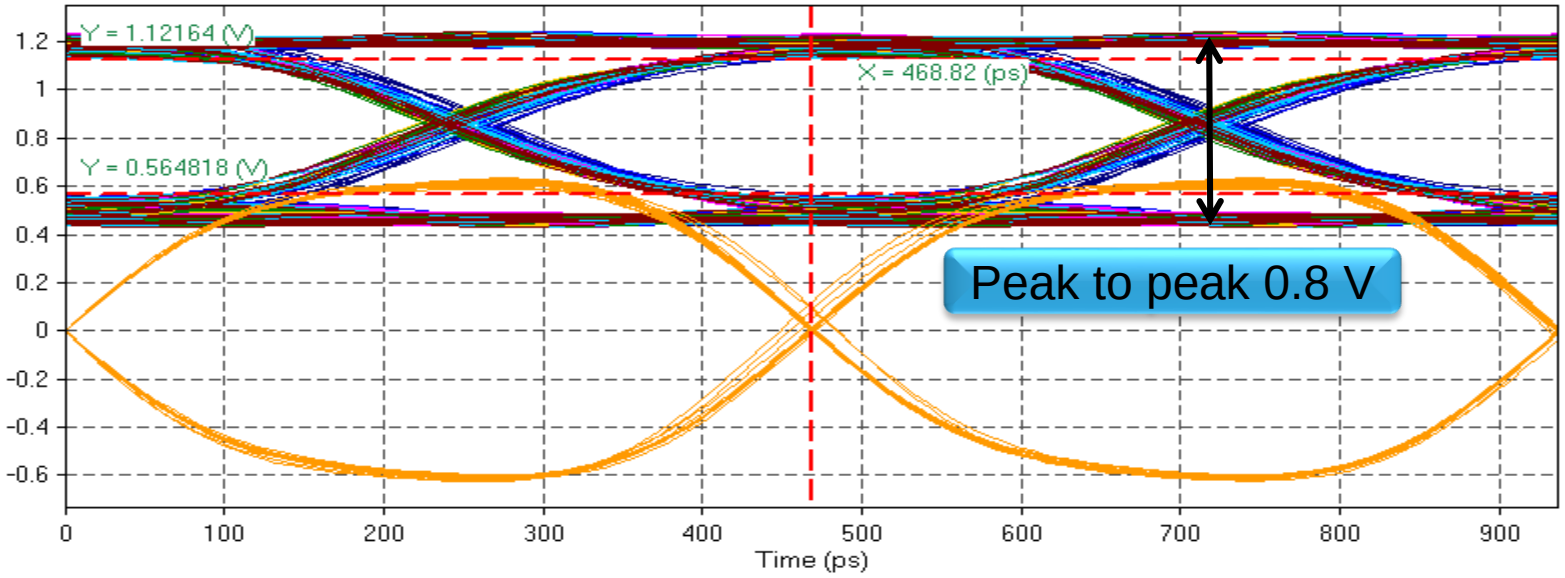
Eye height measurement

Eye Height	Mean
Sim Results	556 mV
H/W Results	526 mV



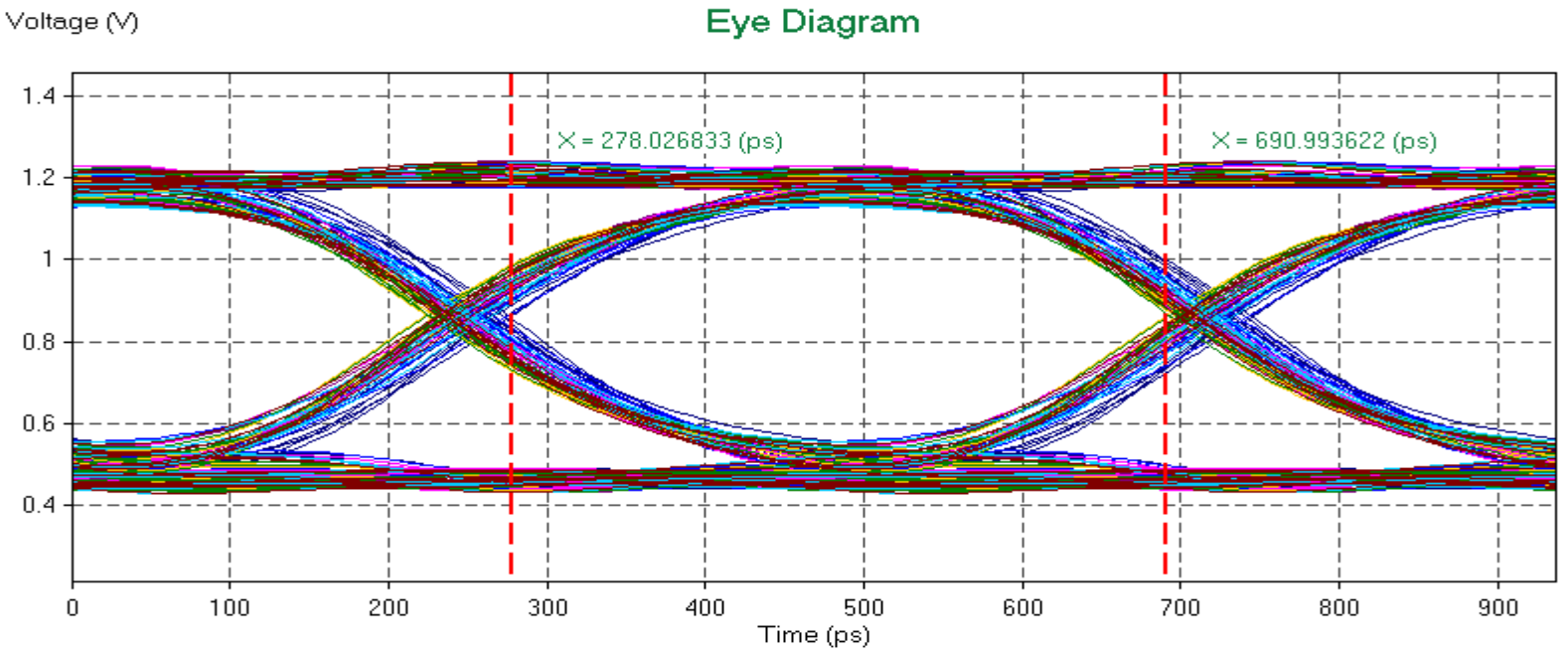


cadence®

Eye width measurement

Eye Width	Mean
Sim Results	412 ps
H/W Results	403 ps

Result within 5 %



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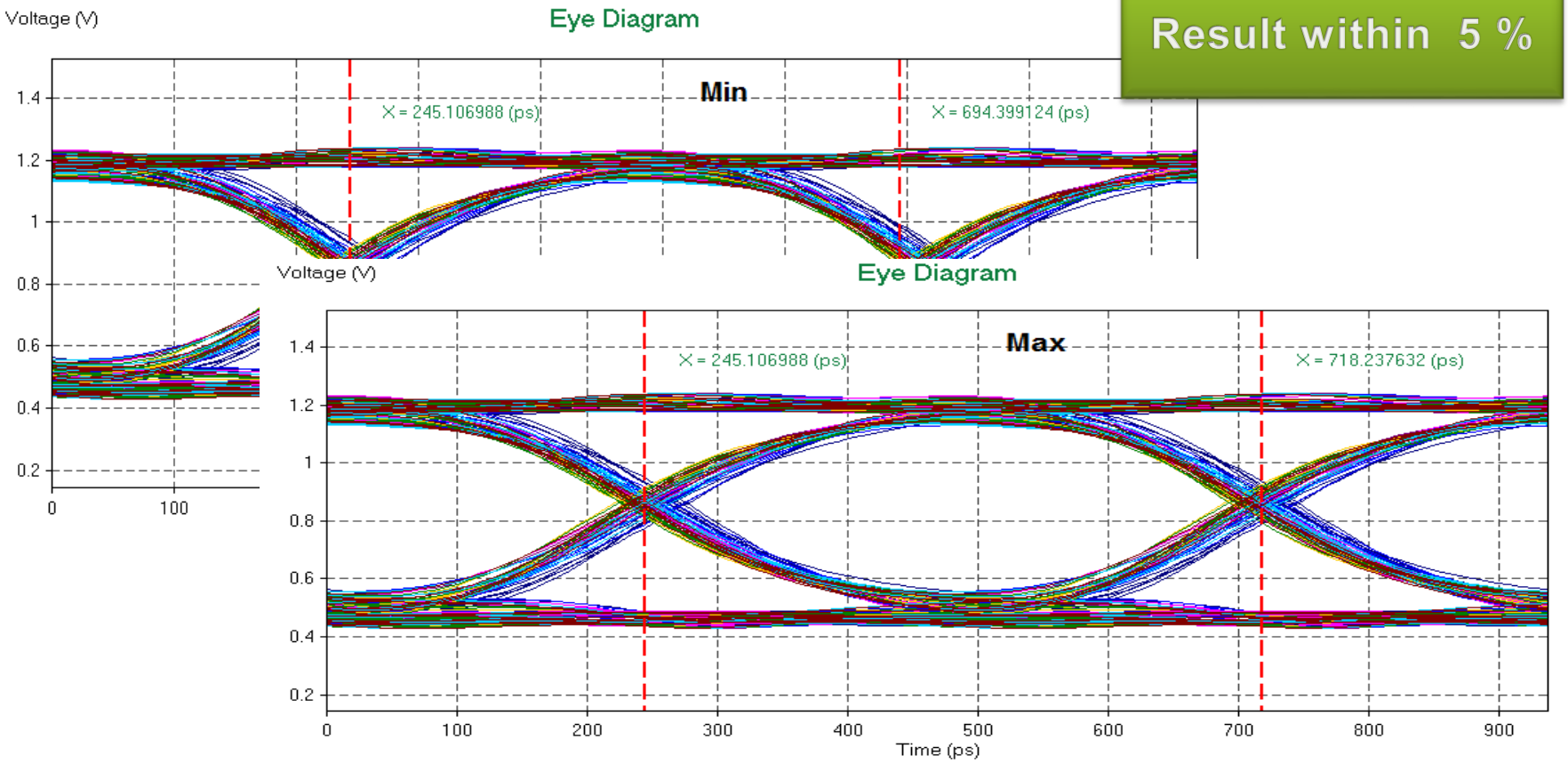
Data tDIPW measurement

tDIPW(DQ)	Mean	Max	Min
Sim Results		473 ps	449 ps
H/W Results	586 ps	-	453 ps

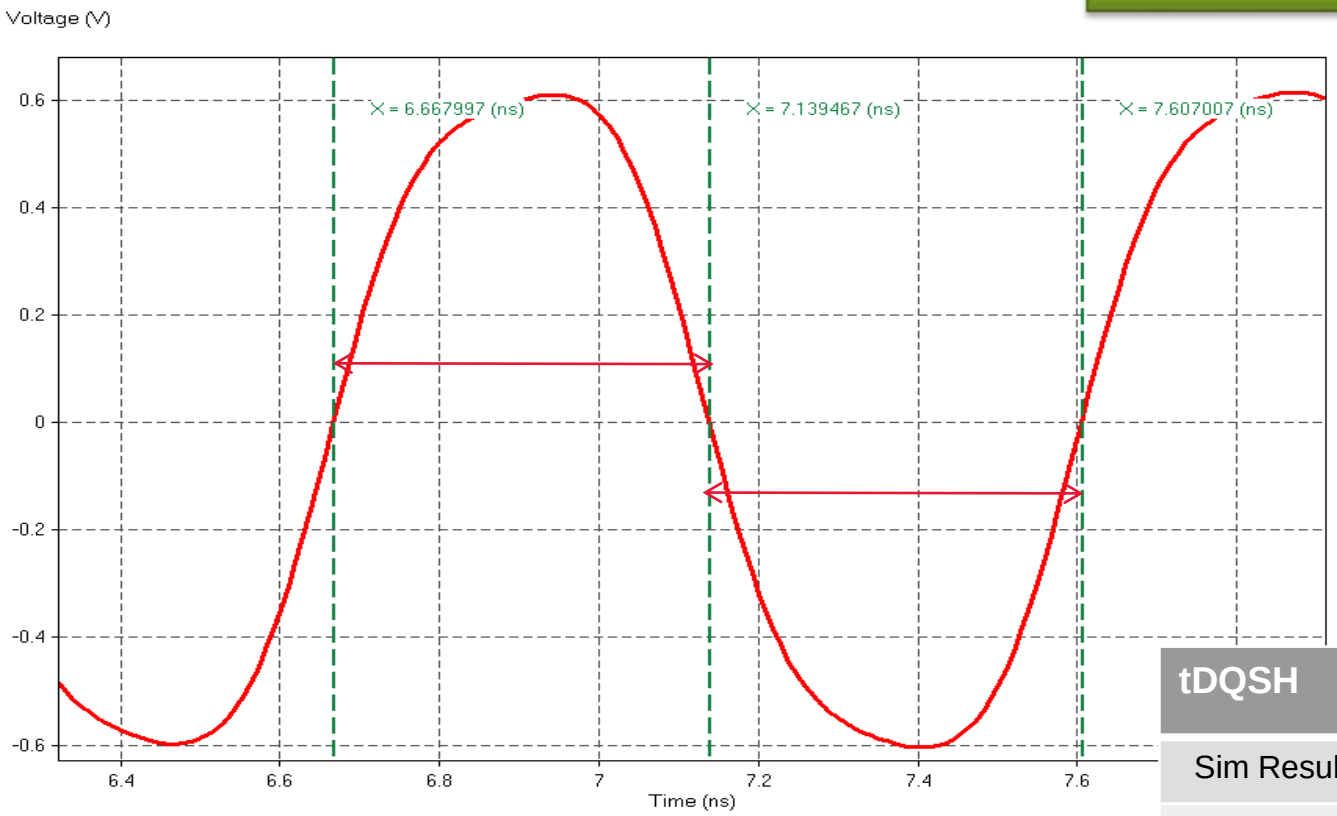
Result within 5 %



Strobe tDQSH/tDQSL measurement

tDQSH	Mean
Sim Results	470 ps
H/W Results	455 ps

Result within 5 %



tDQSH	Mean
Sim Results	468 ps
H/W Results	476 ps

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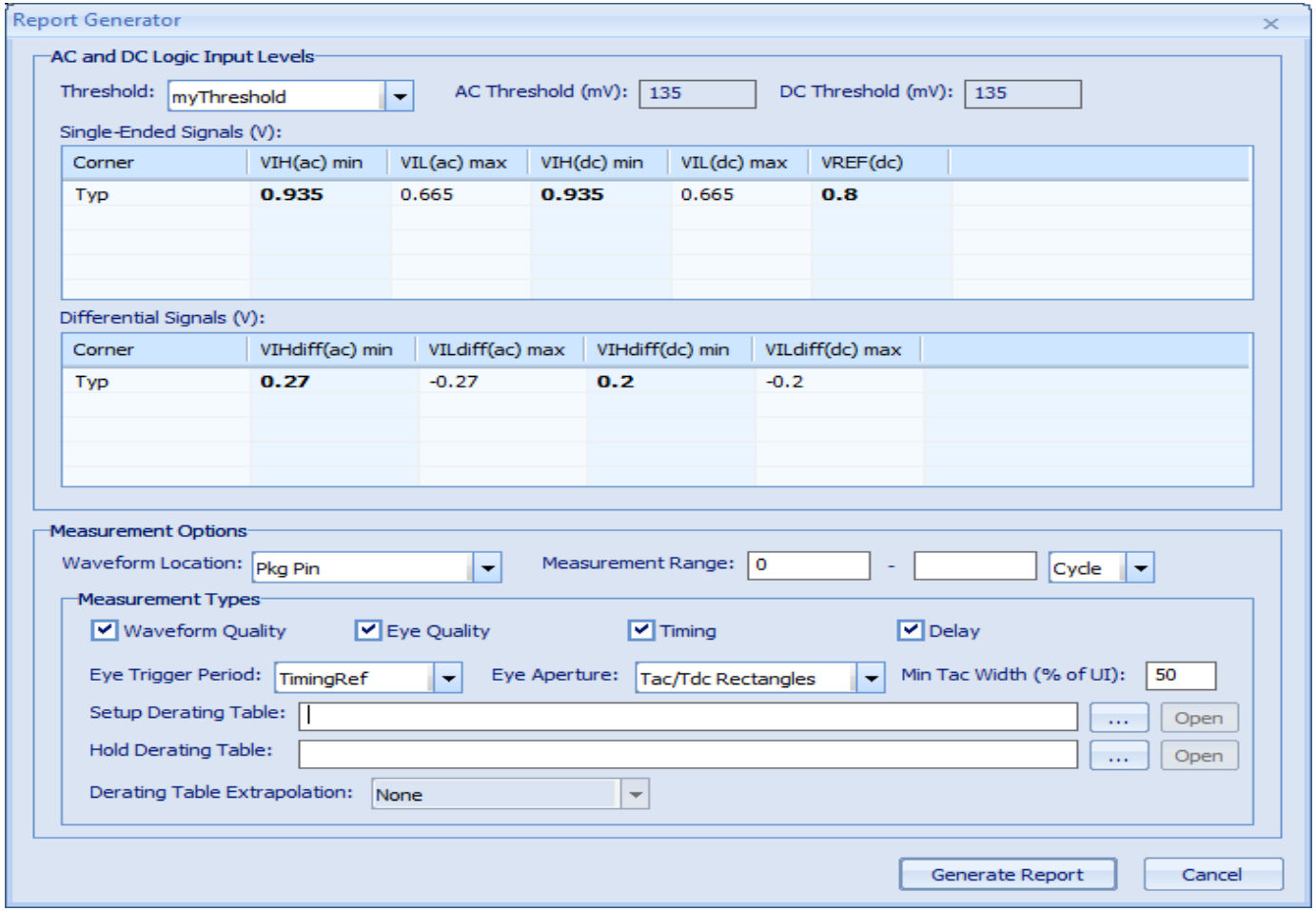
Report generation settings



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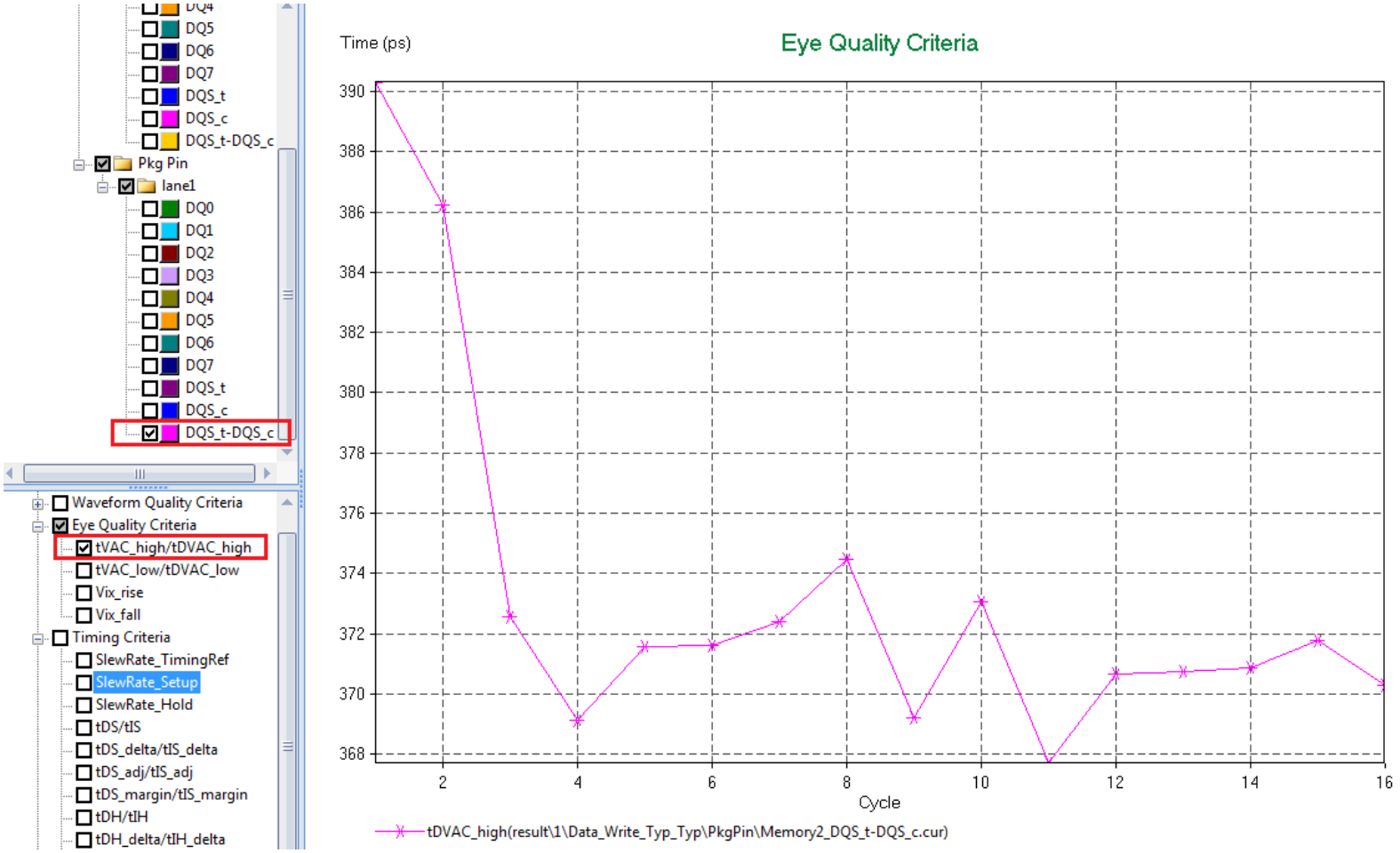
tDVAC variation with cycle of a DQS net



tDVAC Strobe report

tDVAC	Mean	Max	Min
Sim Results		367 ps	360 ps
H/W Results	347 ps	382.7 ps	343.10 ps

Bus Type: Data, Edge Type: BothEdges, Bus Group: lane1, Timing Ref: DQS_t-DQS_c, Measurement Range: [2459.72ps, end]

Rx Signal		Min tVAC_high/tDVAC_high (ps)	Min tVAC_low/tDVAC_low (ps)	Max Vix_rise (n
Eye Diagram	Pin			
DQ0	C2	403.689	293.118	NA
DQ1	B7	401.138	283.602	NA
DQ2	D3	403.334	**278.492**	NA
DQ3	D7	402.287	278.533	NA
DQ4	D2	402.607	290.734	NA
DQ5	D8	**400.973**	287.822	NA
DQ6	E3	402.034	284.53	NA
DQ7	E7	402.854	287.137	NA
All Signals		NA	NA	NA
DQS_t-DQS_c	C3, B3	367.733	360.154	**84.706**

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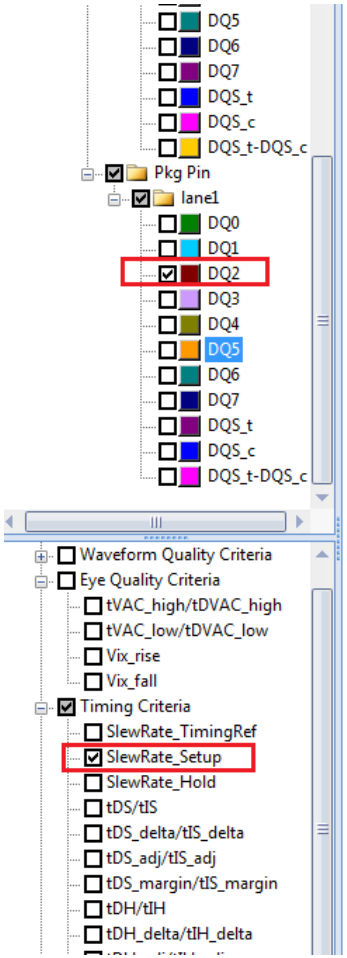
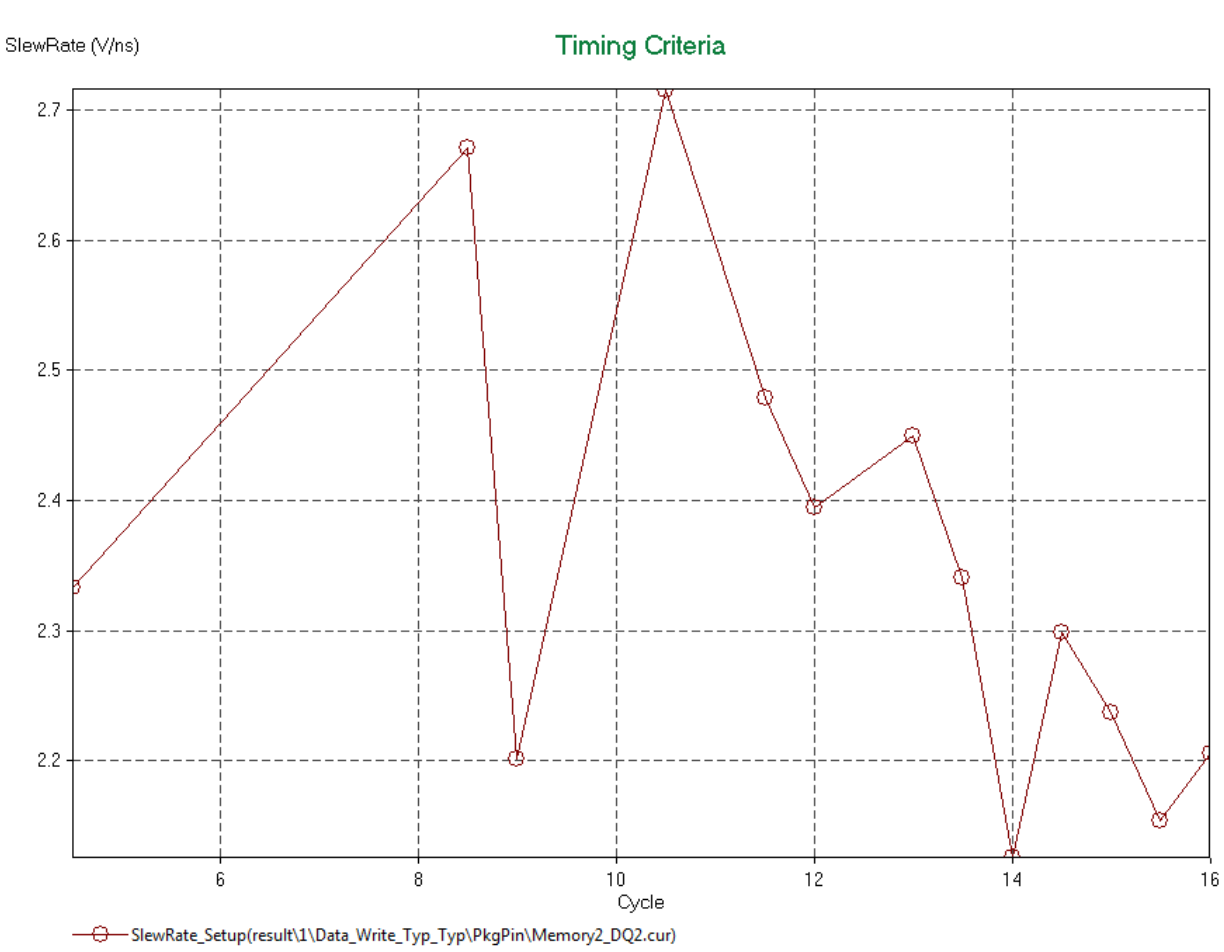
Slew rate variation with cycle of a DQ net





Slew rate report

SRIN_dIVW_Fall	Mean	Max	Min
Sim Results		-3.13 V/ns	-1.96 V/ns
H/W Results	- 2.32 V/ns	-2.81 V/ns	-2.19 V/ns

Bus Type: Data, Edge Type: BothEdges, Bus Group: lane1, Timing Ref: DQS_t-DQS_c, Measurement Rang

Rx Signal		[Min, Max] SlewRate_TimingRef (V/ns)	[Min, Max] SlewRate_Setup (V/ns)	[Min, Max] SlewRate_Hold (V/ns)
Waveform	Pin			
DQ0	C2	[5.40253, 6.20775]	[2.02237, 2.92797]	[2.3287, 3.13065]
DQ1	B7	[5.40253, 6.20775]	[2.06105, 2.83201]	[2.21683, 2.93704]
DQ2	D3	[5.40253, 6.20775]	[2.12613, 2.71579]	[1.96773, 2.86994]
DQ3	D7	[5.40253, 6.20775]	[2.0459, 2.70162]	[2.1333, 2.90077]
DQ4	D2	[5.40253, 6.20775]	[1.97432, 2.88566]	[2.50374, 2.97561]
DQ5	D8	[5.40253, 6.20775]	[1.92858, 2.82142]	[2.46565, 2.91835]
DQ6	E3	[5.40253, 6.20775]	[2.13529, 2.66773]	[2.11598, 2.88237]
DQ7	E7	[5.40253, 6.20775]	[2.19001, 2.71038]	[2.24738, 2.8795]

SRIN_dIVW_Rise	Mean	Max	Min
Sim Results		2.92 V/ns	1.92 V/ns
H/W Results	1.86 V/ns	2.79 V/ns	1.8 V/ns

Summary

Conclusion

- DDR4 and LPDDR4 technologies pose new challenges to parallel bus design and analysis
  - Serial link design methods introduced to the design specification
  - Lower power assumption requires dedicated margin tuning
- Combination of power-aware SI simulation and channel simulation is the only way to support these new technologies
- Cadence Sigrity™ technology provides comprehensive system level SI/PI solutions for core, package, and PCB
  - Unique methodology of power-aware simulation for core and parallel bus system
  - Behavioral model (Chip and core power) generation and simulation
  - Package and board model extraction
  - Integration of patented channel simulation approach in parallel bus analysis flow