Power Integrity in System Design

FLEX Computing

FLEXTRONICS
Design. Build. Ship. Service.

CAE / Design Simulation

Skipper Liang

5/20/2008

Agenda

- Introduction
- Power Integrity Concept
- DC Analysis for Power Integrity
- AC Analysis for Power Integrity
  1. Observe from Frequency Domain
  2. Observe from Time Domain
- Summary
- Q & A

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Introduction

Desktop | Notebook | Server | Server Link Card | Enterprise Storage

Design. Build. Ship. Service.

~Flextronics International Ltd (NASDAQ: FLEX) is the world No.1 EMS provider from yr2001 to yr2004.

~Flextronics began its design service at the end of yr2006.

~Numbers of Sigrity Tool Sets help us to increase our customer's competitiveness

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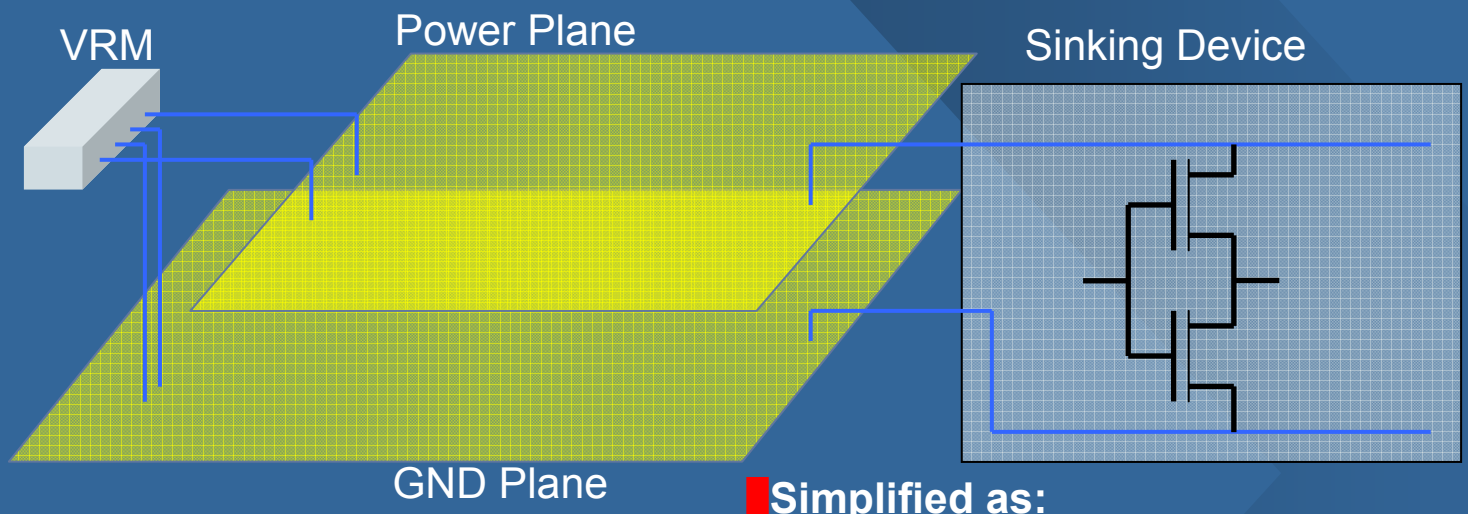
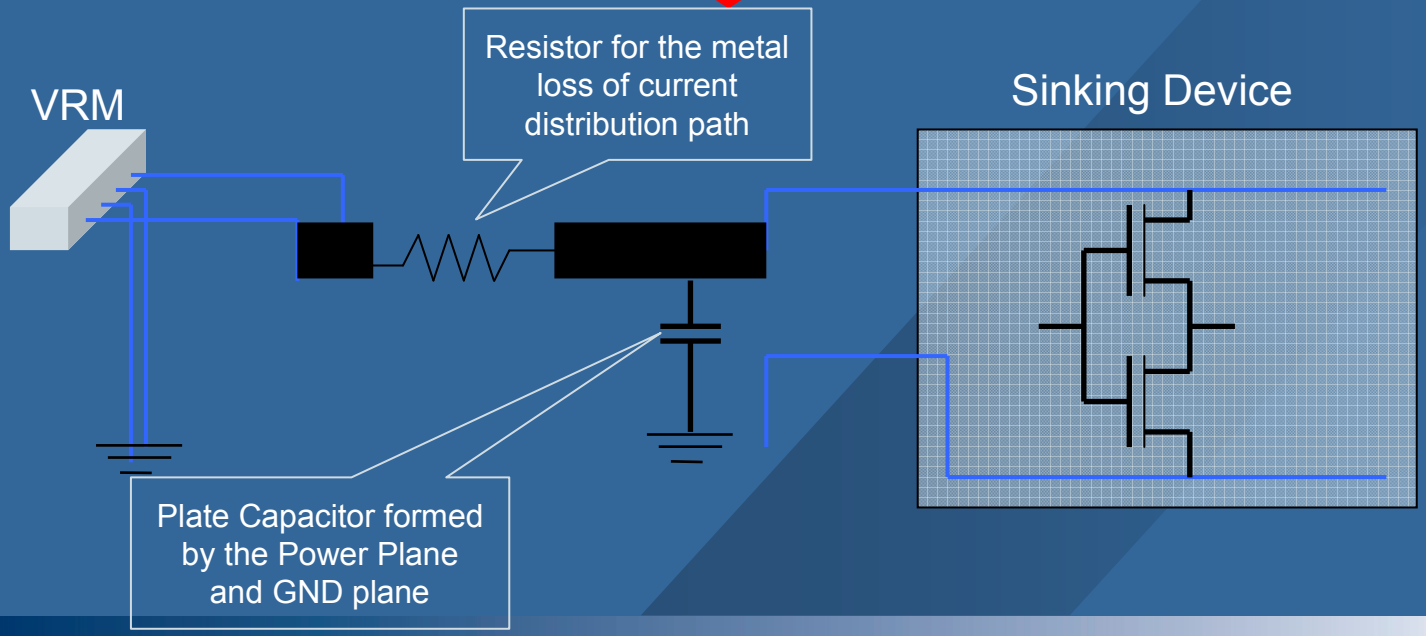
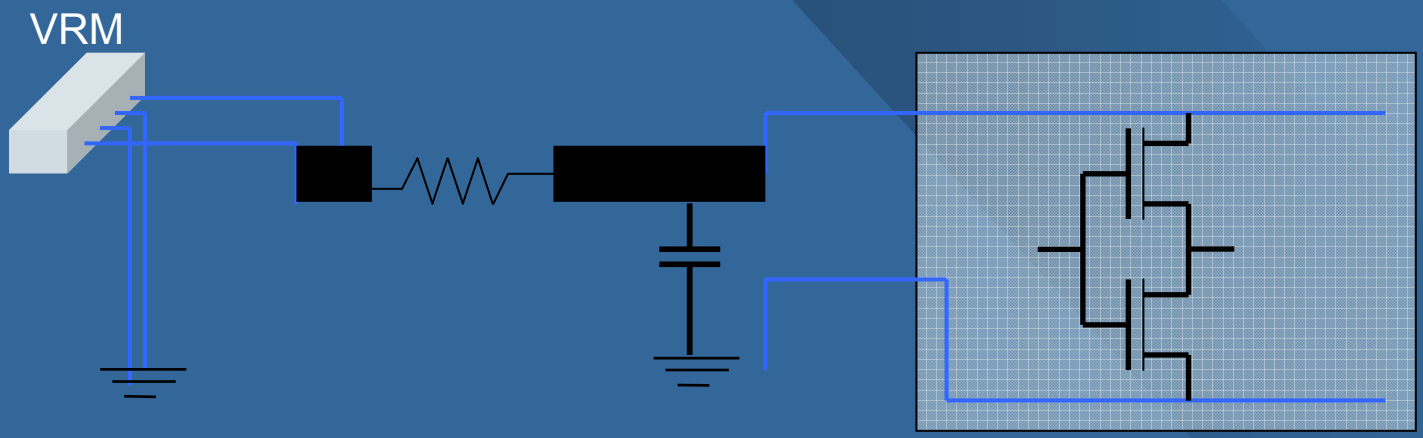
Power Integrity Concept



Simplified as:

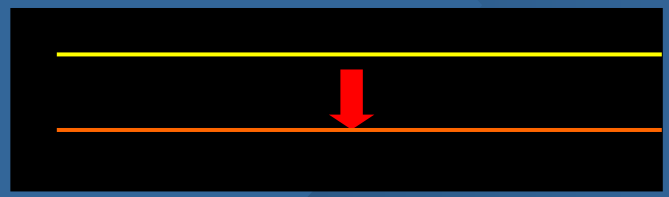


Power Integrity Concept



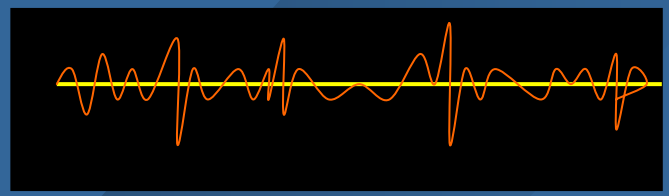
Cause the Voltage level shifted from the ideal level

We need **DC Analysis**.

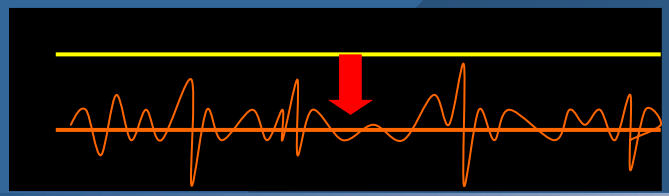


Cause the Voltage level variation from the ideal level during the current transient

We need **AC Analysis**.

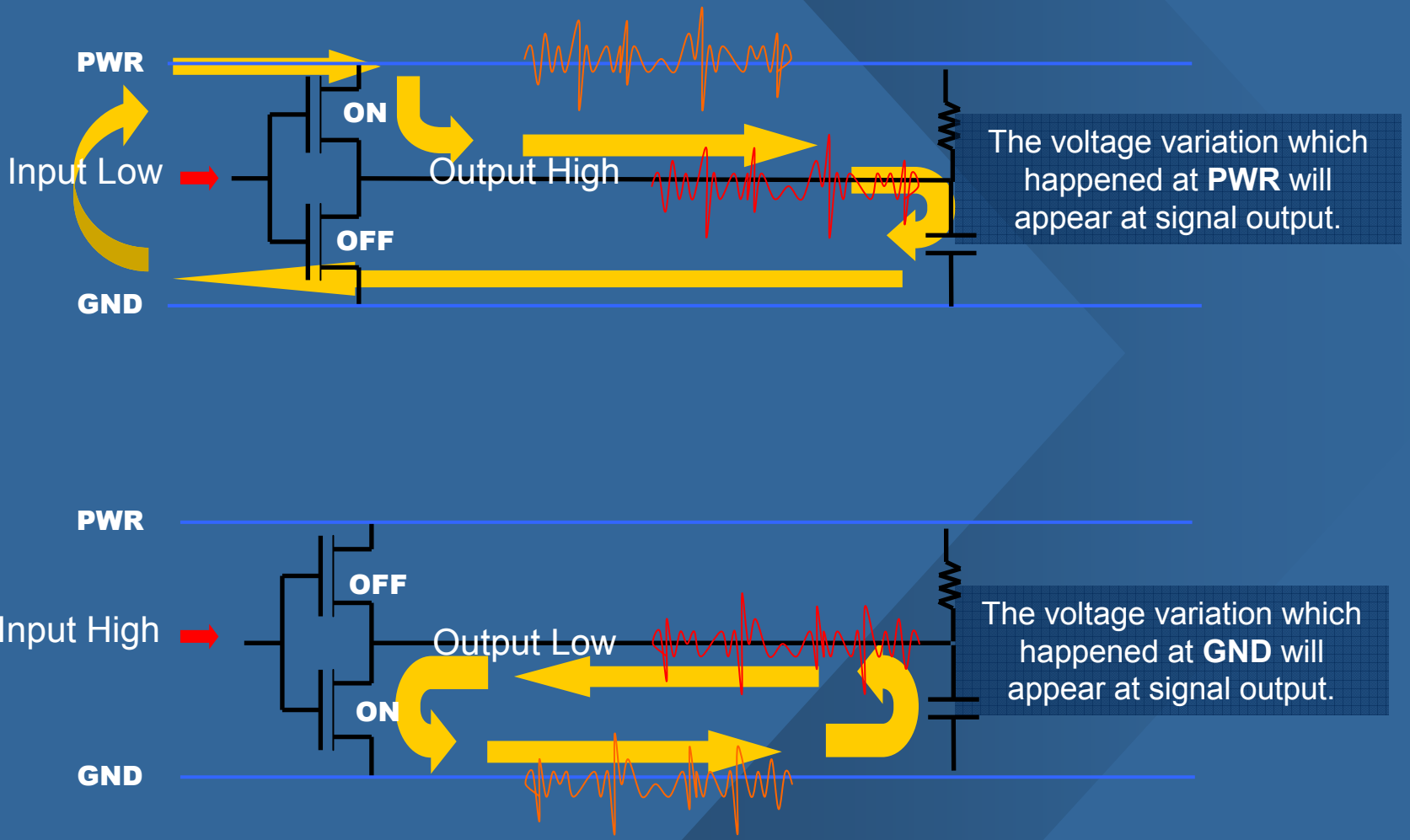


Total Effect



Power Integrity Concept

Effect to Signal Integrity (Besides the coupling between planes and Traces):



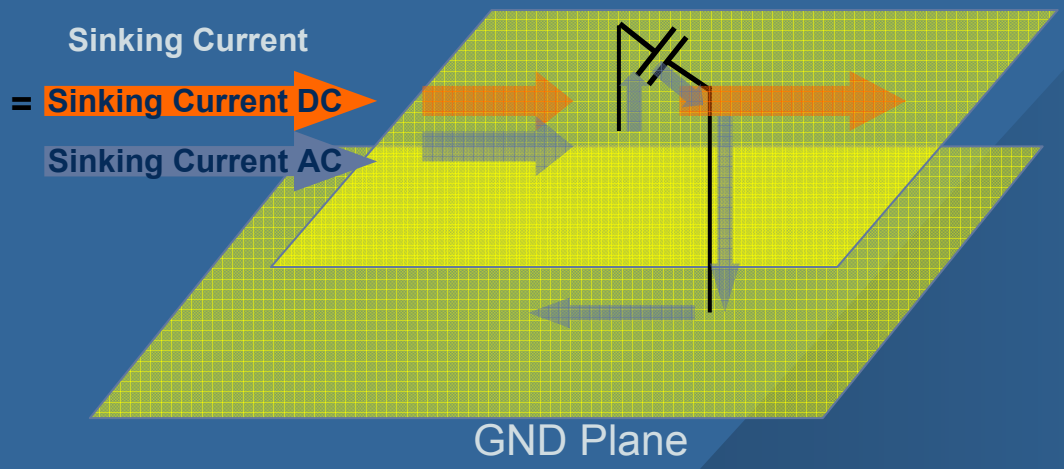
Power Integrity Concept

How to lowering the impedance contributed by power/ground plane pair?

Capacitor Parallel Connected (De-Coupling Capacitor)

$$Z(f)//(\frac{1}{j2\pi fC}) = \frac{Z(f)}{j2\pi fC \cdot Z(f)+1}$$

This can be viewed as:



A Capacitor will be treated as a short path by the AC part.

A Capacitor will be treated as an open path by the DC part.

Power Integrity Concept

If the analysis result is fail, how's the impact?

DC Analysis	AC Analysis
1. Add Layers 2. Add trace Width 3. Location of VRM and Sense 4. VIA numbers and location → Change the geometry of the Power Distribution System	1. Add Capacitors → Modify the Schematics → Modify the location of capacitors 2. Modify the layers: i. Floor planning ii. Shape geometry → Change the geometry of the Power Distribution System

To speed up the design procedure and reduce the frequency of modifying the PDS's geometry, we will frozen the PDS's geometry after the DC Analysis and simply modify the capacitor's size, number and location of capacitors, that is:

DC Analysis → Change the geometry of the Power Distribution System → AC Analysis → Modify the Schematics, Modify the location of capacitors

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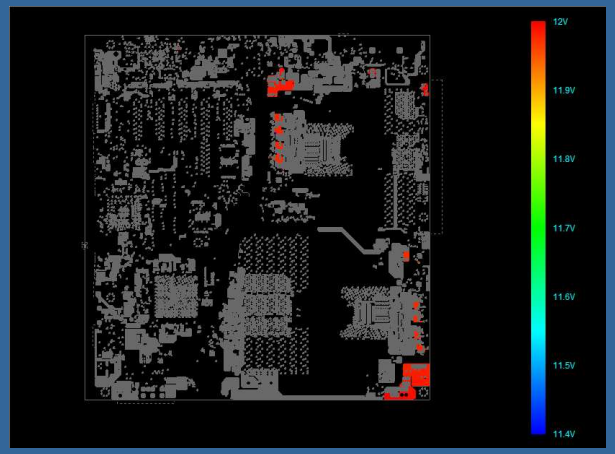
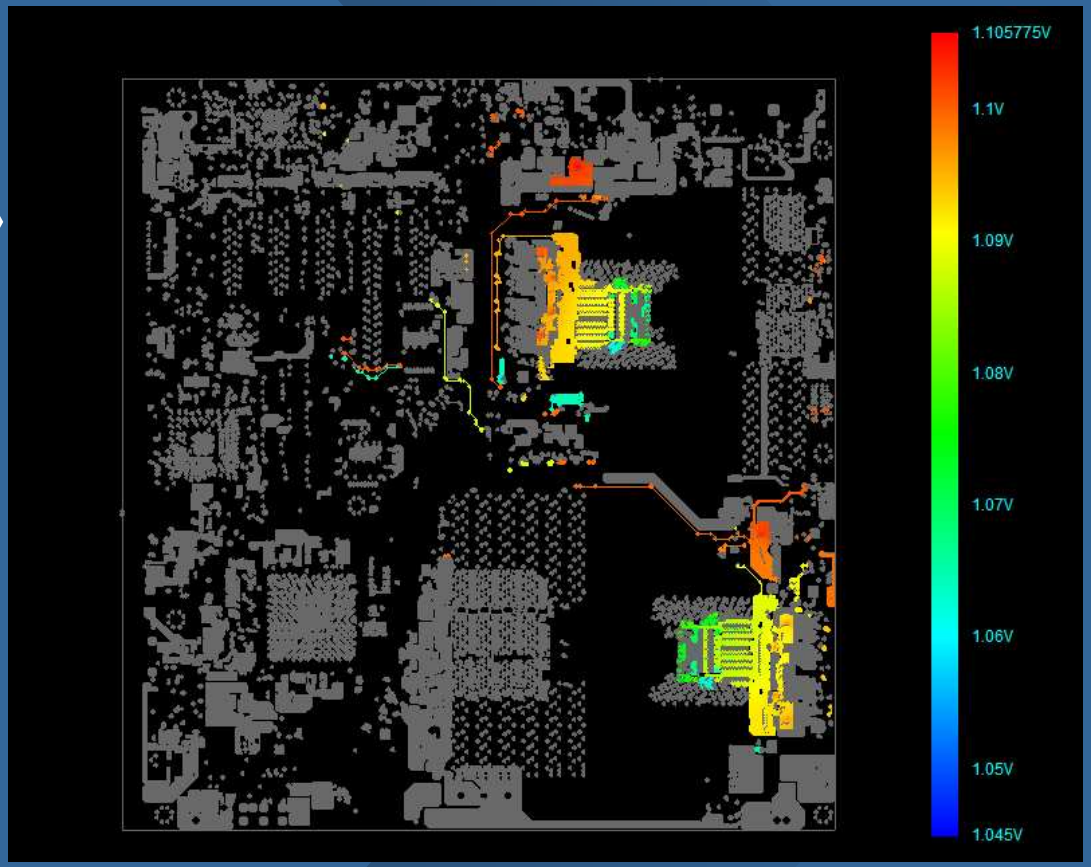
DC Analysis for Power Integrity

Voltage Drop:





i. Power DC helps us to track down the voltage distribution along the Power Delivery Path.

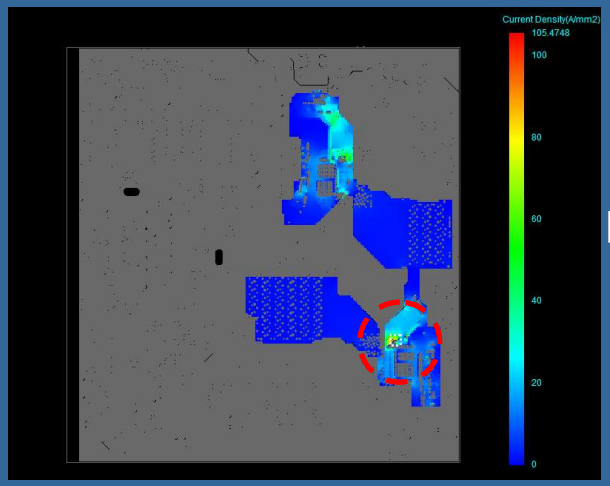
ii. Power DC helps us to generate clear table to judge the simulation result Pass or Fail.

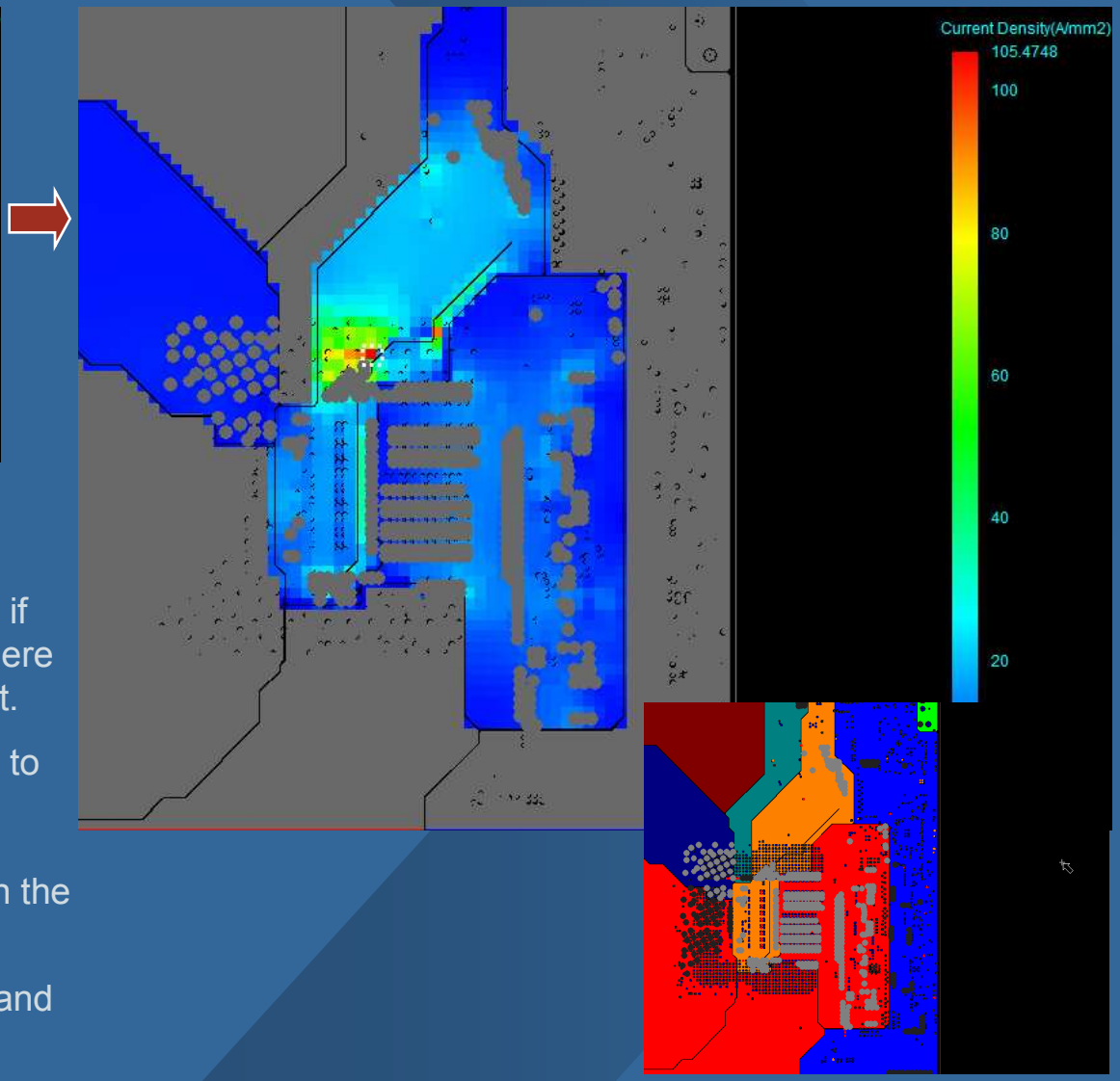
iii. The whole procedure is easy and fast.

Sink Name	Model	Nominal Voltage (V)	Input Tolerance (%)	Actual Voltage (V)	Margin (V)
SINK_U15_PV_VCCP_CPU0_GND	Equal Current	1.100000e+000	5.000000e+000	1.066218e+000 ✓	2.121827e-002
SINK_U16_PV_VCCP_CPU1_GND	Equal Current	1.100000e+000	5.000000e+000	1.068928e+000 ✓	2.392785e-002
SINK_U15_PV_VTT_CPU0_GND	Equal Current	1.100000e+000	5.000000e+000	1.049691e+000 ✓	4.690785e-003
SINK_U16_PV_VTT_CPU1_GND	Equal Current	1.100000e+000	5.000000e+000	1.047043e+000 ✓	2.042829e-003

DC Analysis for Power Integrity

Current Density:





i. Power DC helps us to find out if there's any critical location where exist a large amount of current.

ii. By the capability of Power DC to analyze the current density distribution, we can find out if there's any redundant moat on the plane.

iii. The whole procedure is easy and fast.

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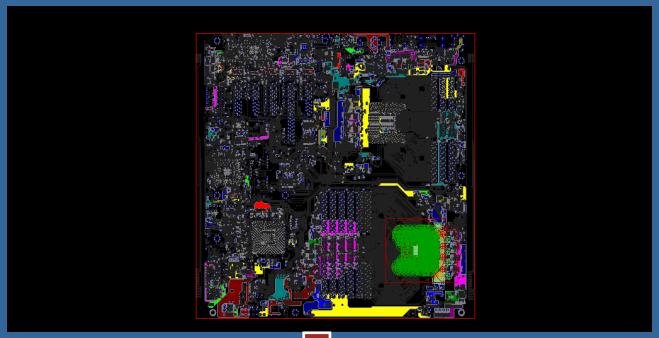
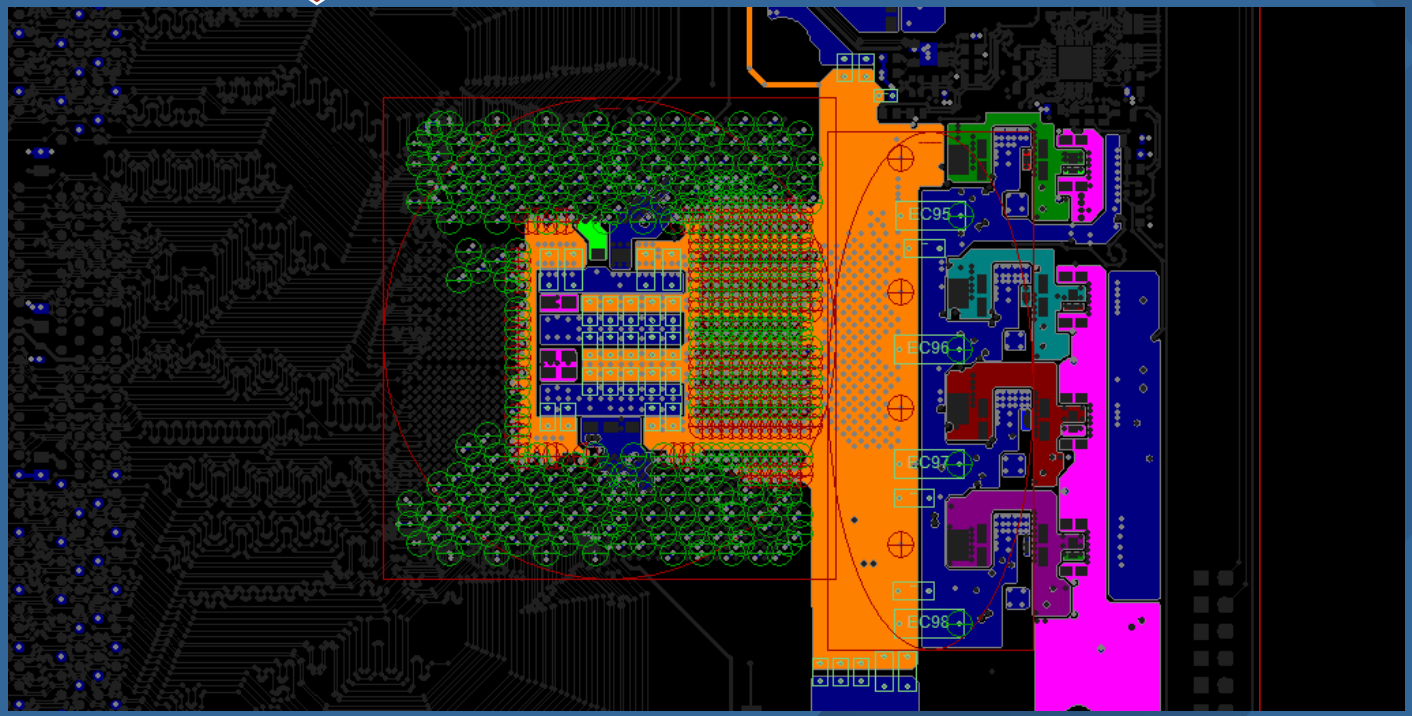
Observe from frequency domain

Impedance Plot File:



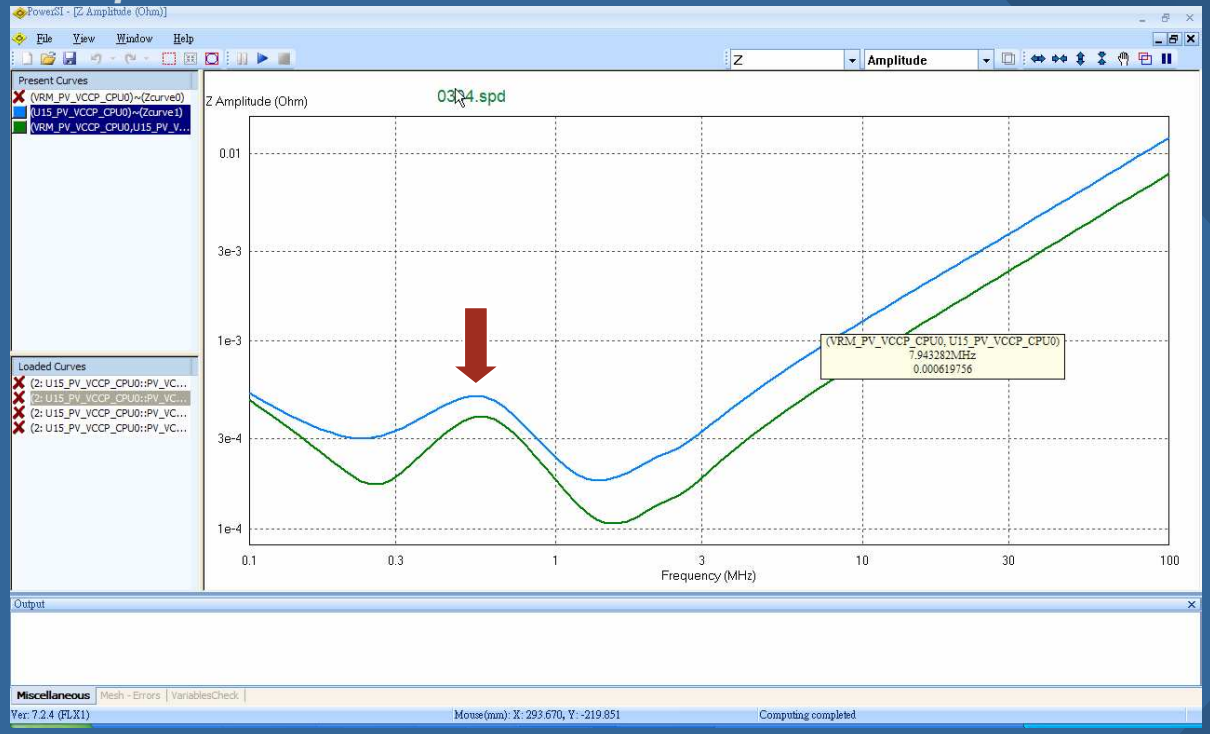
i. Power SI helps us to get more information such as S-parameter than only the impedance.

ii. The whole procedure is easy and fast.



Observe from frequency domain

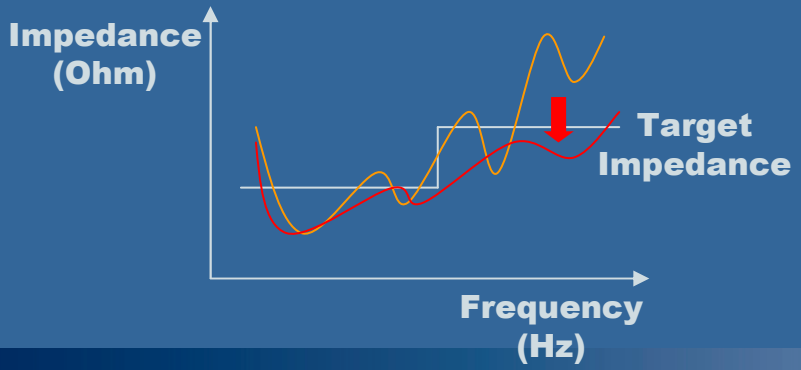
Impedance Plot File:

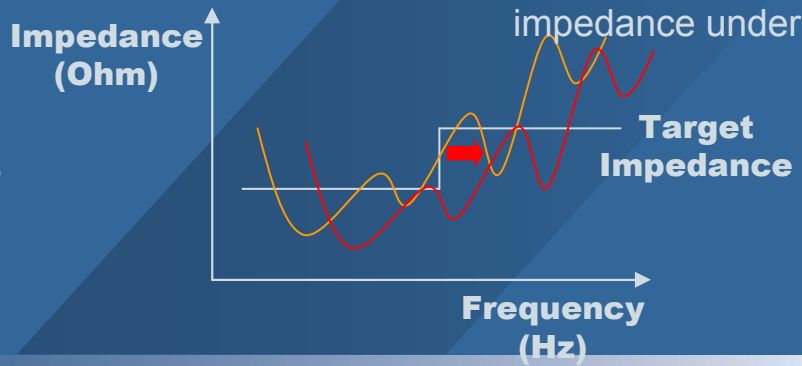


i. Power SI gives us more freedom to choice solutions -> not only to suppress the impedance against certain frequency where the impedance exceed the target impedance.

ii. For Example, we can see there's a resonant frequency at 400KHz. While choosing 220uF as the solution, which is against 300KHz, it only takes 5 capacitor to lower the impedance under the target.

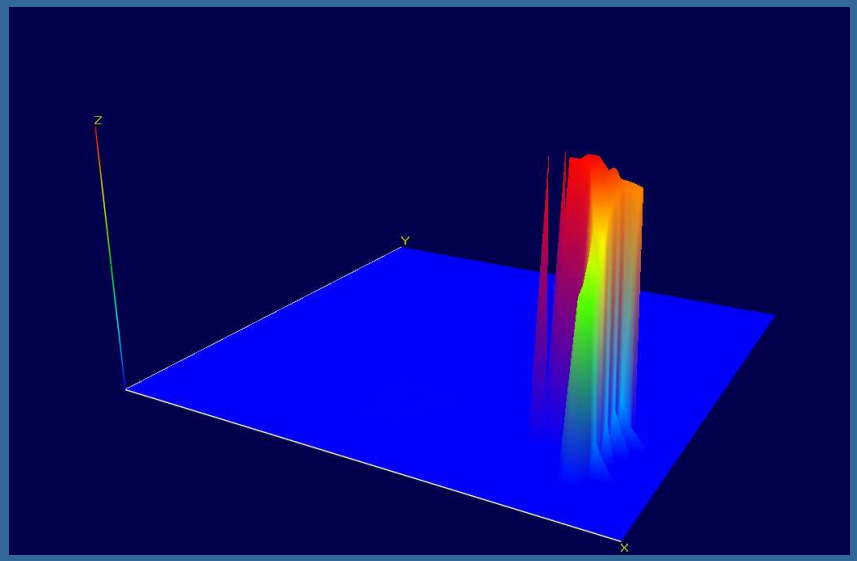
iii. While choosing capacitors which is against 400KHz as the solution, it will takes 8 capacitor to lower the impedance under the target.

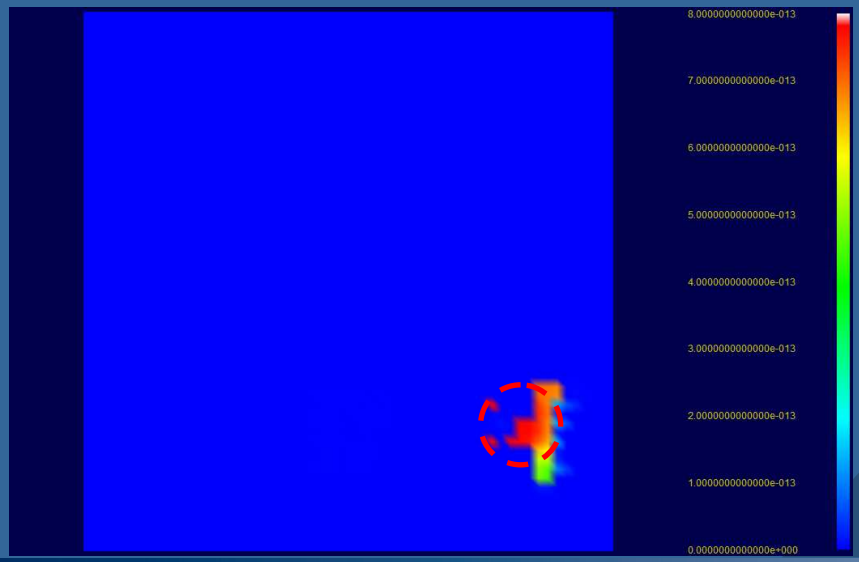




Observe from frequency domain

Impedance Spatial Distribution:



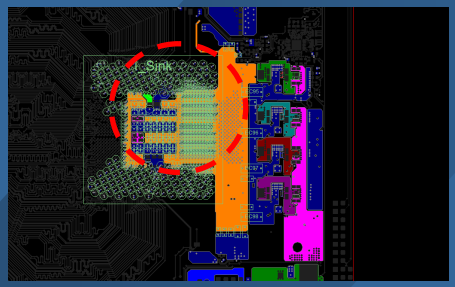


i. Power SI helps us to find out the best location to add capacitors where the impedance is largest.

ii. Power SI's Spatial mode allows us to customized the current sink as Gaussian Pulse or any other waveforms described in PWL to ignore the effect above certain frequency range.

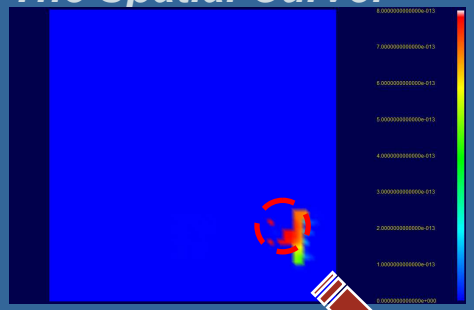
iii. Of course, Power SI's Spatial mode also allows us to set the current sink as an unit impulse, what we do in Extraction mode to extract the S-parameter and Z-parameter.

iv. The whole procedure is easy and fast.



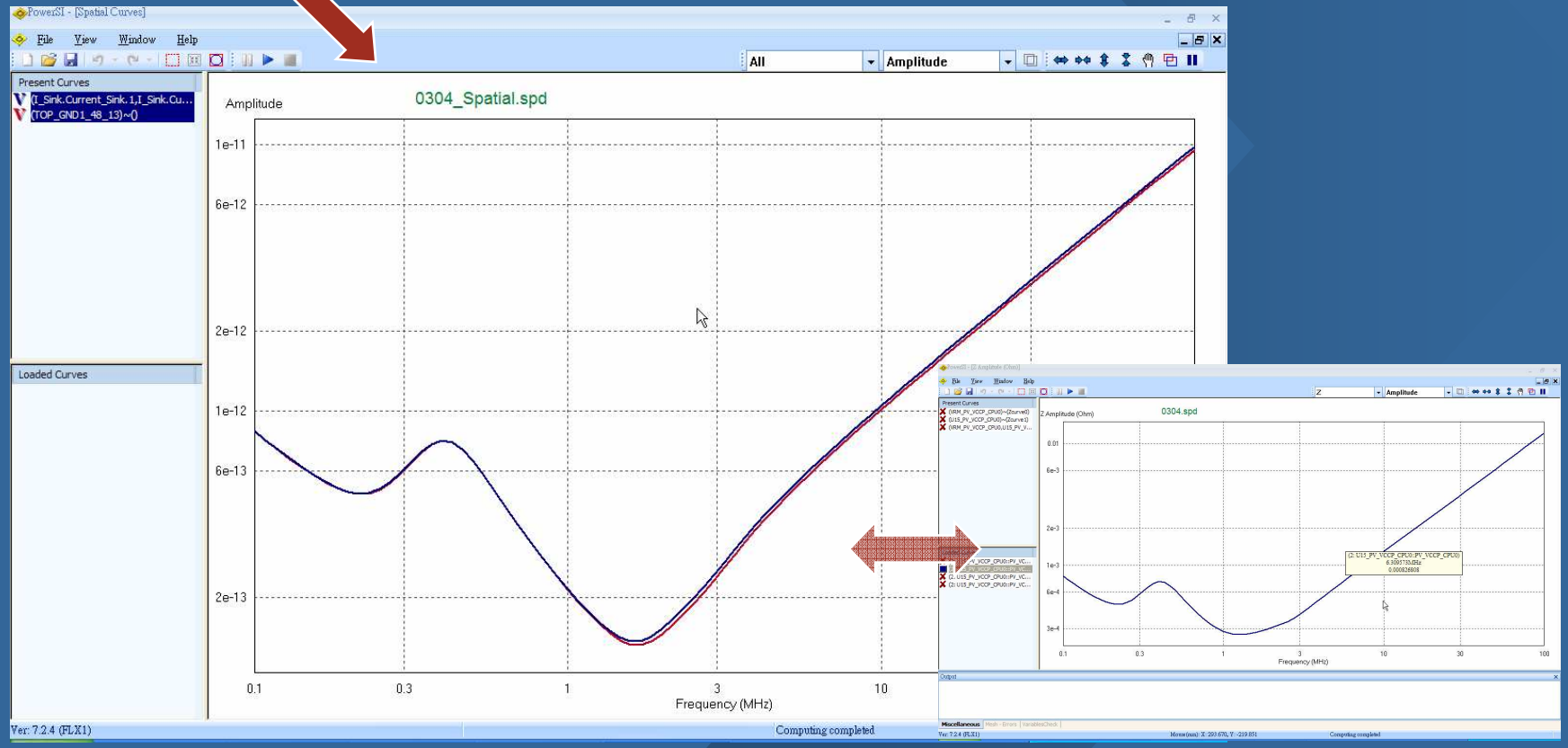
Observe from frequency domain

The Spatial Curve:



i. Spatial Mode still helps us to observe the voltage plot along the frequency axis for certain location, which gives similar information with the one obtained from Extraction Mode.

ii. According to our experience, use Extraction Mode first, and then use Spatial Mode next to get detail and spatial information.



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Observe from Time domain

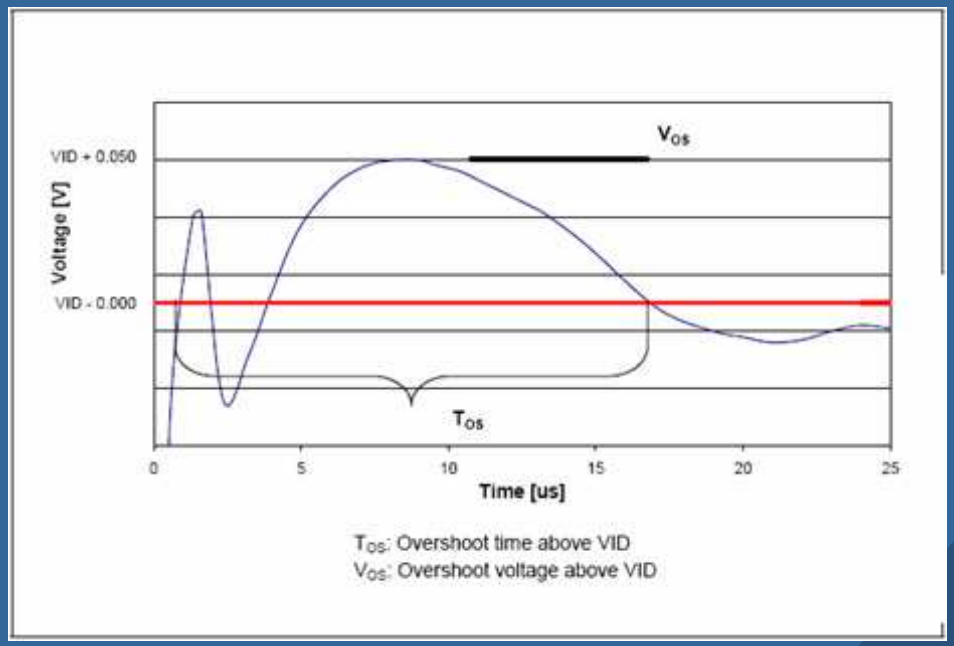
Time Domain Analysis is necessary for PDS of which the SPEC has definition about: 1. The maximum current slew rate, 2. The maximum overshoot voltage above VID, and 3. The maximum overshoot time duration above VID. 4.Load Line

***For Example, if we have*:**

The Maximum Current Slew Rate of 300A/μs

The Maximum Overshoot Voltage above VID=50mV

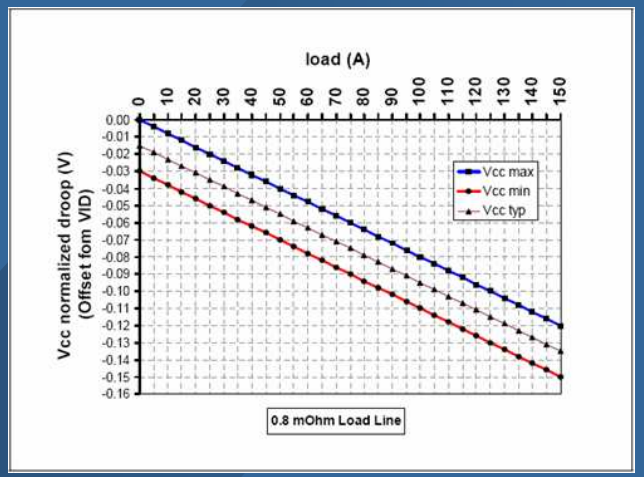
The Maximum Overshoot Time Duration above VID=25μs



The Load Line:

*Vcc(max) = VID – 0.8mΩ*Icc*

*Vcc(min) = VID – 0.8mΩ*Icc-30mV*



Observe from Time domain

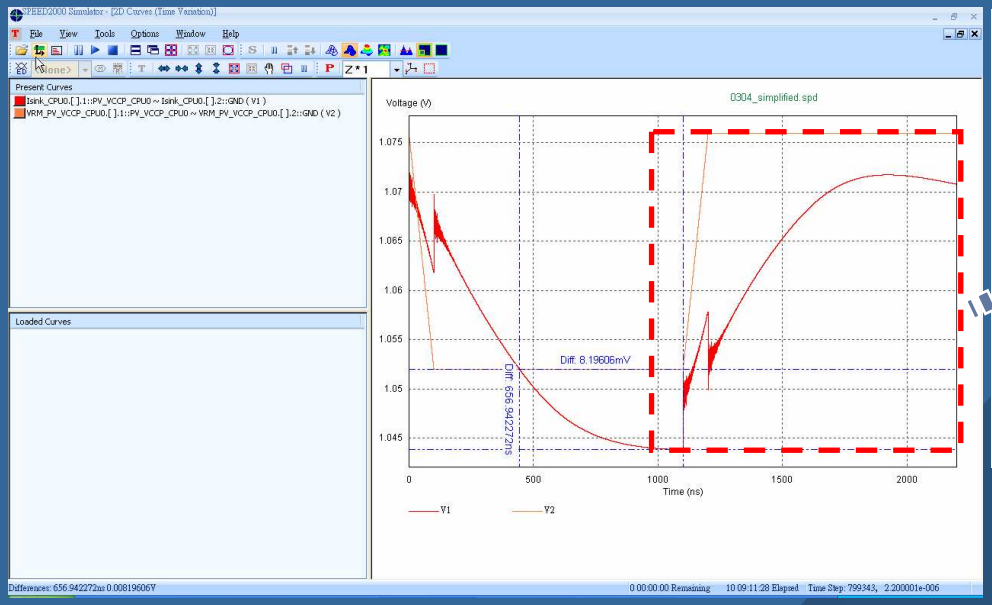
In time domain analysis, we can customize the current sink and the voltage source (i.e. the VRM) according to the maximum current slew rate and the load line defined in VRD Spec and use Speed2000 to emulate the behavior.

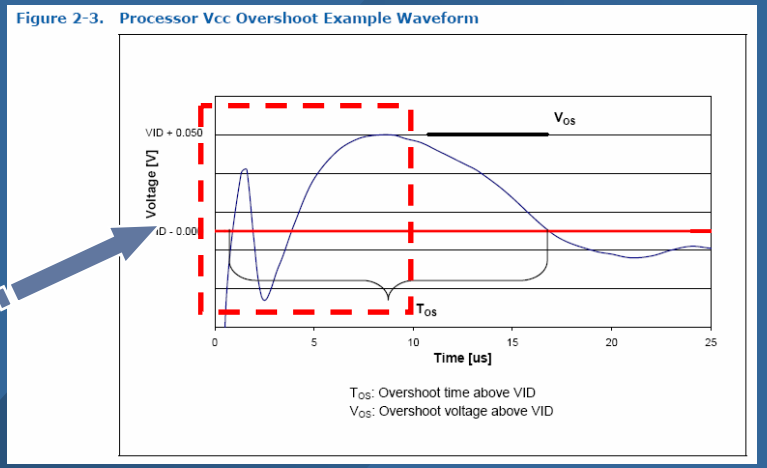
For Example:

VRM V 1 2 PWL(0 1.061 50n 1.061 450n 0.965 4450n 0.965 4900n 1.061 8900n 1.061 9350n 0.965 13350n 0.965)

Current Sink I 1 2 PWL (0 30 50n 30 450n 150 4450n 150 4900n 30 8900n 30 9350n 150 13350n 150)

Simulation Result:





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Summary

- *As the transferring rate increase, Power Integrity becomes a more and more critical issue in modern high speed design.*
- *A complete power integrity analysis should cover both frequency domain and time domain.*
- *Spatial distribution of capacitors would affect how efficiency our solution is.*
- *Due to the concern of cost and time-to-market, Flextronics chooses Sigrity's tool set to ensure our design is safe to work properly.*

Q&A

Thank you~

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