Effective Decoupling Radius of Decoupling Capacitor*

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Abstract: Decoupling capacitors on packages and printed circuits boards are often essential to reduce voltage fluctuations and maintain power and signal integrity. This paper presents a measure for the evaluation of effectiveness of decoupling capacitors placed on package or board structures.

I. Introduction

The integrity of power distribution systems is becoming more critical as the increase of the operating frequency and power consumption of ICs. Faster switching buffers induce larger simultaneous switching noise as their operating voltage levels are lowered. The placement of decoupling capacitors on packages and printed circuit boards is a common approach to reduce the power supply noise [1-3]. However, how to choose the right number and values of decoupling capacitors to achieve the optimal results remains to be a challenge. With given capacitors and board structures, even when equivalent circuit models of the capacitors are known, it is often unclear in what frequency ranges and within what distances these capacitors are effective.

This paper presents a measure to evaluate the effectiveness of decoupling capacitors. The effectiveness of a capacitor is represented by the measure called "effective radius - R_{eff}". A capacitor is regarded effective within its effective radius. The effective radius of a capacitor depends on its equivalent circuit model, its mounting structure, board and dielectric medium parameters, and is frequency dependent. The effectiveness of different capacitors can then be evaluated by comparing their corresponding effective radii.

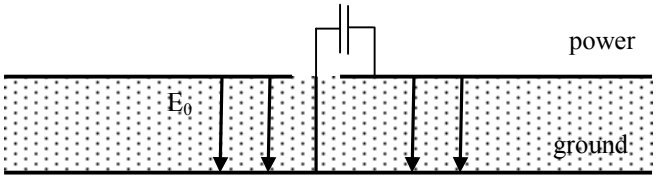

Figure 1: A decoupling capacitor connecting through a via between the power and ground planes

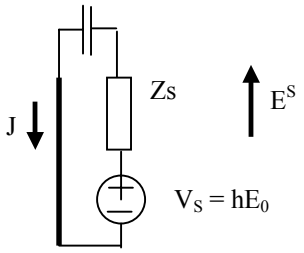

Figure 2: Equivalent circuit of the via connecting the capacitor

II. Derivation of Effective Decoupling Radius

Consider a pair of power and ground planes between which there is a voltage distribution V(x, y). The voltage is assumed to be of certain frequency and have a uniform magnitude throughout the planes. The corresponding electric field distribution is assumed to be E_0. A capacitor is placed between the planes as shown in Figure 1. After adding the capacitor, a current will be induced in the via that is connected to the capacitor and passes through the planes. The current in the via will in turn generate a scattering field between the planes. The scattering field is given by [4]

$$E^S(\rho) = -j\omega \oint_{\Gamma_V} G(\rho \mid \rho') J(\rho') d\Gamma' \tag{1}$$

where $J(\rho')$ is the current density on the surface of the via post. In this analysis, the effects of edges of metal planes are ignored. The two dimensional Green's function is given by

$$G(\rho \mid \rho') = \frac{-j\mu}{4} H_0^{[2]}(k \mid \rho - \rho' \mid) \tag{2}$$

*** The paper is presented in the EPEP conference in 2001**.

$H_n^{[2]}(.)$ is the n-th order Hankel function of the second kind and the integration path Γ_V is the circumference of the via. Assume that the current distribution is uniform along the circumference of the via post, then the scattering field can be given by

$$E^S(\rho) = -\frac{\omega\mu}{4} J \oint_{\Gamma_V} H_0^{[2]}(k\,|\rho - \rho'|)\, d\Gamma' \tag{3}$$

where k is the wave number in the medium. By the small argument approximation of the Hankel function, it can be shown that when $\rho = a$, which is the via radius, (3) can be simplified to

$$E^S(\rho)\Big|_{\rho=a} = -\frac{\omega\mu}{4} J \cdot 2\pi a \cdot H_0^{[2]}(ka)\,. \tag{4}$$

The input impedance Z_S looking into the planes where the capacitor is connected can be found by letting the total electric field equal to zero on the surface of the via,

$$\left(E^S(\rho) + E_0\right)\Big|_{\rho=a} = 0 \tag{5}$$

then

$$Z_S = \frac{E_0 h}{2\pi a \cdot J} = \frac{h\omega\mu H_0^{[2]}(ka)}{4}\,. \tag{6}$$

The equivalent circuit, looking into the power and ground planes at the capacitor location, is represented in Figure 2, where Vs is the open circuit voltage when the capacitor is absent, Zc is the impedance of the capacitor. The surface current density on the via surface is therefore

$$J = \frac{V_S}{(Z_C + Z_S)2\pi a}\,. \tag{7}$$

At any location in the power and ground planes, the total voltage is the sum of the scattering voltage and the original voltage,

$$V = \left(E_0 + E^S\right)h \tag{8}$$

where the scattering field at any location is found by (1).

Assume the voltage without the capacitor is 1V everywhere. The contour plot of the voltage amplitude distribution around the capacitor is shown in Figure 3. It can be seen that the voltage amplitude decreases as the location gets closer to the via. We define the radius of the circle within which the total voltage is lower than 0.5 as the decoupling radius, or the effective radius R_{eff}, of the capacitor. The decoupling radius is a measure of the effectiveness of a decoupling capacitor. It is a function of many factors, including the plane geometry, the frequency as well as the capacitor parameters. In the next section, the effects of these factors on R_{eff} will be studied.

III. Simulation Results

In all the examples, the materials between the power and the ground planes are assumed to have a dielectric constant of 4.0. First consider the case where the plane separation is 200 um and the via radius is 200 um. Figure 4 shows the total voltage away from a 10 μF capacitor at 200 MHz. The capacitor model includes an ESR of 10 mohm and an ESL of 0.1 nH. Its R_{eff} is several millimeters. The dotted line shows the voltage distribution if a shorting via is used instead of a capacitor, which is the maximum effect that can be achieved using any capacitor.

Figure 5 shows the effective radius of a 1 nF capacitor. ESR is 100 mohm and ESL is 0.2 nH. Impedance of the capacitor Zc and the input impedance Zs of the infinite power ground planes are plotted in the same figure. The figure shows that the effective radius of a capacitor is frequency dependent, it also indicates that the largest effective radius may not appear exactly at the series resonant frequency of the capacitor.

The effective radius R_{eff} of a capacitor depends on several factors. Figure 6 shows the effective radius of a 10 uF capacitor with different ESLs. The ESR of the capacitor is 10 mohm. It can be seen from Figure 6, R_{eff} decreases dramatically with the increase of ESL. Figure 7 shows R_{eff} for different capacitances while a ESL of 0.1 nH and a ESR of 10 mohm remain the same. It shows that for different capacitance, the effective radius and the effective frequency range will change accordingly.

To see the effect of power and ground plane separations, Figure 8 shows R_{eff} of a 10 µF capacitor connected to a plane structure with the spacing between planes varying from 200 µm to 50 µm. Zs decreases as the plane spacing is reduced. For the 50 µm spacing, R_{eff} becomes zero, which indicates that for such a small separation between the power and ground planes, the capacitor is ineffective or unnecessary.

Figure 9 compares R_{eff} of three types of capacitors. The plane spacing is 30 mils and the via radius is 5 mils. The parameters of each capacitor are listed in the following table. It can be seen from figure 9 that IDC 0508 capacitor has a much larger R_{eff} over the other two.

	capacitance	ESR	ESL	mounting inductance
AVX0603	0.1 µF	50 mohm	0.8 nH	0.13 nH
AVX0805	1.0 µF	20 mohm	0.95 nH	0.14 nH
AVXIDC 0508	1.0 µF	20 mohm	0.11 nH	0.02 nH

IV. Conclusions

The effectiveness of decoupling capacitors is investigated in this paper. A new measure to evaluate the effectiveness of a capacitor, the effective radius R_{eff} , is introduced, derived and found to be useful in the evaluation and comparison of capacitors.

Reference:

[1] Alex Waizman, Chee-Yee Chung, "Package Capacitor Impact on Microprocessor Maximum Operation Frequency," *IEEE 51th Electronic Components and Technology Conference*, May 2001.

[2] Y. L. Li, T. G. Yew, C. Y. Chung, and D. F. Figueroa, "Design and Performance Evaluation of Microprocessor Packaging Capacitors Using Integrated Capacitor-via-plane Model," *IEEE Transactions on Advanced Packaging*, vol. 23, No. 3, pp. 361-367, Aug. 2000.

[3] Larry Smith, Raymond Anderson, Doug Forehand, Tom Pelc and Tanmoy Roy, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology", *IEEE Transactions on Advanced Packaging*, pp. 284-291, Aug. 1999.

[4] Constantine A. Balanis, *Advanced Engineering Electromagnetics*, John Wiley & Sons, Inc., 1989.

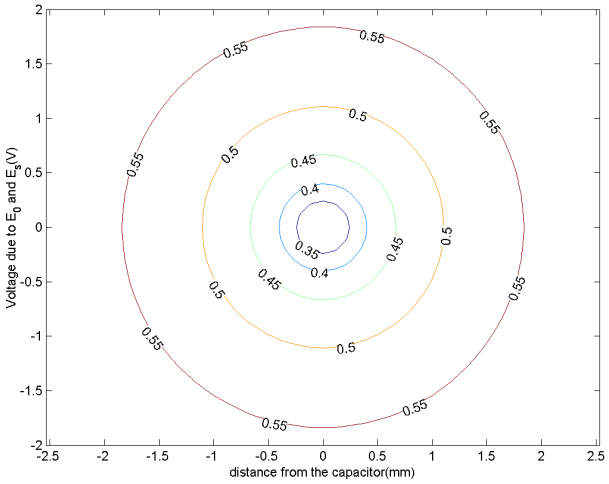

Figure 3: Voltage distribution around the decoupling capacitor

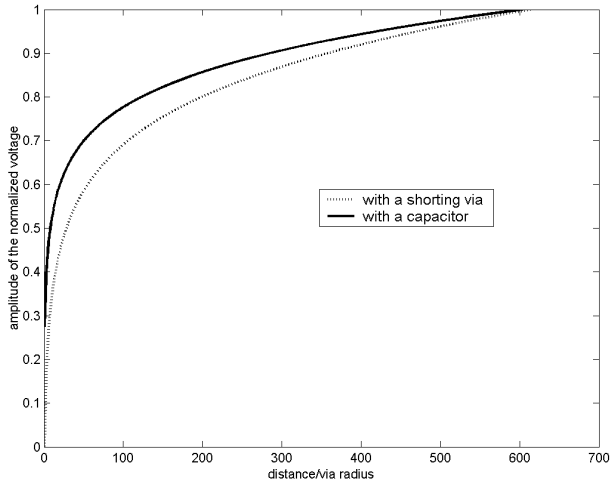

Figure 4: Voltage away from the 10 µF capacitor at 200 MHz. ESR = 10 mohm and ESL = 0.1 nH. Plane separation h = 200 um and via radius is 200 um.

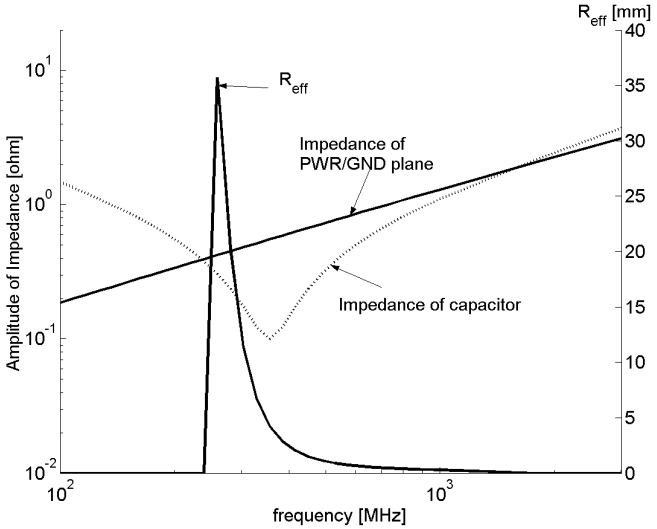

Figure 5: R_{eff} of a 1 nF capacitor plotted together with the impedances of the capacitor and the power ground plane. ESL = 0.2 nH and ESR = 100 mohm.

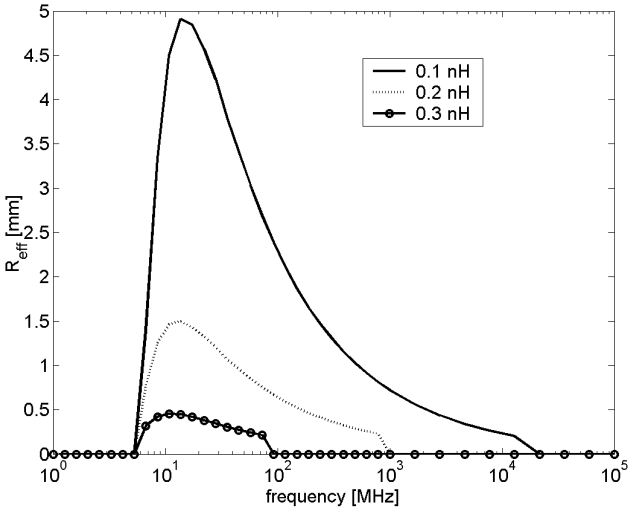

Figure 6: R_{eff} of a 10 uF capacitor with different ESL values. ESR = 10 mohm.

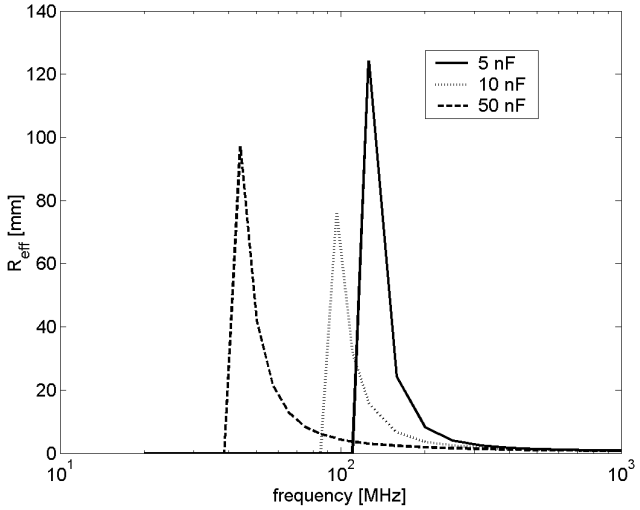

Figure 7: R_{eff} of a capacitor of different capacitances with ESL = 0.1 nH and ESR = 10 mohm.

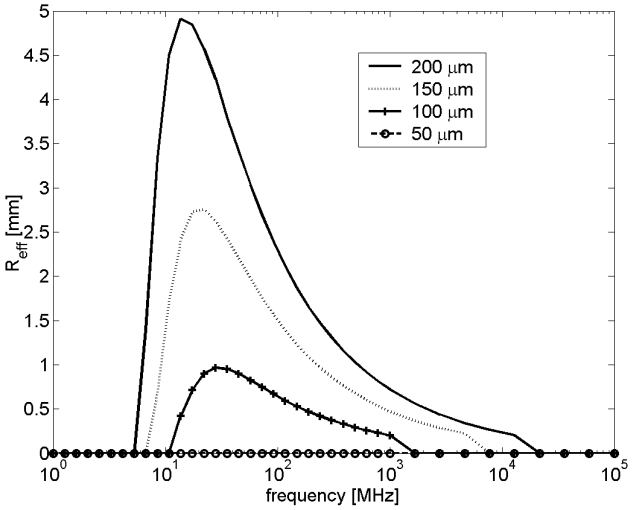

Figure 8: R_{eff} of a 10 uF capacitor connected to planes with different plane spacing. ESL = 0.1 nH and ESR = 10 mohm.

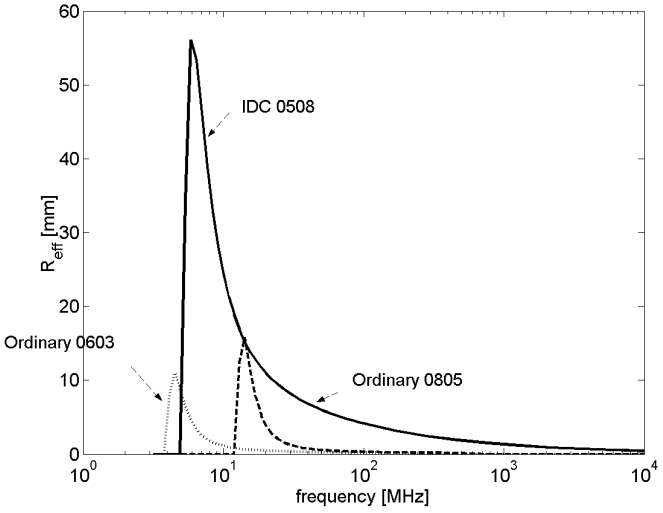

Figure 9: R_{eff} of three types of capacitors.