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Integrity drives successful electronic product design

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As the pursuit of increased performance and lower cost continue, product design trends for chips, packages and boards pose evermore severe power integrity (PI) and signal integrity (SI) challenges. Automated PI and SI design techniques must be applied within each domain, but analyses increasingly are required to cross domain boundaries. Electrical model abstractions must consider accuracy vs. capacity tradeoffs. Tool providers have begun to support such cross-domain analysis and model abstraction, a trend that will proliferate over time.

For today's increasingly large and complex digital integrated circuit designs, design power closure and circuit power integrity drain engineering resources, impacting the device's total time to market. Greater use of battery-powered portable (often wireless) electronic systems is driving demand for chips that consume the smallest possible amounts of power while achieving the best performance. The sheer power consumed by some devices requires expensive packaging and heat sinks. Heat gradients can cause mechanical stress, leading to early breakdown; physically delivering this power into the chip is not trivial. Implementing a reliable power network and minimizing power dissipation are major challenges for today's design teams.

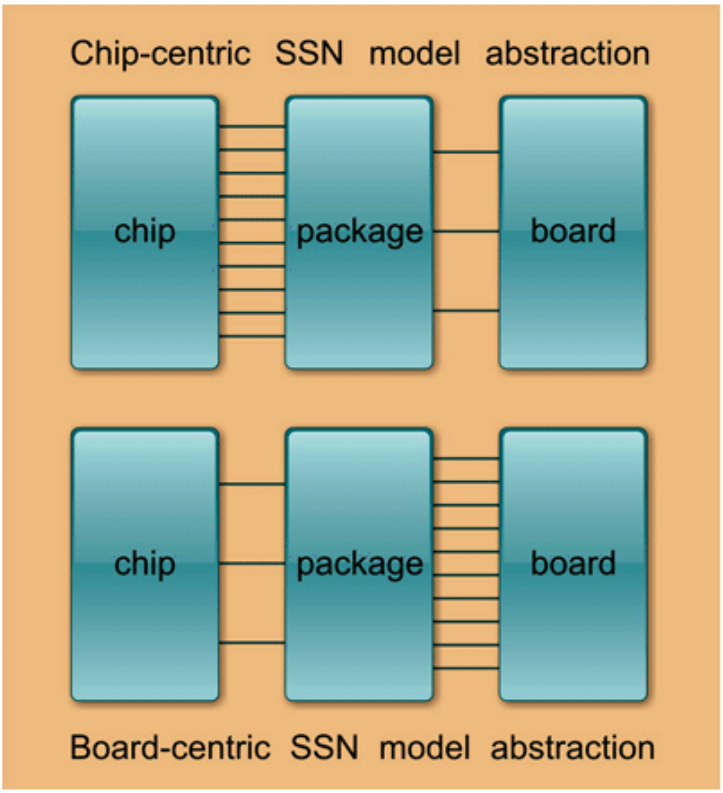
For power distribution, the first problem is getting power from the outside world through the device's package to the silicon chip. Wires used to distribute power throughout the chip have associated resistances--the longer the wires, the bigger the resistance; and the bigger the resistance, the greater the associated voltage drops. Flip-chip packaging technology minimizes power travel distance to reach internal logic by supporting many more power and ground pads. Inductance of the solder bumps in flip-chip packages is significantly lower than that of bonding wires in traditional packaging techniques. Regardless of the package type, an abstract model with information about the RCLK parameters is crucial for accurate on-chip analysis. Package and board model accuracy is critical for power sign-off at the chip level.

Creating optimal low-power designs involves tradeoffs such as timing vs. power and area vs. power at different design flow stages. Engineers must have access to appropriate low-power analysis and optimization engines that are integrated with and applied throughout the RTL-to-GDSII flow. A key requirement for a true low-power design environment is early analysis of voltage drop, signal integrity and other effects using available data, and successive refinement as more-accurate data becomes available. Package- and board-level abstracts are necessary for accurate chip-level analysis and for eliminating chip failures due to effects such as SSN.

Package and PCB-centric challenges

Packages and boards must deliver stable, adequate power to chips, and provide noise-free signal paths. Power delivery must address both static and dynamic requirements. Signal paths must include low-speed control, high-speed clocks and gigabit serial channels.

Power supplies are linked to chips through a power delivery network (PDN) that contains a voltage regulator module (VRM), board and package. A VRM has sense lines to detect remote IR drop and control rail voltage. Board and package parasitcs imply VRM control is effective to a maximum of 100 kHz; therefore, many high-performance chips have local VRMs.



Different levels of model abstraction are required for chip-centric and board-centric SSN analyses.

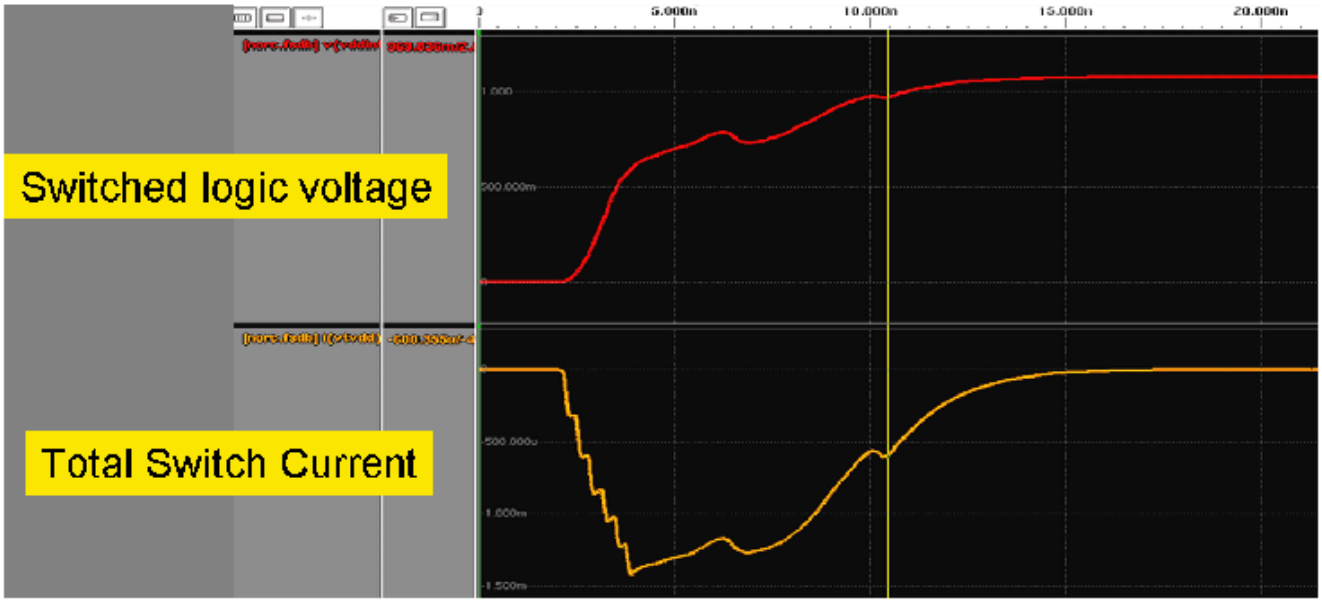
One major issue is package and board power-handling capacity. Chip current requirements are so high that plane current density and via current constraints drive designs. Excessive plane current density results in fire risk for organic substrates. Vias act as fuses and have caused catastrophic failure of entire PDN rails mandating detailed DC IR drop analysis and electrical rule check (ERC) sign-off. ERC violations of current flow are back-annotated directly to layout tools, enabling such issues to be corrected early in the design.

Noise margins become razor thin with decreased supply voltage and increased current. More careful IR drop design is required for DC resistance and optimal placement for VRM sense lines. Such simulations are completed in minutes and performed long before the layout is finalized.

Decoupling capacitors (decaps) are connected to power planes throughout a PDN to provide the required dynamic current to maintain stable rail voltages. Decap self-resonances provide low impedance paths between power planes through which transient return currents flow. Decaps also prevent power plane resonances for reduced radiated emissions. Board decaps are typically 1 nF or 100 microF, and package decaps 1 nF to 10 microF. Board decaps are effective to a maximum of 100 MHz, and package decaps to approximately 300 MHz. On-chip capacitance stabilizes rail voltage above this frequency.

Designers cannot reliably predict PDN performance without detailed simulation tools. Circuit simulation cannot address PDN design because signal return paths are assumed to be ideal and electromagnetic (EM) simulation tool capacity is quickly exceeded by even the simplest PDN. Algorithms that are a hybrid of circuit and EM analyses are commonly applied for PI and SI simulation. These tools accurately characterize all dynamic effects throughout the entire PDN ñ package, board and chip. They provide frequency-dependent impedances and transient power plane noise voltages as simulation results, while enabling visualization of plane resonances for proper placement of decoupling capacitors.

Component vendors may provide overly robust design guides for decap placement to assure performance. New cost-based decap optimization tools maintain analytically known performance, while reducing excess decaps. Decap cost reductions of 15 to 50 percent are typical. Decap reductions result in recaptured design area, easing routing and reducing layer count.



Signal channel design

SI engineers apply circuit simulation to concatenate component models for pre-layout signal channel design. Netlists or schematics are created to investigate loss, impedance and 3D transitions. EM simulation is applied to generate parametric component models. Designs of Experiments (DOE) analyses are performed to predict manufacturing variations. Schematics must be augmented manually to include proximity coupling, a tedious process; accuracy depends on engineer judgment to include all relevant coupling. Capacity limitations make it impractical to perform EM verification for all but the simplest signal channel. Many circuit and EM simulation tools are available, and vendors differentiate their solutions based on both technology (e.g., capacity, generality), and automation and SI task focus.

This SI approach is familiar, but fails to consider the reality of non-ideal return paths caused by structures such as; split planes, multi-layer vias, and decoupling capacitors. The coupling between signals and planes caused by these structures highlights the interdependence of SI and PI effects. Hybrid EM/circuit analysis tools include all such effects, and must be applied to fully characterize the package-board system.

A critical product-level challenge occurs due to power plane fluctuations and proximity signal coupling when multiple I/O drivers are switched simultaneously ñ SSN. Many SI engineers consider SSN a signal channel issue, but it is predominantly a power delivery issue. This effect can be partially mitigated through on-chip clock gating, but careful PDN design across chip-package-board domains is essential to meet SSN challenges. Model abstractions are valuable for simplifying detailed analysis of combined chip-package-board effects.

Extraction tools are available for detailed modeling of on-chip power grid and signals, and for entire packages. Per-pin models are extracted for chip and package regions local to high-speed I/O drivers. More abstract models are applied for remote chip regions and the package-board interface. It is common to short together multiple pins of a power net at the package-board interface. The board PDN is represented as a frequency-dependent impedance, and signal lines as lumped loads; both are extracted from a hybrid EM/circuit whole-board analysis. This detailed chip model and abstracted package model typically are concatenated using a time domain circuit simulator. Switching schemes and physical design modifications are explored with node voltages from the circuit simulator, representing both power and signal noise effects.

Similar model abstraction is applied to board-centric SSN analysis, which requires more detail at the board-package interface and less at the package-chip interface. I/O drivers commonly are represented as IBIS models or simply transient current sources with a known current profile. When board designers lack access to the package layout, both PDN and signal parasitics of the package should be included in component models. Board designers often represent component power planes as equivalent RC loads.

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