Application and Extraction of IC Package Electrical Models for Support of Power and Signal Integrity Analysis

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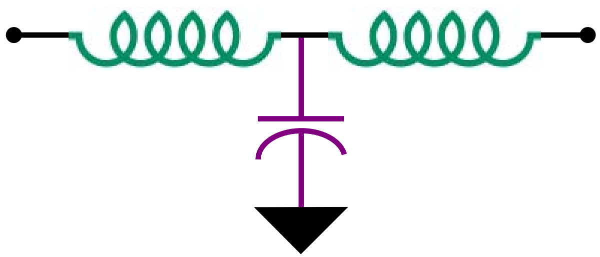
Focus:

- Understand how extraction conditions, model type and electrical analysis application dictate requirements for IC package models.

- Sigrity's package extraction tool XtractIM® is applied.

- We examine
  - -- extraction frequency for 1-segment RLCK model
  - -- bandwidth of data upon which model is based
    (*DC, low frequency, broadband circuit parameters*)
  - -- type and bandwidth of model
    (*lumped to fully distributed*)
  - -- edge rate of the switching signals
    (*effective bandwidth of signals*)
  - -- effects of above choices on PI-SI simulation of noise in high-speed package systems

Single-segment RLCK Models



Bandwidth

-- net length < 10% wavelength

-- plane size < 15% to 20% of first resonance (*without decaps*)

Estimated reliably by considering length of longest signal net.

Extraction

-- DC data: (a) split DC inductance to form symmetric T-circuit

-- AC data: (b) closed form equation fit to single frequency point data

(c) optimize to broadband data

AC single-frequency extraction

-- any frequency (F_0) ***in this bandwidth*** can be applied (*including DC*)

-- R increases with F_0

-- L decreases initially with F_0, then increases with skin loss

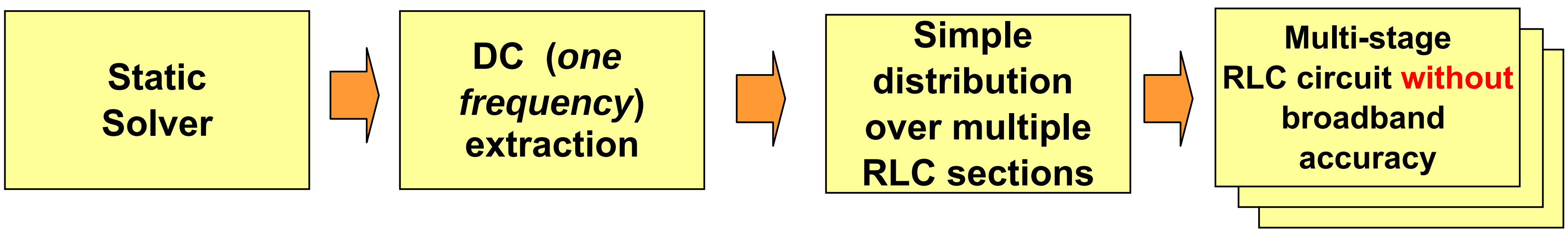
-- C insensitive to F_0

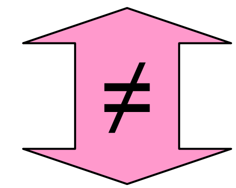
AC multi-frequency extraction

-- maximum frequency should be in this bandwidth

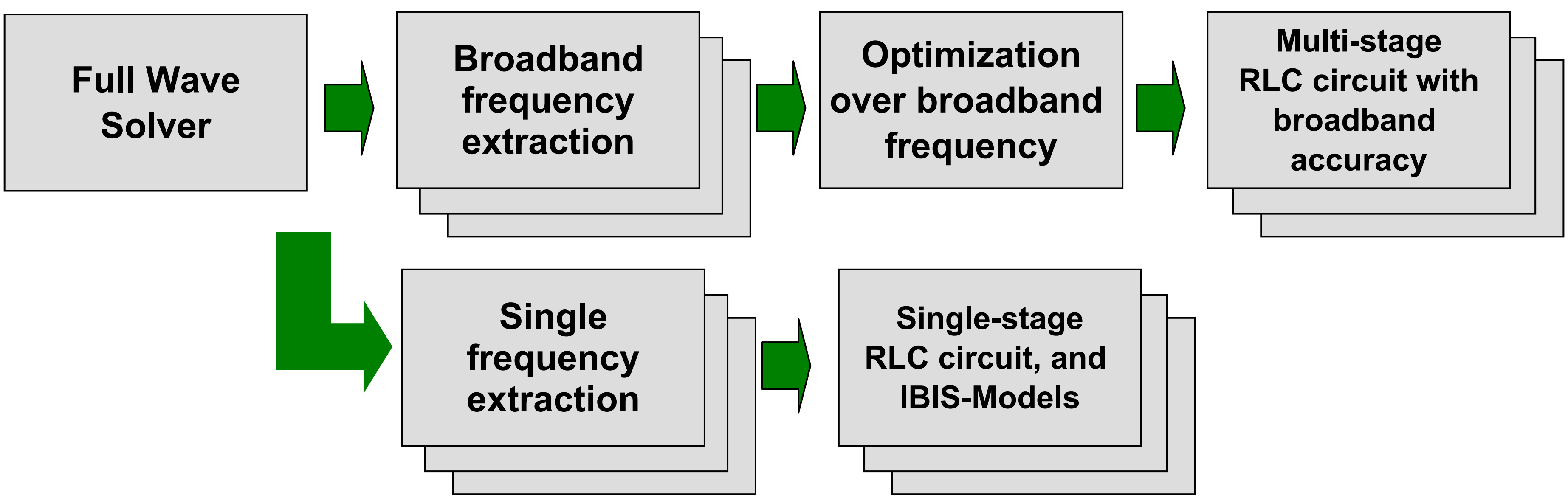
Electrical Package Model Extraction

Traditional Approach

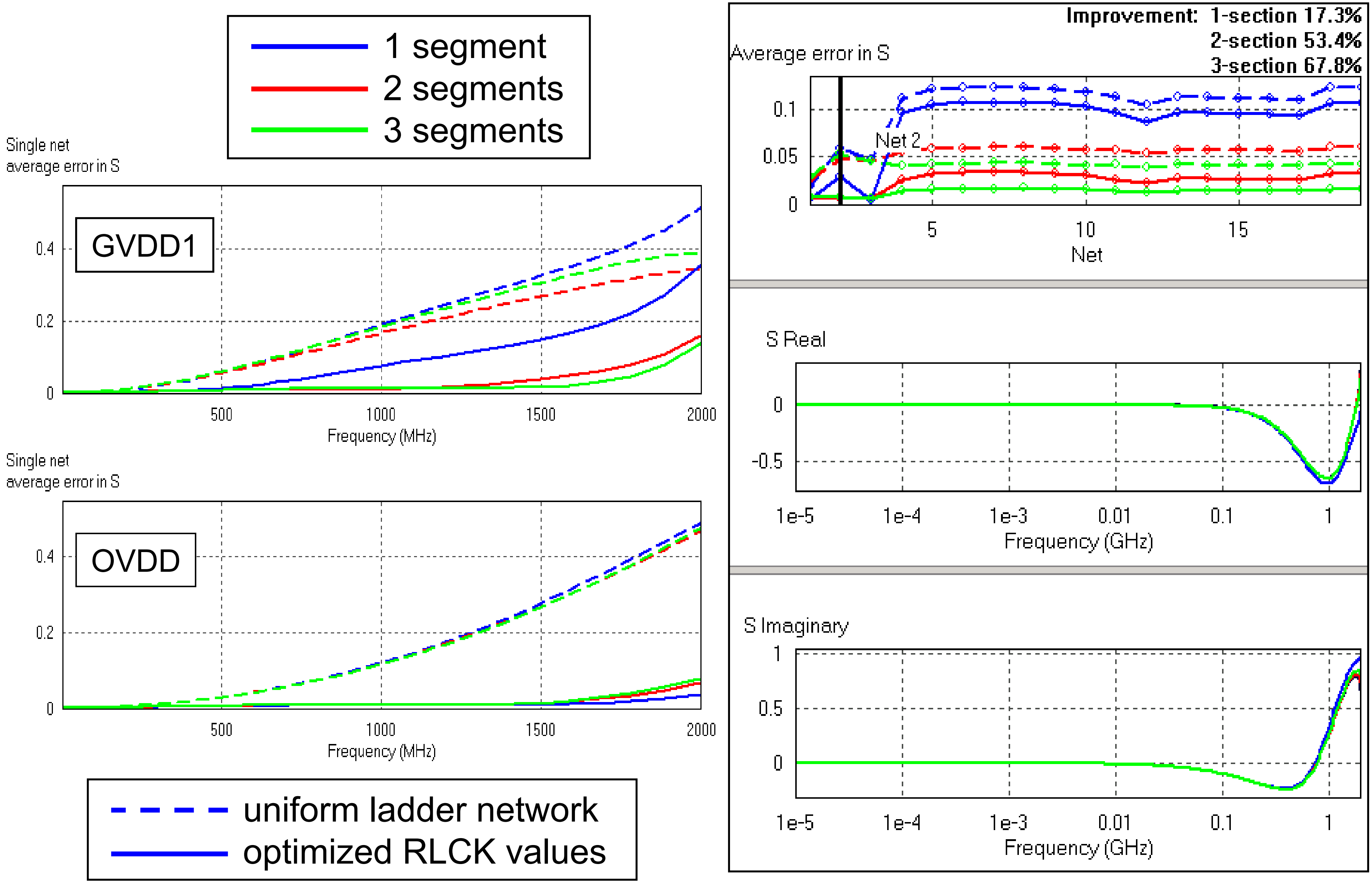




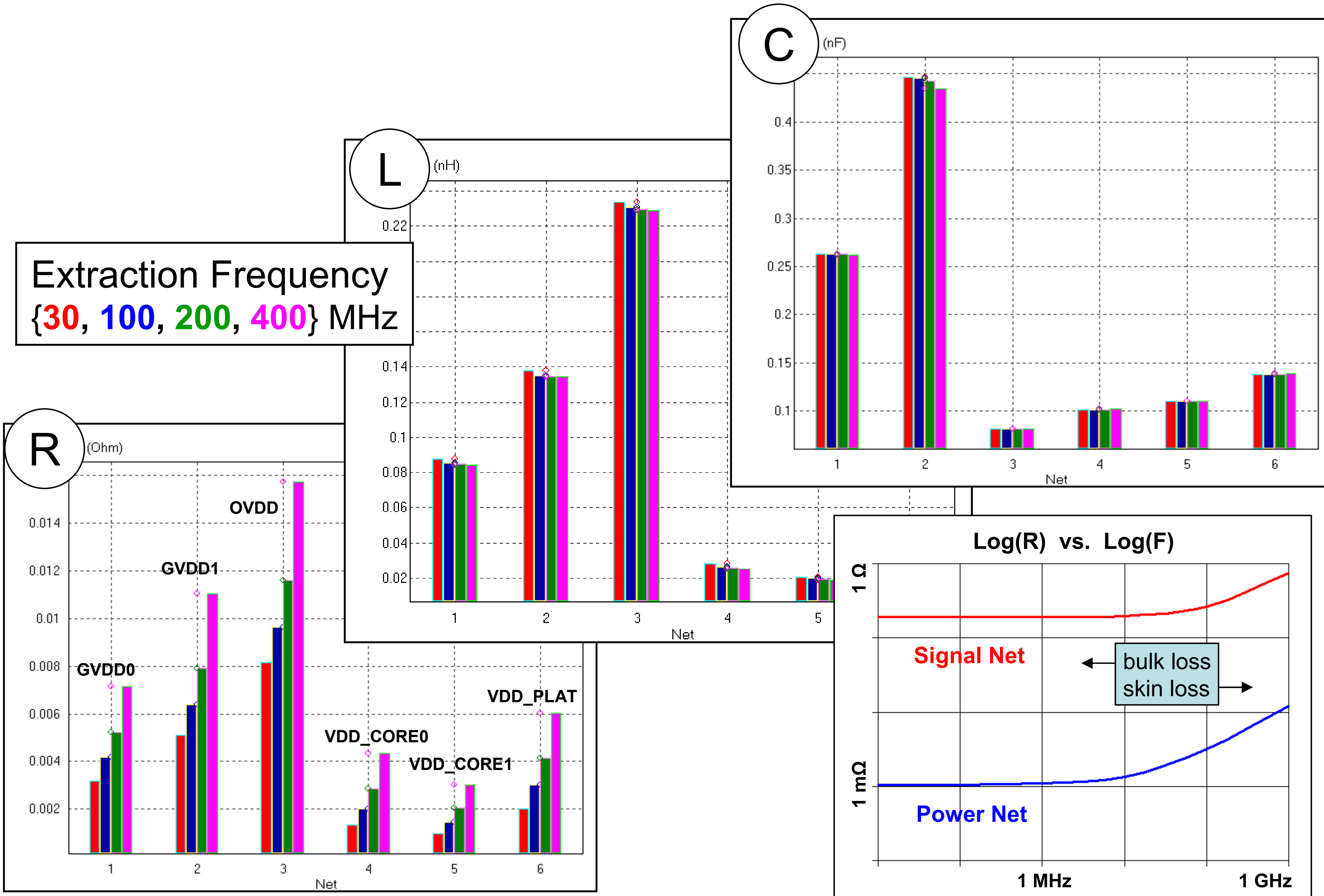
XtractIM Approach



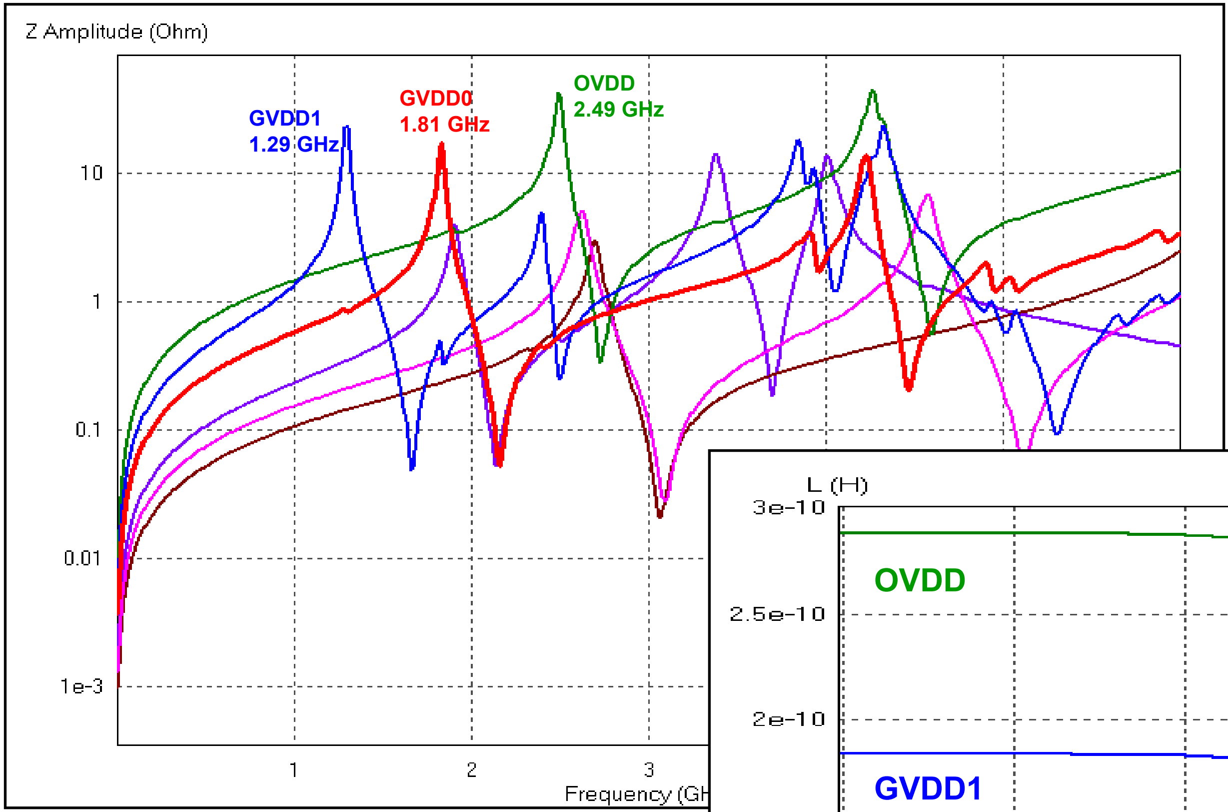
Optimized Broadband RLCK Model: DC to 2 GHz



Single-segment RLCK Model vs. Extraction Frequency

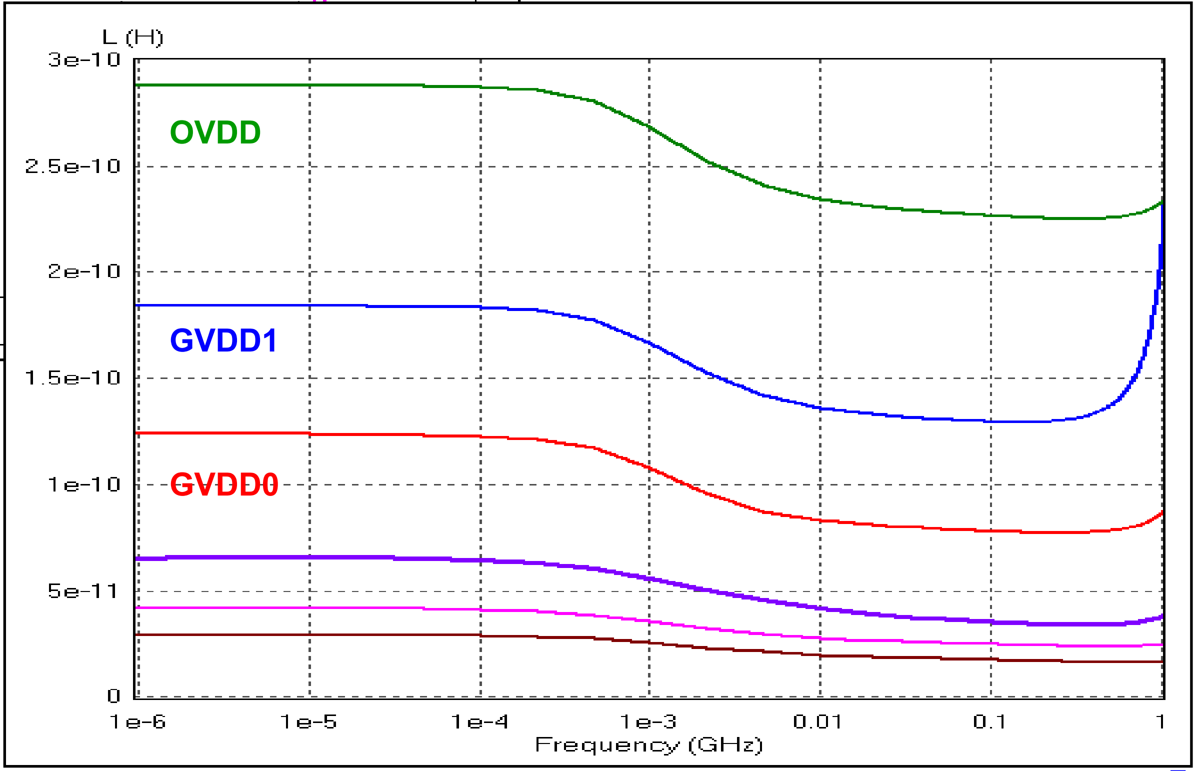


Broadband Impedance and Extracted Loop Inductance



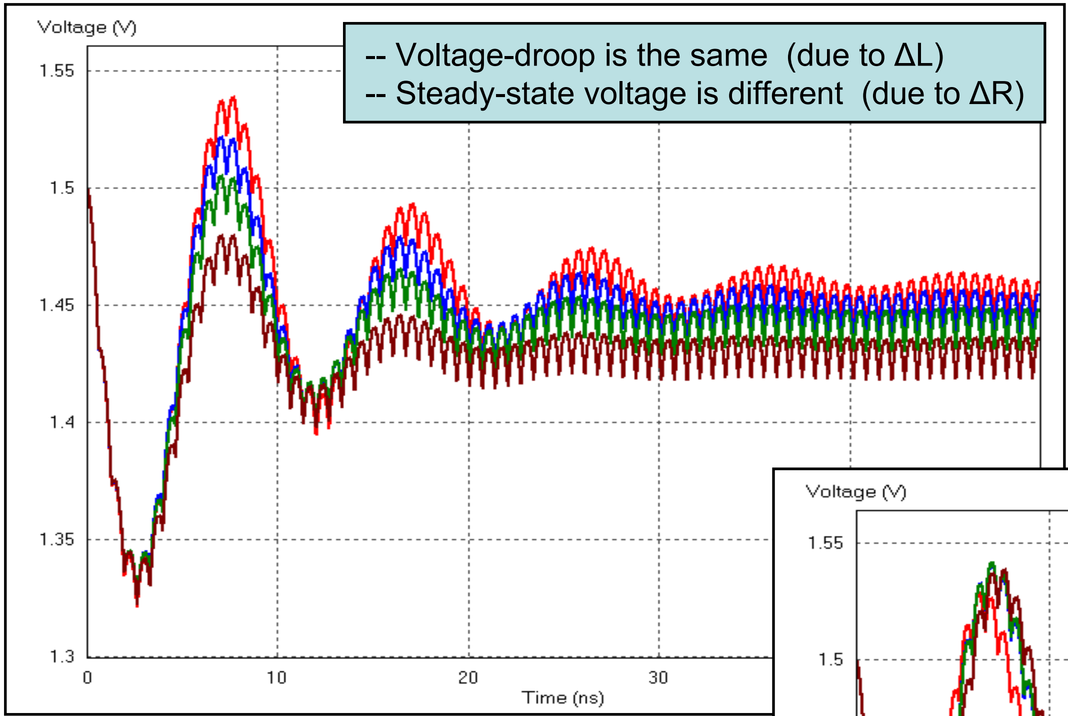
L(freq) behaves as expected – internal inductance decreases as DC bulk current flow transitions to AC skin current.

1-segment RLCK model breaks down as we approach ≈ 20% of net resonance.
Specifically, L value increases rapidly with frequency.

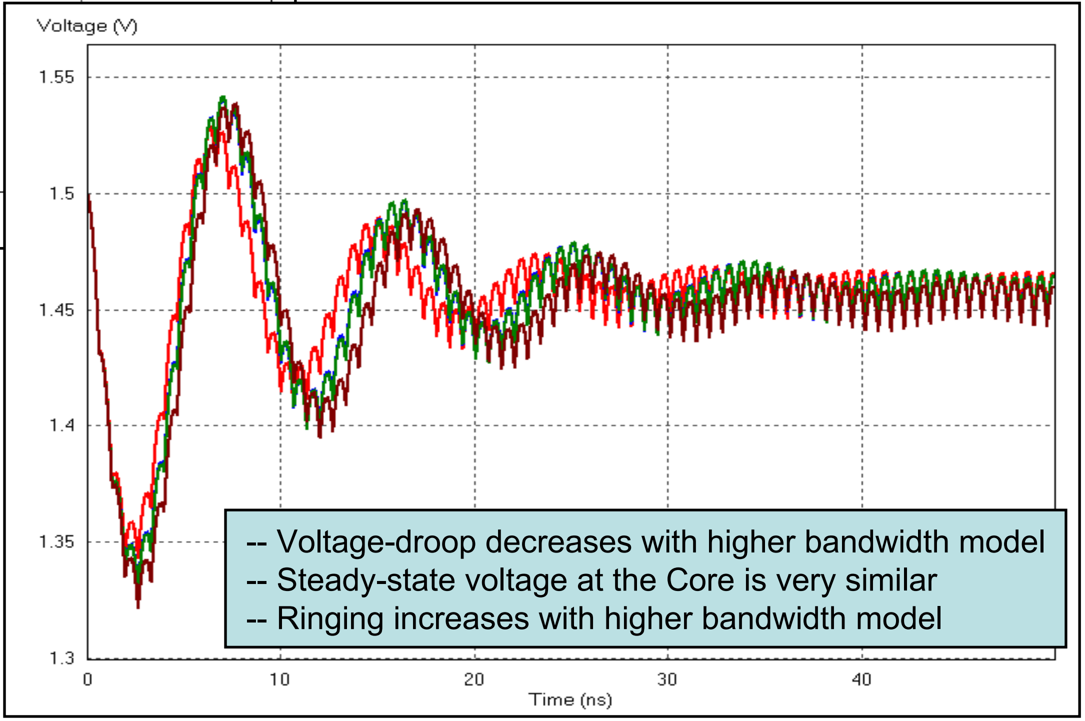


Core Noise Voltage for Pulsed Core Current

Pav = 25W, V= 1.5 V, f = 1.5 GHz, Cdie = 80 nF, Rg = 4 mOhm



Single-segment model
{30, 100, 200, 400} MHz



Model Type:

- **1-segment, 30 MHZ**
- **3-segment, 2 GHz**
- **3-segment, 6 GHz**
- **S-parameters**

SSN at Load with 14-of-16 DDR Signals Switched

F_{switch}= 400 MHz , T_{rise}= T_{fall}= 100 ps with

Signal Integrity

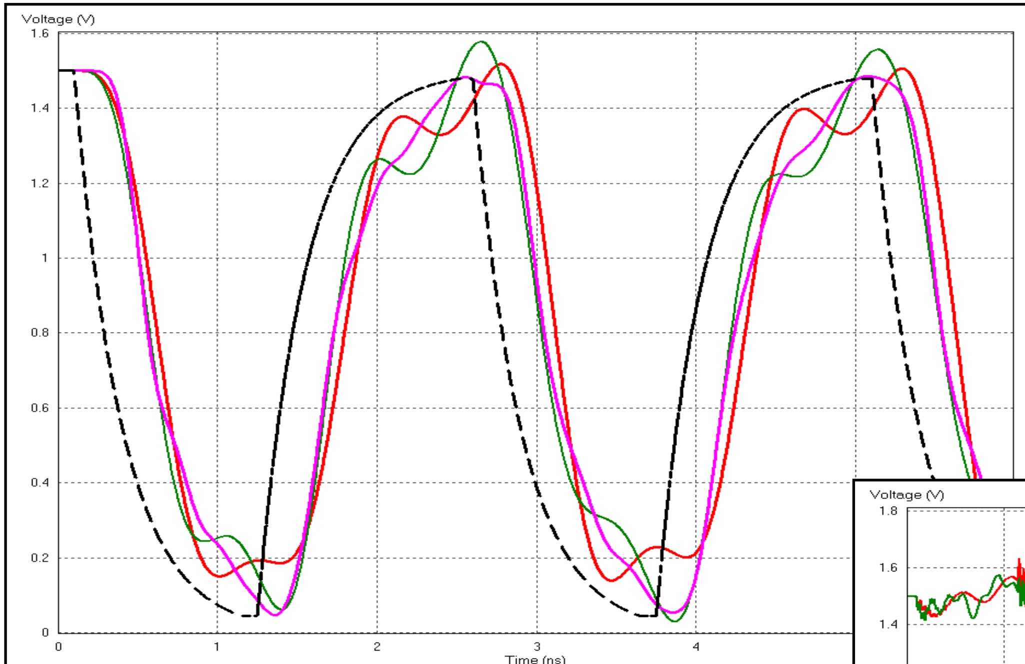
Model Type:

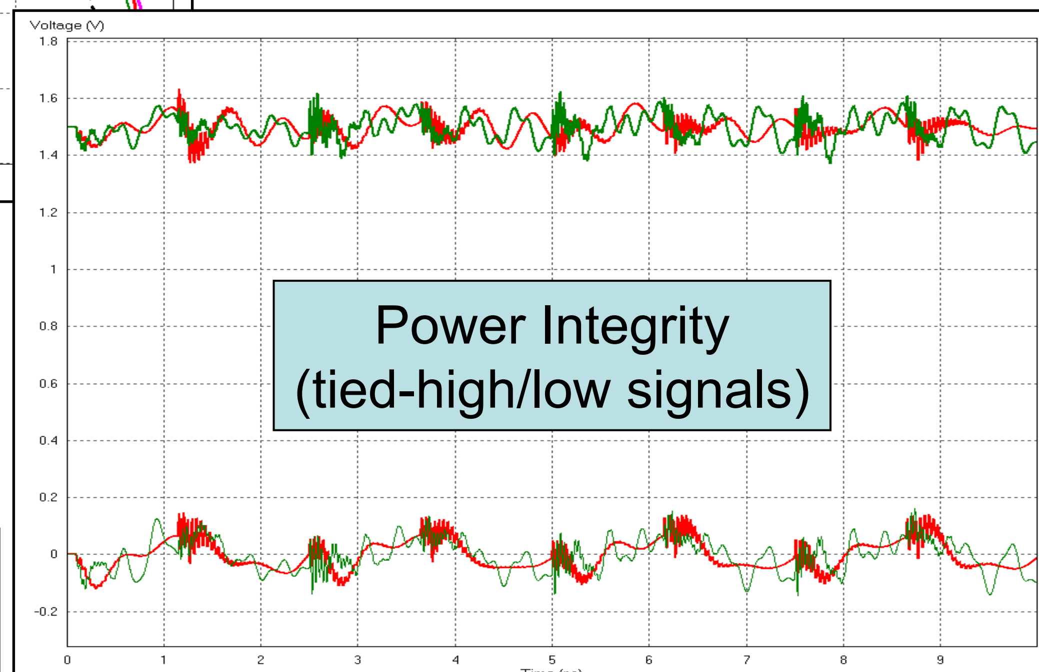
None

1-segment, 30MHz

1-segment broadband 2GHz

3-segment broadband 2GHz





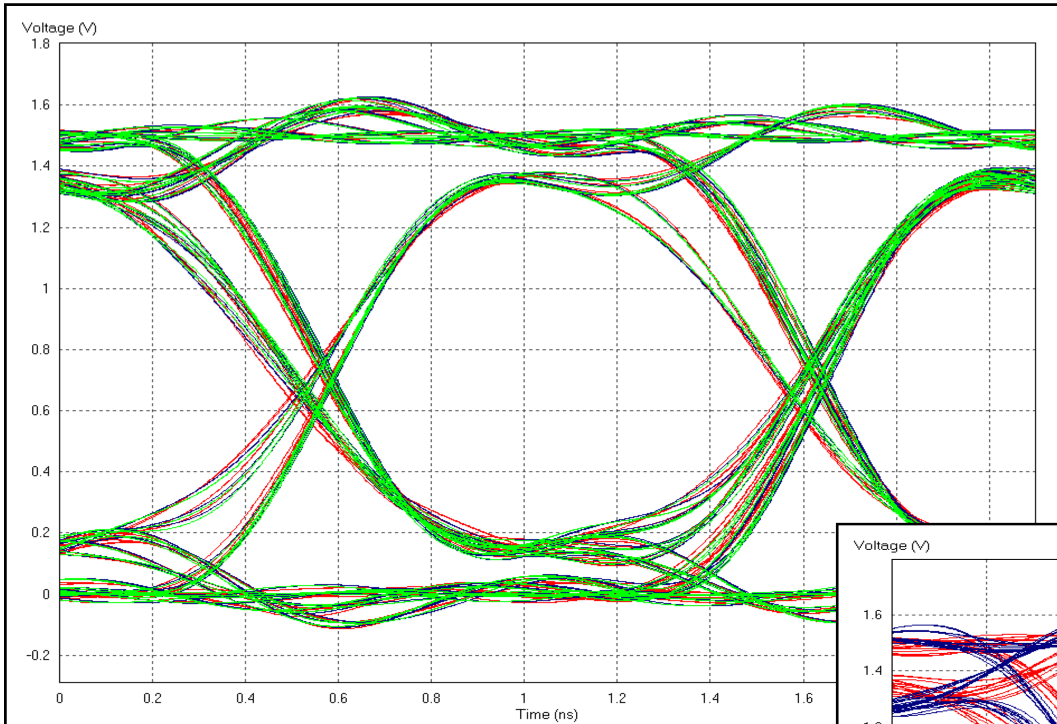
Model Type:

1-segment broadband, 2GHz

3-segment broadband, 2GHz

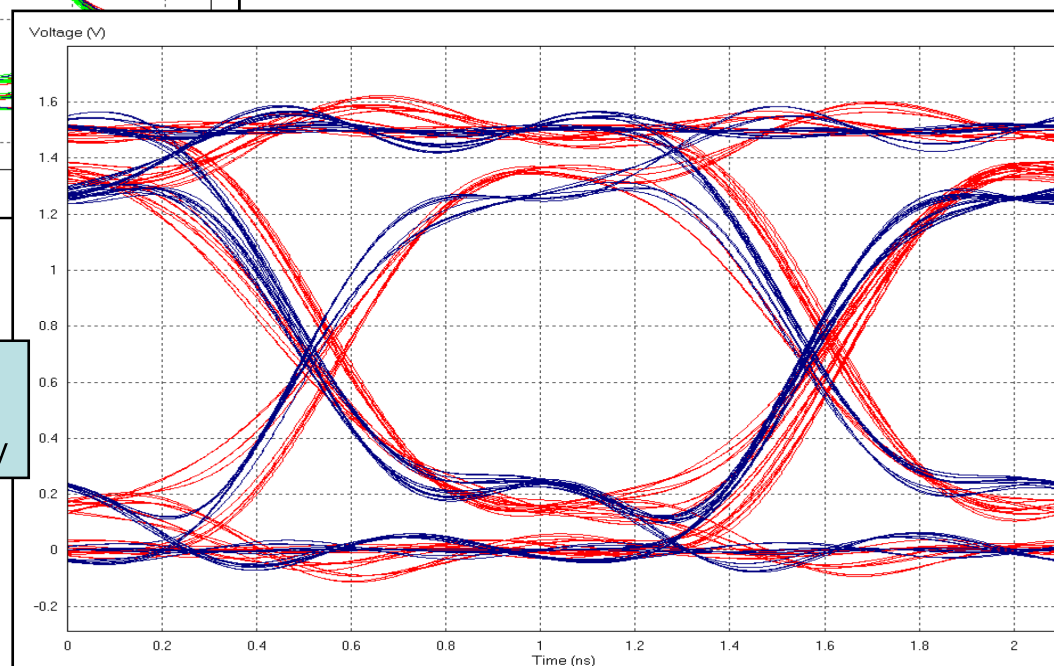
Eye Diagram at the Load

F_{switch}= 400 MHz , T_{rise}= T_{fall}= 100 ps



Single-segment model
{30, 100, 200} MHz

-- Similar eye openings
-- A bit more jitter with lower extraction frequency

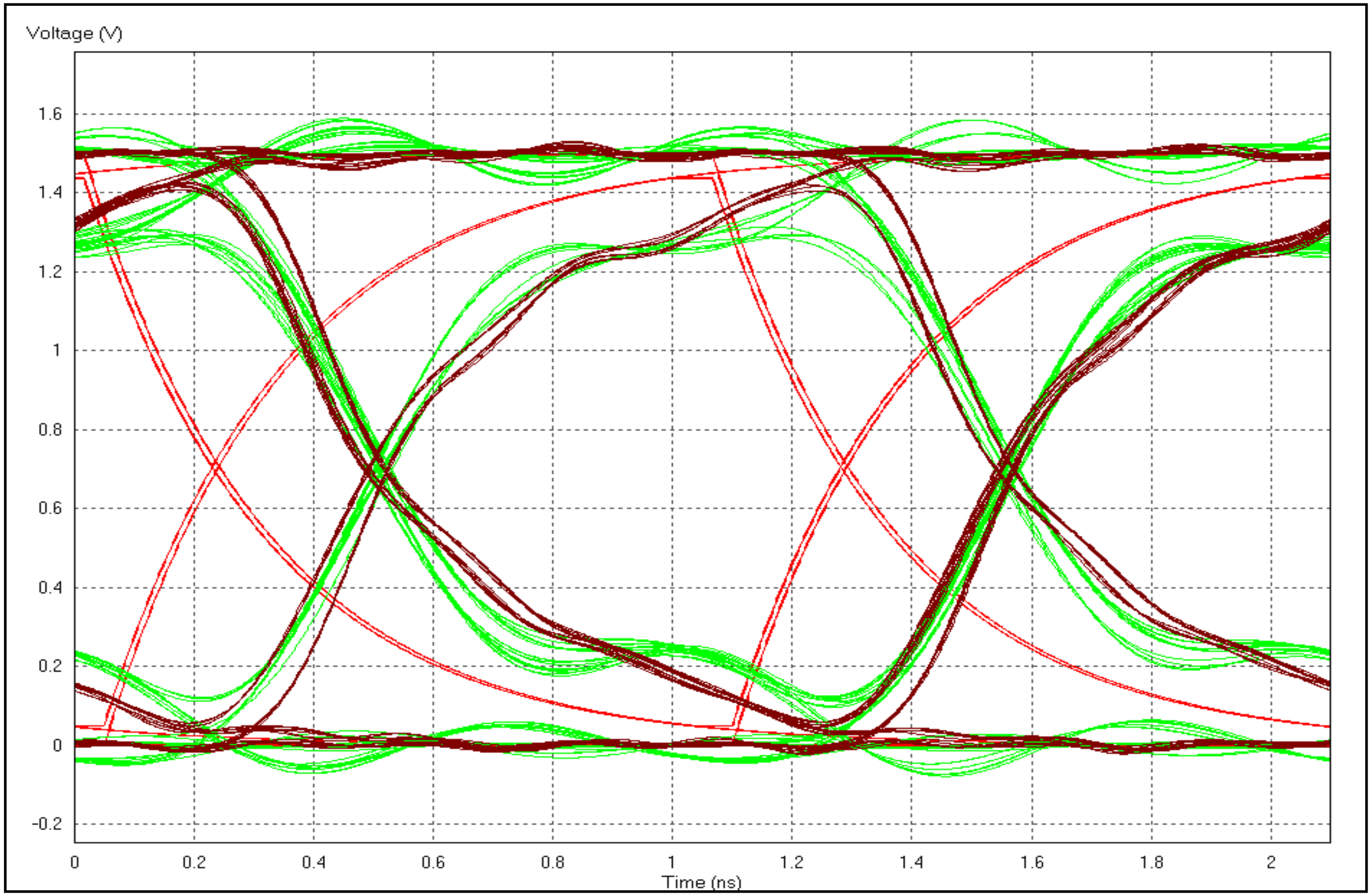


-- Very similar eye openings
-- Overshoot/Undershoot and ringback are very similar
-- Significantly more jitter with single extraction frequency

Single-segment model
30 MHz
broadband, 2GHz

Eye Diagram at the Load

F_{switch}= 400 MHz , T_{rise}= T_{fall}= 100 ps



<u>Model Type</u>:

None
1-segment broadband, 2GHz
3-segment broadband, 2GHz

-- Package model effects are quite dramatic
-- Similar eye openings for each broadband model
-- Overshoot/Undershoot and ringback are quite different
-- Similar jitter for each broadband model

Conclusions:

-- System noise performance differs for various types of package models and the conditions under which they are extracted

- -- Loop inductance, AC resistance, voltage droop, power bounce, eye diagrams and jitter are used as figure of merits for noise performance evaluation
- -- **Broadband data based, multi-segment models predict more realistic SI-PI performance with significant differences for DC single-segment models**

-- Extraction frequency affects models and SI-PI performance as expected

- -- RLC values vary as intuitively expected
- -- RLC values affect signal switching as expected and also affect power noise as might not be expected
- -- **Multi-segment broadband based RLCK models correspond best with full-wave S-parameter SI-PI performance predictions**

-- Lessons learned for system-level modeling and design

- -- **select appropriate package model type for signal bandwidths**
- -- **extract package models with adequate bandwidth**
- -- proper models enable efficiency of iterative simulation-based design improvements of for high performance processor and ASIC packages