OrbitIO Interconnect Designer

Cross-substrate interconnect pathway design and optimization from silicon through IC package to PCB

Cadence® OrbitIO™ interconnect designer revolutionizes the cross-substrate interconnect architecting, assessment, implementation, and optimization process by unifying IC, package, and PCB data in a single environment where signal-to-bump/ball assignment and connectivity/routing pathway scenarios are easily derived and evaluated in the context of the complete system prior to implementation. Full-system visualization and a unified data model enable rapid exploration and propagation of changes to adjacent substrates, providing instantaneous feedback on their system-wide impact. The OrbitIO interconnect designer helps the engineer or architect achieve the right balance of cross-substrate interconnect integration for optimal performance, cost, and manufacturability prior to implementation—resulting in fewer iterations and shorter cycle times.

Introduction

The OrbitIO interconnect designer helps design teams optimize device and system performance by providing a single environment for architecting, evaluating, and driving critical high-speed interfaces such as DDR3, DDR4, PCI Express® (PCIe®) Gen 3, USB 3.0, and others across the multiple substrates that comprise the system.

The OrbitIO interconnect designer is ideal for system architects, project leads, or individual designers responsible for developing the die-to-package or package-to-PCB interface, and coming up with the optimal combination of bump/ball configurations and signal assignments. It enables fabless semiconductor and systems companies to evaluate package route feasibility and to communicate a route pathway scenario to their package design team, whether it's an internal group or an outsourced assembly and test (OSAT) provider.

Benefits

- Anticipate and avoid downstream issues with early cross-substrate interconnect architecture design
- Significantly shorten the time to converge on the optimal die/package interface
- Utilize key PCB components to influence package ball pad assignments
- Better prediction of cost and performance using well-qualified design definitions
- Quickly generate design abstractions in response to marketing feasibility studies
- Clearly communicate design intent and route plan to external design resources
- Coordinate pin assignments for high-speed interfaces across multiple substrates
- Design tool compatibility with OSAT providers

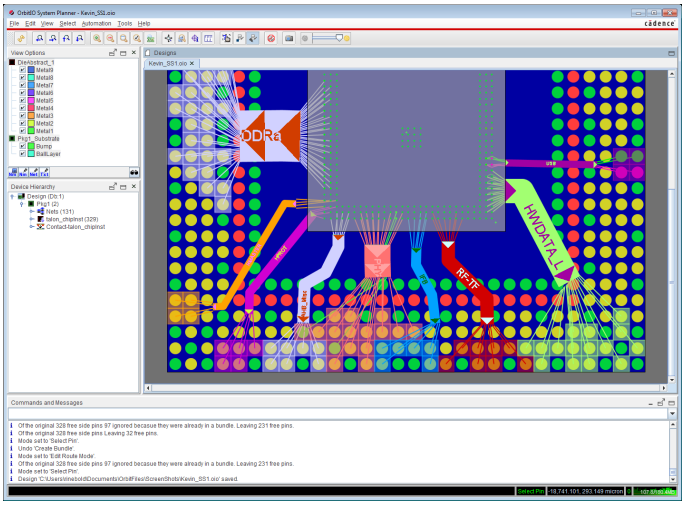

Figure 1: Rapid die/package route pathway scenario development and assessment in the OrbitIO interconnect designer

Features

Cross-substrate interoperability and optimization

The OrbitIO interconnect designer provides an environment capable of uniting design content from various sources for the purpose of interconnect pathway development and optimization, and communicating that data back to their respective implementation tools for completion. It's part of an overall cross-substrate solution that provides interoperability across a range of Cadence products.

Silicon data is exchanged with Cadence Innovus™ or Virtuoso® technologies using the open XML-based die abstract format, which provides a single-file exchange mechanism that conveys I/O planning-related content while protecting sensitive chip IP.

Package definitions and interconnect pathway architectures developed in the OrbitIO interconnect designer can be directly imported into Cadence SIP Layout to help expedite detailed package implementation. This methodology is of great value to companies working with external design resources as it removes ambiguity in communicating design intent and routing pathway scenarios. PCB-related interconnect architecture can be exchanged with Cadence Allegro® PCB Designer, and third-party tool support is provided using industry-standard formats, such as LEF/DEF, Verilog, and TXT/CSV.

System construction

An initial step in cross-substrate optimization is establishing the physical relationships between the die, package, and PCB. The OrbitIO interconnect designer provides an automated hierarchy system that manages these relationships while maintaining the individual integrity of each substrate, including items like constraints and layer stack-up.

A common application of the OrbitIO interconnect designer is to use key components and connectors on the PCB to drive package ball pad (and flip-chip bump) assignments in support of a bottom-up flow for system compatibility. These components can also include route fan-out patterns, enabling a greater level of specification in route ordering and sequencing.

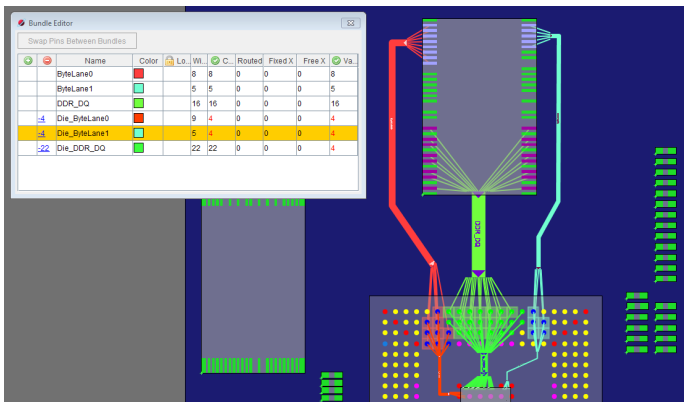

Figure 2: PCB-driven package and die assignment

"Big picture" pathway development

Conventional design methodology has been a serial top-down approach, where the silicon drives downstream connectivity with minimal upstream feedback, and with data communicated using static spreadsheets. Growing functional integration at both the die and package level, combined with the latest generation of multi-gigabit parallel bus interfaces like DDR3 or DDR4, requires careful architecting and implementation coordination across all substrates. Such complexity leaves little room for inefficient and error-prone methodologies.

The OrbitIO interconnect designer's environment enables rapid exploration and evaluation of connectivity architectures, providing immediate feedback on the impact to adjacent devices and substrates. It can be used for early feasibility through detailed implementation, making use of the best available data or creating devices on the fly when needed. Silicon considerations can guide downstream connectivity in a top-down flow, or PCB-level considerations can drive upstream connectivity in a bottom-up flow. The OrbitIO interconnect designer's flexible and adaptable environment also supports a middle-out flow where package-level considerations can simultaneously drive die and PCB connectivity.

As a flexible exploration environment, the OrbitIO interconnect designer has the ability to work with an existing netlist, without a netlist, or as in most cases, with a partial netlist. Nets are automatically propagated between substrates as result of the assignment and optimization process.

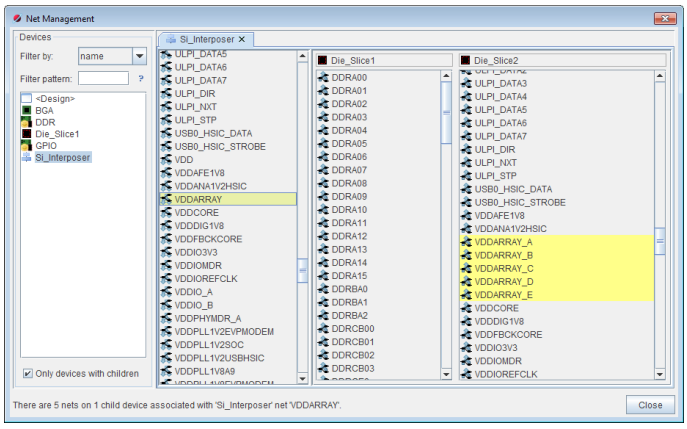

Figure 3: Net mapping example: Several nets on a die mapping to one net on the interposer

Functionally, logic relationships are addressed through net management, which provides a correlation engine for mapping nets between substrates, even when the names are different. Regular expressions are used to define patterns for automatic mapping, or a simple drag-and-drop function can be used for interactive mapping. Many-to-one mapping scenarios, common among power and ground nets, are also addressed.

Pin assignment and management

The ability to work at the pin level with or without a netlist is a key aspect of early pathway development. The OrbitIO interconnect designer's robust pin personality capability enables allocation of pins based on common characteristics or pin types, and can range from a simple power-signal allocation to complex scenarios that specify down to the byte-lane level.

Besides helping with visualization, pin personalities are used to establish the desired signal, power, and ground (SPG) ratios to ensure proper power supply and return paths. The OrbitIO interconnect designer can automatically distribute pin attributes based on a target SPG ratio, or patterns of attributes can be copied and propagated onto other pins to create a repeating pattern.

In situations where interconnect architecture might start with a previous generation of a design, the OrbitIO interconnect designer provides a synthesis function to automatically assign personalities based on existing net names. The nets can then be removed, leaving the attributes and a convenient starting point for a new design.

Logic definition and management

A key differentiator for the OrbitIO interconnect designer is the ability to maintain the individual integrity and extents of each substrate while providing a complete system view and interoperability. In comparison, other approaches define a monolithic representation of die, package, and PCB using a single massive layer stack-up. Such stack-ups lead to numerous issues related to net names, constraint management, and substrate boundaries.

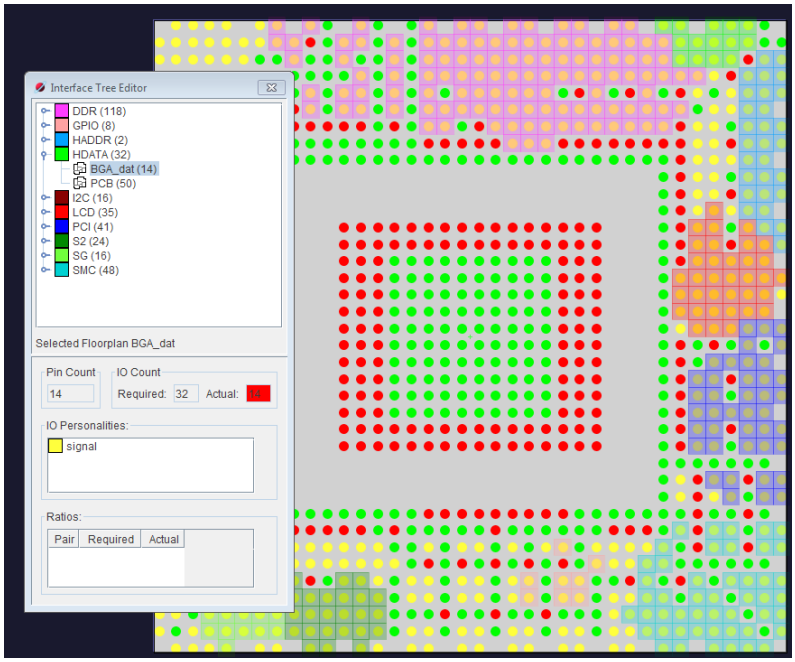

Figure 4: Early interface exploration without the die

Route pathway exploration and feasibility analysis

One of the key benefits of the OrbitIO interconnect designer is the ability to define and evaluate a route pathway scenario, then to communicate those results to SIP Layout for detailed constraint-driven implementation. This route architecture is accomplished by starting with the bundles defined during connection optimization and using them to sketch the desired flow of routing between devices. Layer assignments are specified per bundle and color coded for visualization, while the width of a bundle is representative of the number of nets it contains, indicating the relative space required.

The OrbitIO interconnect designer feasibility functions include a route engine that quickly generates escape routes from bumps and balls pads to help evaluate layer requirements and assignment quality. Linked with the route engine is a sequence editor to control the flow and ordering of connections into the bundle. This combination enables rapid route pathway evaluation, and editing, resulting in a well-qualified route plan that can be passed with high confidence of completion to SIP Layout for detailed implementation.

Pathway Design Flow Support

- PCB-driven package BGA ball map design and optimization, including PCB schematic symbol generation (DE-HDL support)
- IC-driven BGA ball map design and optimization

- Cross-substrate IC bump array and package ball definition and optimization with route pathway design including PCB
- Early package start-from-nothing BGA ball map creation
- Package BGA-driven IC bump array design and optimization
- Package BGA ball map-based design and optimization targeting multiple PCBs (variants-based design)

Integration

- Chip data: Die Abstract, Library Exchange Format (LEF)/Design Exchange Format (DEF), Verilog, and TXT/CSV files
- Package data: Direct data exchange with Cadence SiP, AIF, and TXT/ CSV files
- PCB data: Cadence Allegro PCB and other popular systems

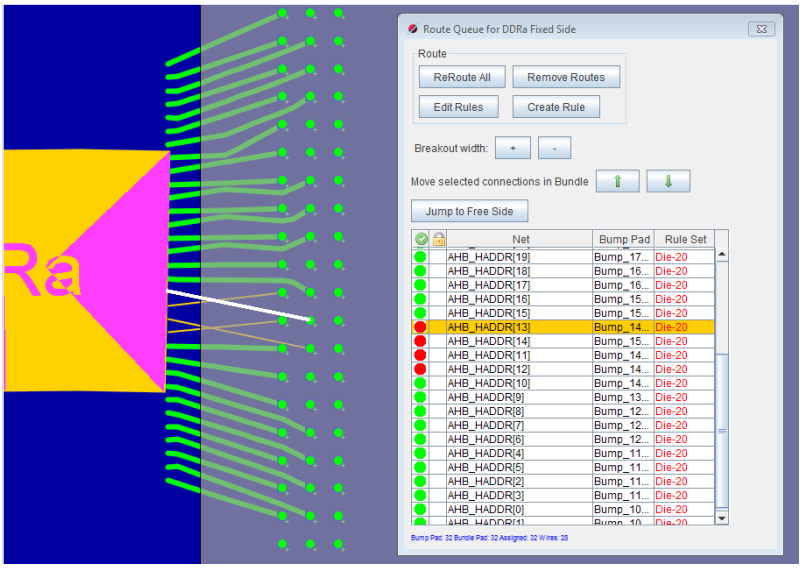

Figure 5: Route sequencing and feasibility