Using IBIS-AMI in the Modeling of Advanced SerDes Equalization for Serial Link Simulation

CDNLive Boston
August 2013

Mark Marlett and Mahesh Tirupattur, Analog Bits
Ken Willis and Kumar Keshavan, Cadence Design Systems

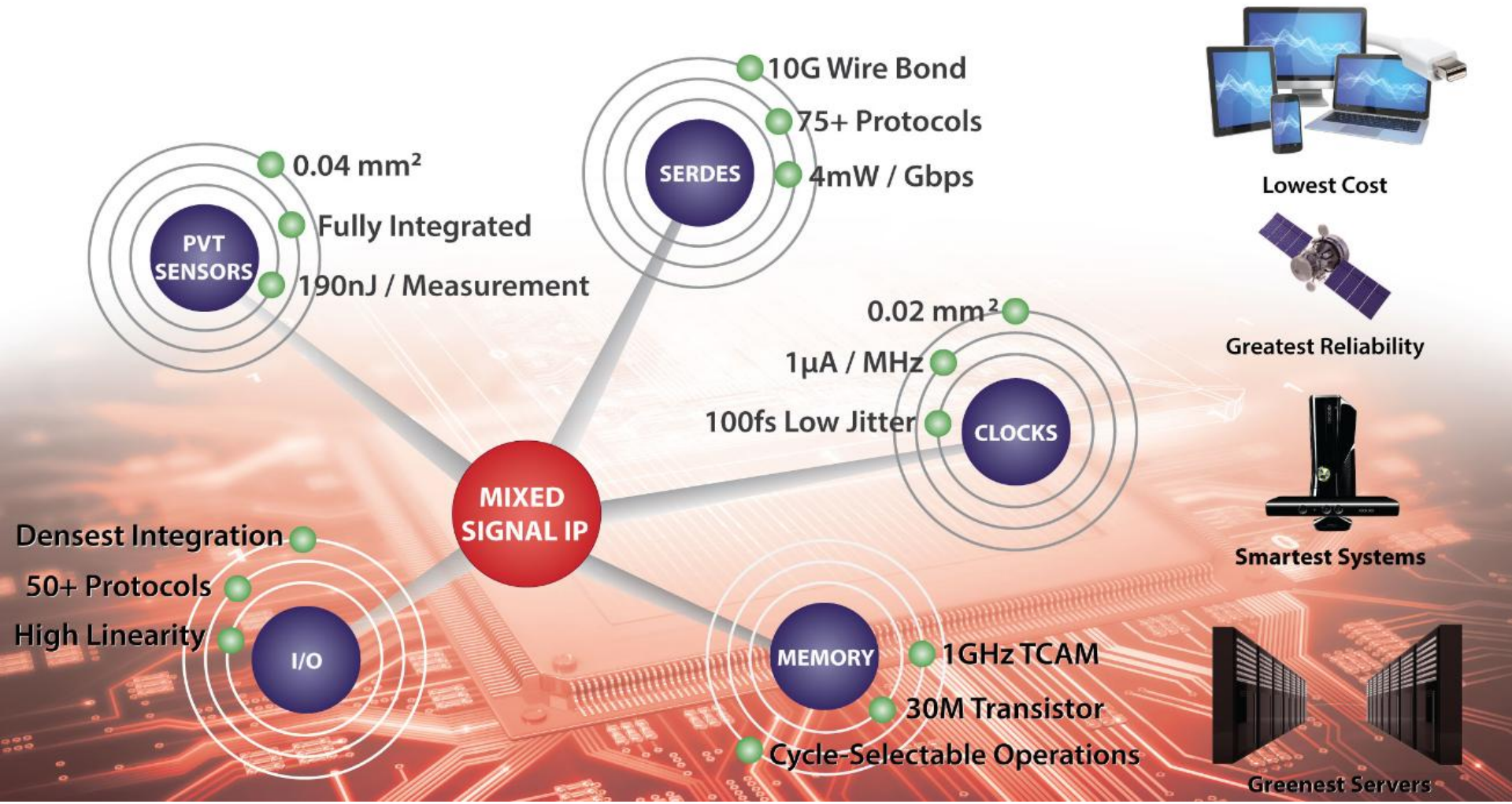
Agenda

- Introduction
- Motivation for AMI modeling
- Why channel simulation?
- What is IBIS-AMI?
- Case study > Analog Bits SerDes

Agenda

- ***Introduction***
- Motivation for AMI modeling
- Why channel simulation?
- What is IBIS-AMI?
- Case study > Analog Bits SerDes

Broadest Portfolio of Differentiated IP
Billions in Silicon



Lowest Power SERDES

- Multi-Rate Multi-Protocol SERDES
  - Lowest power & latency
  - Smallest area
  - Programmable for numerous channel environments
- SOC applications

FPGA

Consumer Cables

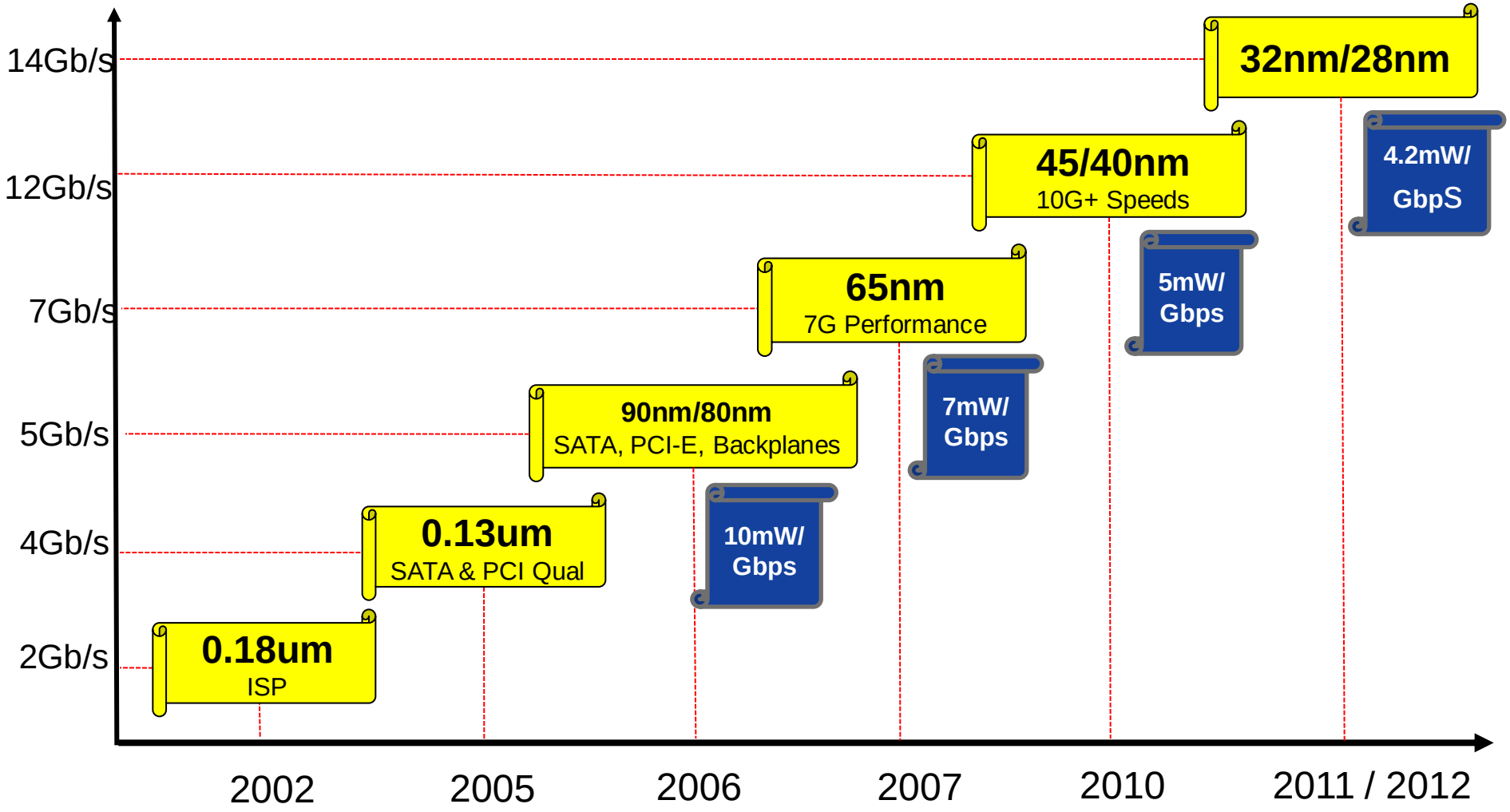
Mobile Computing

Supercomputers & Communications

Flat Panel Display

10 Years of SERDES Track Record

1st Time Right in over 10 processes

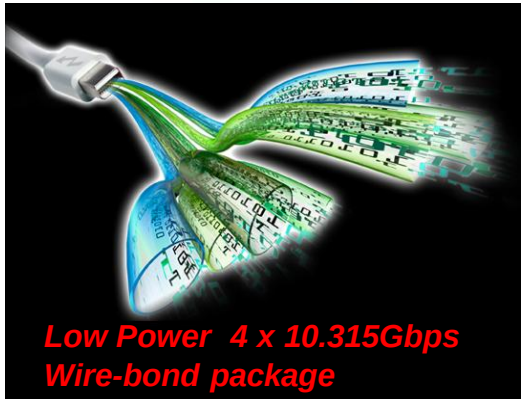


SERDES differentiates Networking to Consumer SoCs

Modern Fanless PC Graphics Card
x16 PCI Express SERDES Pixel Class PLLs,
Low Jitter X-tal oscillators and multiport RAMs

V-by-One SERDES in 3D Display TV's

THUNDERBOLT.



Low Power 4 x 10.315Gbps
Wire-bond package

100Terabits/sec. Supercomputer
28 SERDES implemented in 7 Quads
27 chips in board, 36 boards in chassis
Measured Bit Error Rate <10^{-23}

Multi-core processor with
72 Lanes of 10G+ SERDES under 3 sq.mm
DDR3 IOs and Clocking IPs

cadence®

Agenda

- Introduction
- ***Motivation for AMI modeling***
- Why channel simulation?
- What is IBIS-AMI?
- Case study > Analog Bits SerDes

Analog Bits Motivation for AMI

- Strong demand from chip customers to provide AMI models for SerDes IP
  - Considered part of doing SerDes IP business today
  - Systems customers of those chips strongly demand AMI to support simulation efforts
- Enables up-front feasibility analysis with customer channels during pre-sales phase
- Enables in-house system simulation for package and test board designs

Why Analog Bits partnered with Cadence/Sigrity for AMI

- Technical Experience
  - IBIS-AMI spec driven by Dr. Kumar Keshavan of Cadence in 2007
- Strong AMI IP Library base to work from
  - Many top-level modules for SerDes equalization could be leveraged
  - Accelerates turnaround and reduces time-to-customer
- Spirit of partnership
  - Close collaboration by Sigrity with Analog Bits engineering team

Agenda

- Introduction
- Motivation for AMI modeling
- ***Why channel simulation?***
- What is IBIS-AMI?
- Case study > Analog Bits SerDes

Why is Channel Simulation + AMI required?

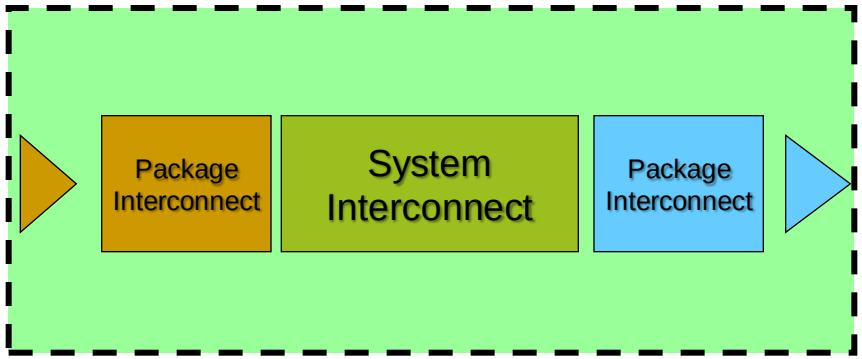
- Multi-gigabit serial links need to pass LOTS of data traffic to give reliable eye diagrams
- Multi-gigabit serial links need to pass LOTS of data traffic to provide enough samples to accurately predict BER
- Multi-gigabit SerDes devices often utilize adaptive equalization, which need to pass LOTS of data traffic before they stabilize and lock in
- Data rates have risen from 2.5 to 25Gbps in about 10 years
- Future designs targeting 400Gbps to 1Tbps

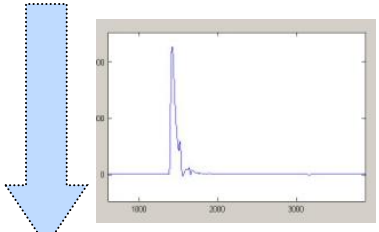
- *To accurately simulate multi-gigabit serial links, you need to simulate very large bit streams with very fast and accurate equalization models*

Channel Simulation Provides Ultra High Capacity

- Focuses on a single Rx
- Analog channel is exercised in Spice to produce an impulse response
- Impulse response is convolved with the bit stream to produce raw waveforms

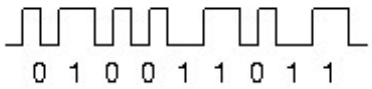
- Can simulate millions of bits in minutes
- Supports AMI models for EQ

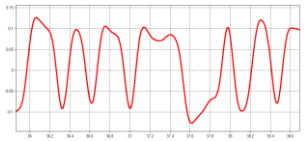




impulse response

Channel Simulator





Agenda

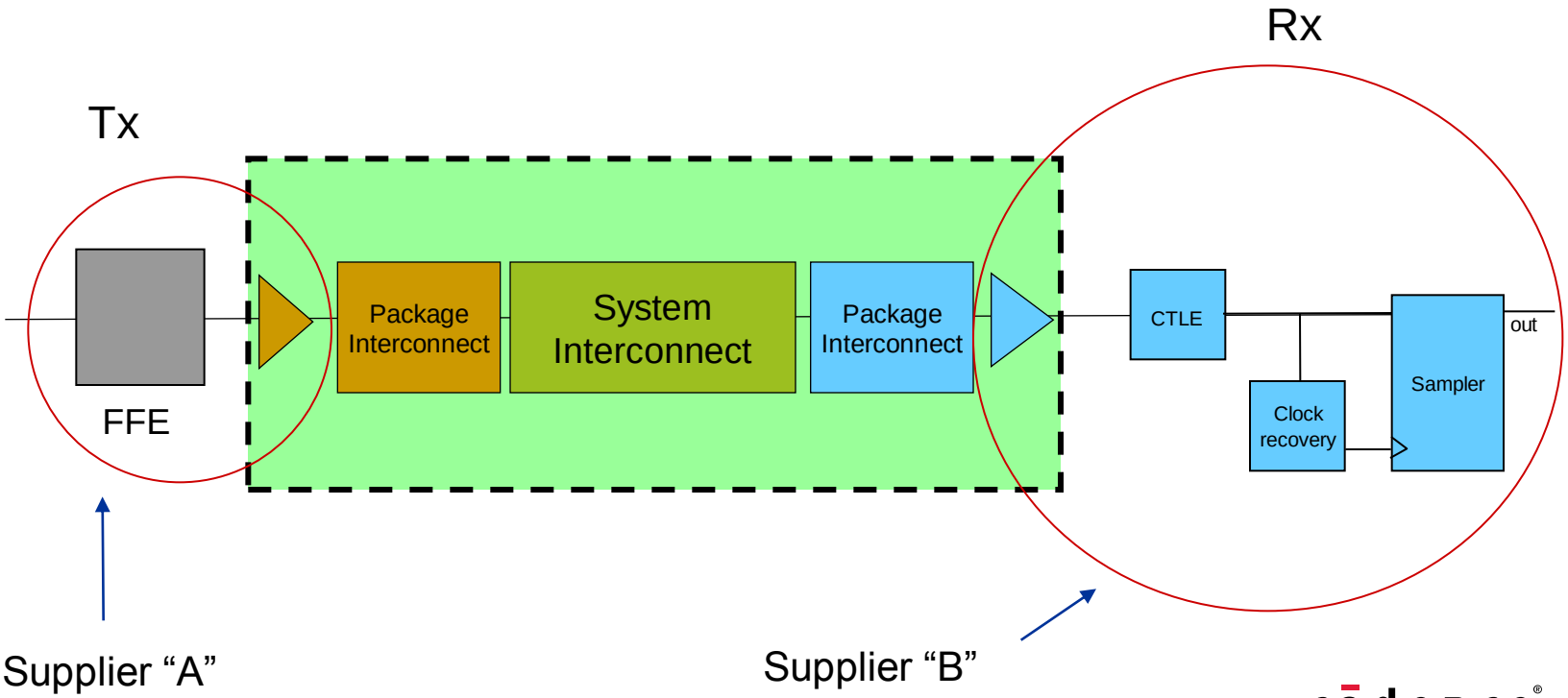
- Introduction
- Motivation for AMI modeling
- Why channel simulation?
- ***What is IBIS-AMI?***
- Case study > Analog Bits SerDes

AMI > Algorithmic Modeling Interface

- Extension made to IBIS in 2007
- Enables executable, software-based, algorithmic models to work together with traditional IBIS circuit models
- Enables SerDes adaptive equalization algorithms to be modeled and used during channel simulation

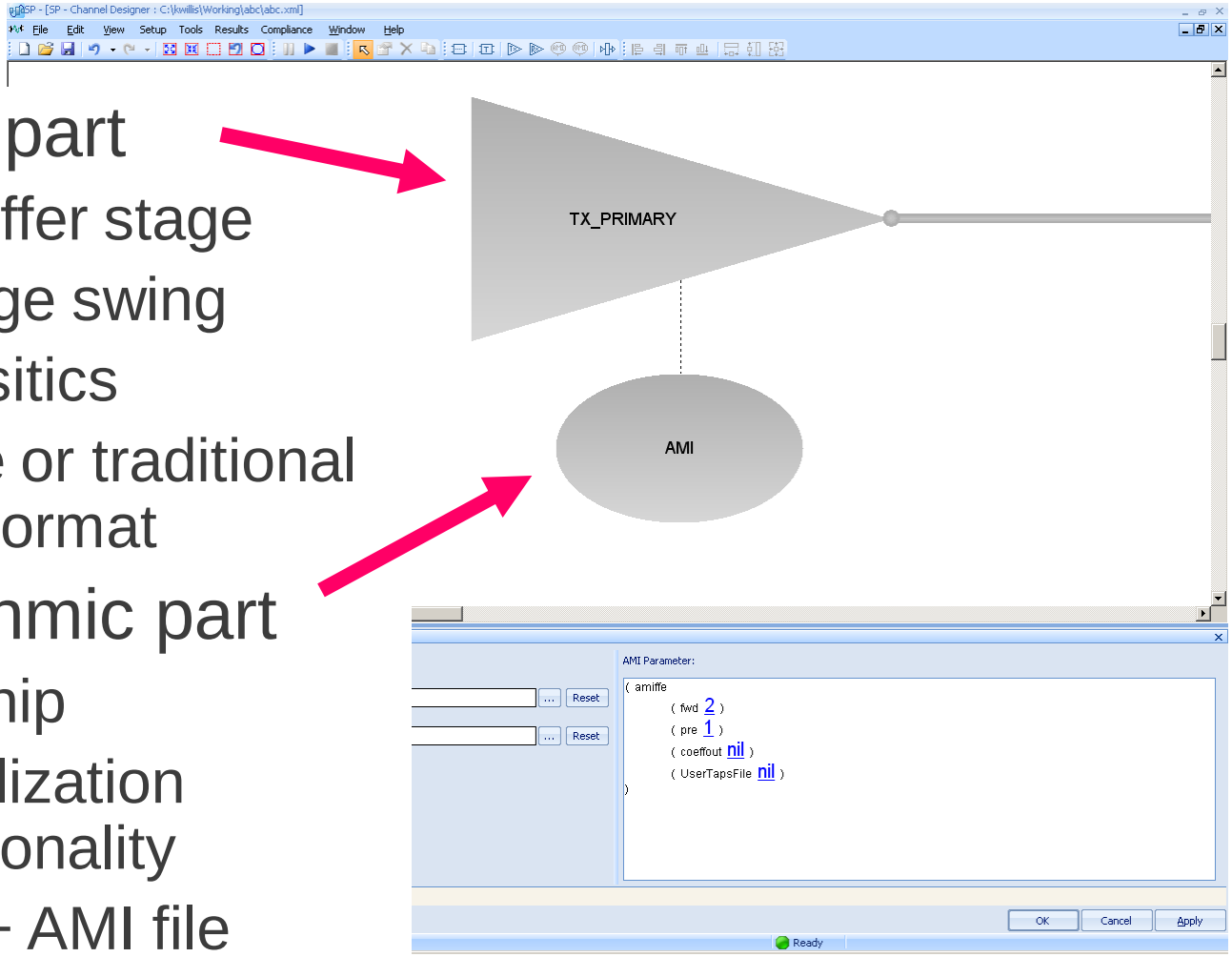
Motivation for AMI

- The intent of IBIS-AMI is to enable plug-and-play simulation compatibility between SerDes models from different suppliers, in a standard commercial EDA format



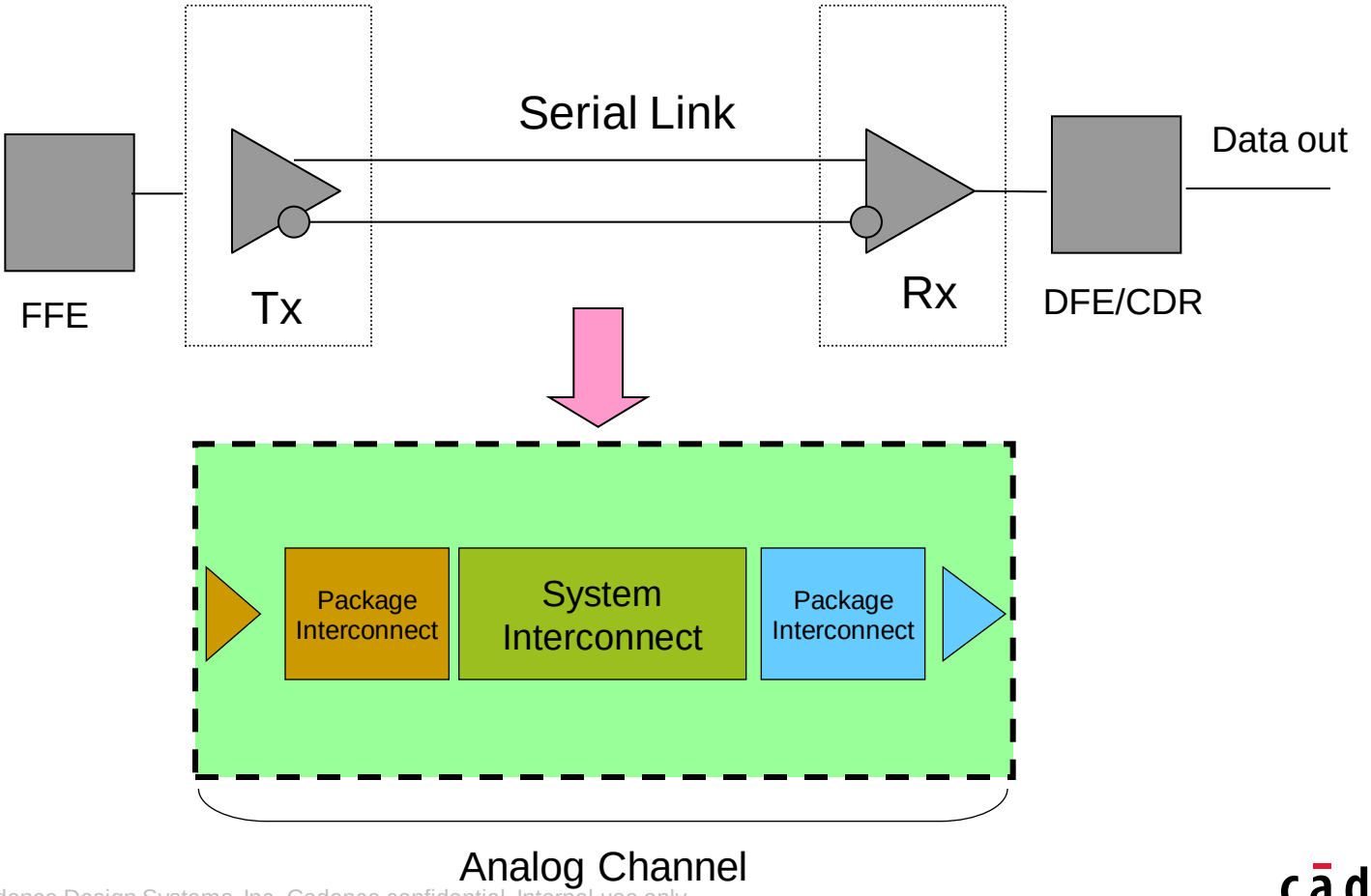
IBIS-AMI Model Sub-Components

- Circuit part
  - IO buffer stage
  - Voltage swing
  - Parasitics
  - Spice or traditional IBIS format
- Algorithmic part
  - On-chip
  - Equalization functionality
  - DLL + AMI file

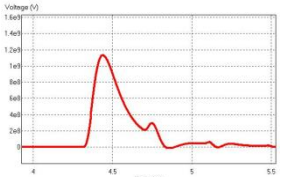


Characterizing the Analog Circuit

- Analog circuit part of channel separated from algorithmic EQ



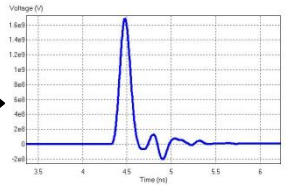
APIs in IBIS-AMI Modeling



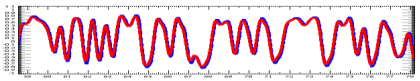
Impulse Response

Model input parameters

AMI_Init
-Initialize filter
- Setup Data Structures

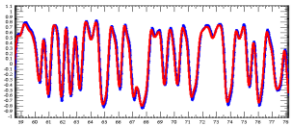


Modified Impulse Response



Continuous waveform

AMI_GetWave
-Waveform Processing
-Clock and Data Recovery



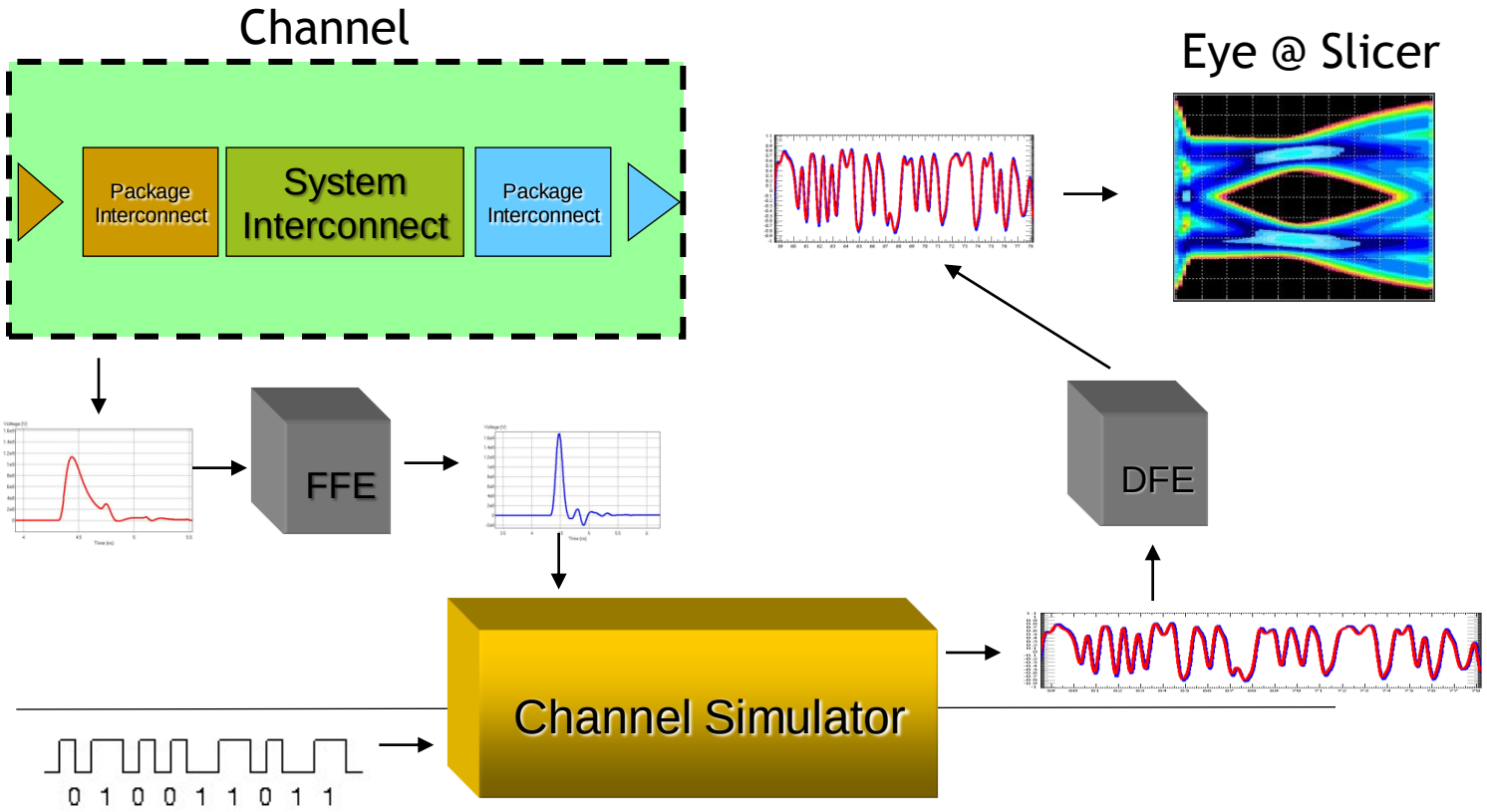
Equalized waveform

Clock tics

AMI_Close
-Free memory etc.

- AMI_Init for “one-time adaptive EQs
- AMI_GetWave for “real-time” adaptive EQs

IBIS-AMI and Channel Simulation



Agenda

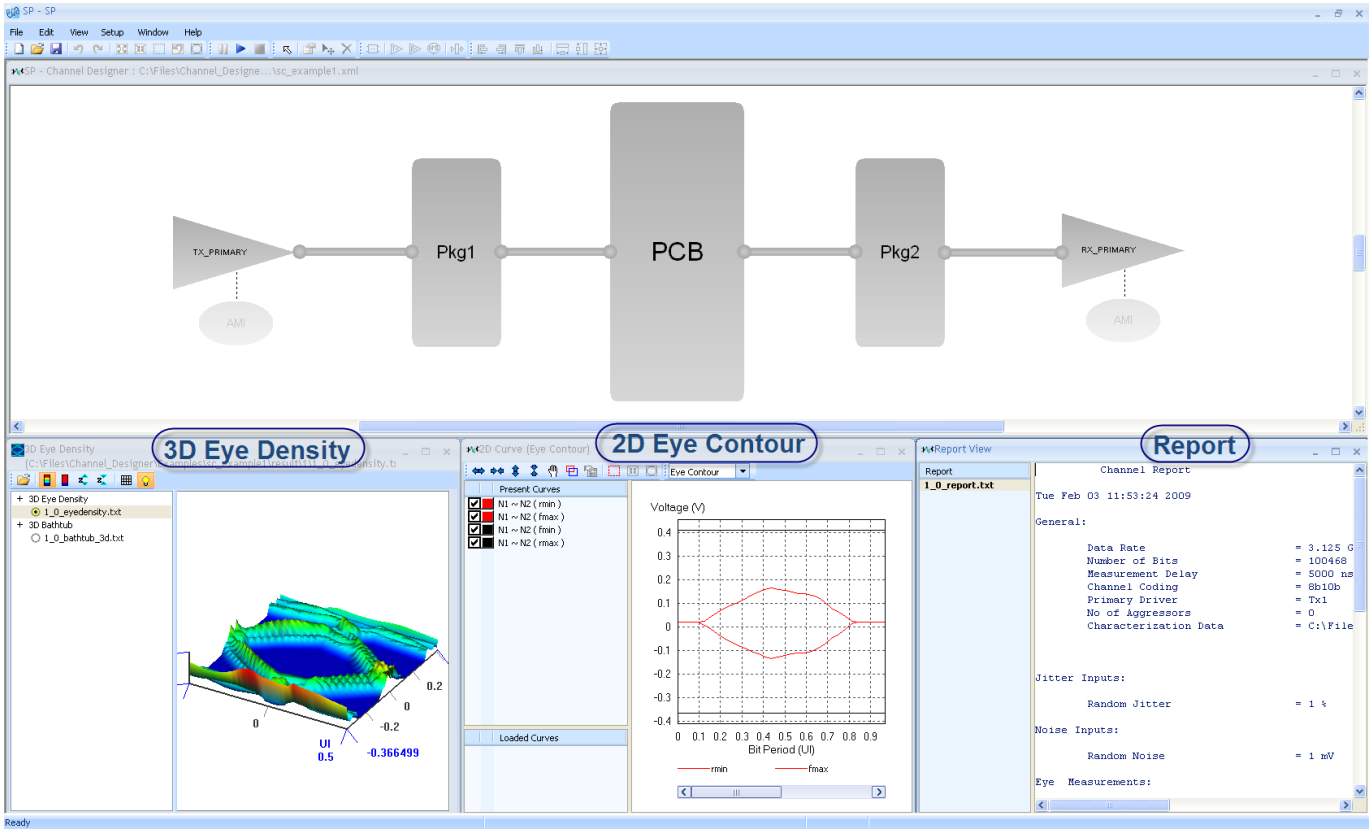
- Introduction
- Motivation for AMI modeling
- Why channel simulation?
- What is IBIS-AMI?
- ***Case study > Analog Bits SerDes***

Case Study > Analog Bits Transmitter

- Tools
- Transmitter equalization
- Channel simulation vs. transistor-level HSpice simulation
- AMI model for equalization vs. transistor-level Spice

Cadence's SystemSI – Serial Link Analysis

- Provides a comprehensive environment for the accurate assessment of high speed serial links to ensure robust IC package and PCB implementations.



Cadence's Algorithmic Model IP Library

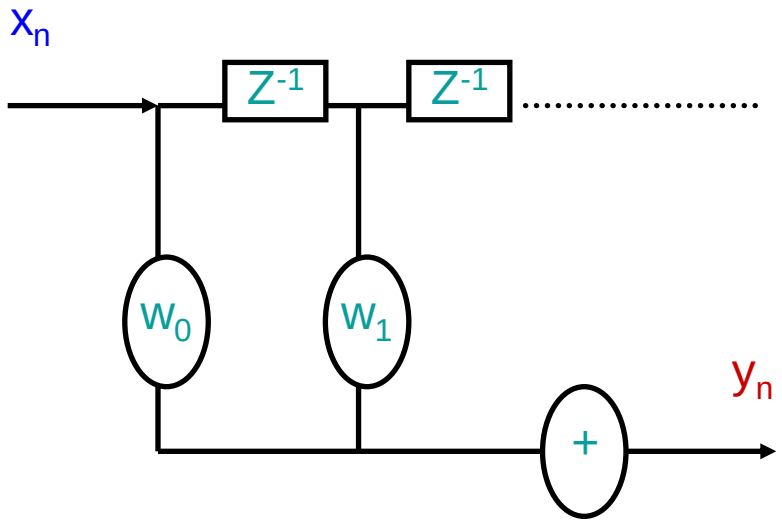
- FFE – Feed Forward Equalizer
- CDR – Clock and Data Recovery
- CTLE – Continuous Time Linear Equalizer
  - Standard
  - Adaptive, with integrated CDR and DFE
- DFE – Decision Feedback Equalizer
  - Standard
  - Non-linear with "lookahead" gain
- AGC – Automatic Gain Control

Custom AMI model development available
Source code available as baseline
Fully IBIS-5.0 compliant

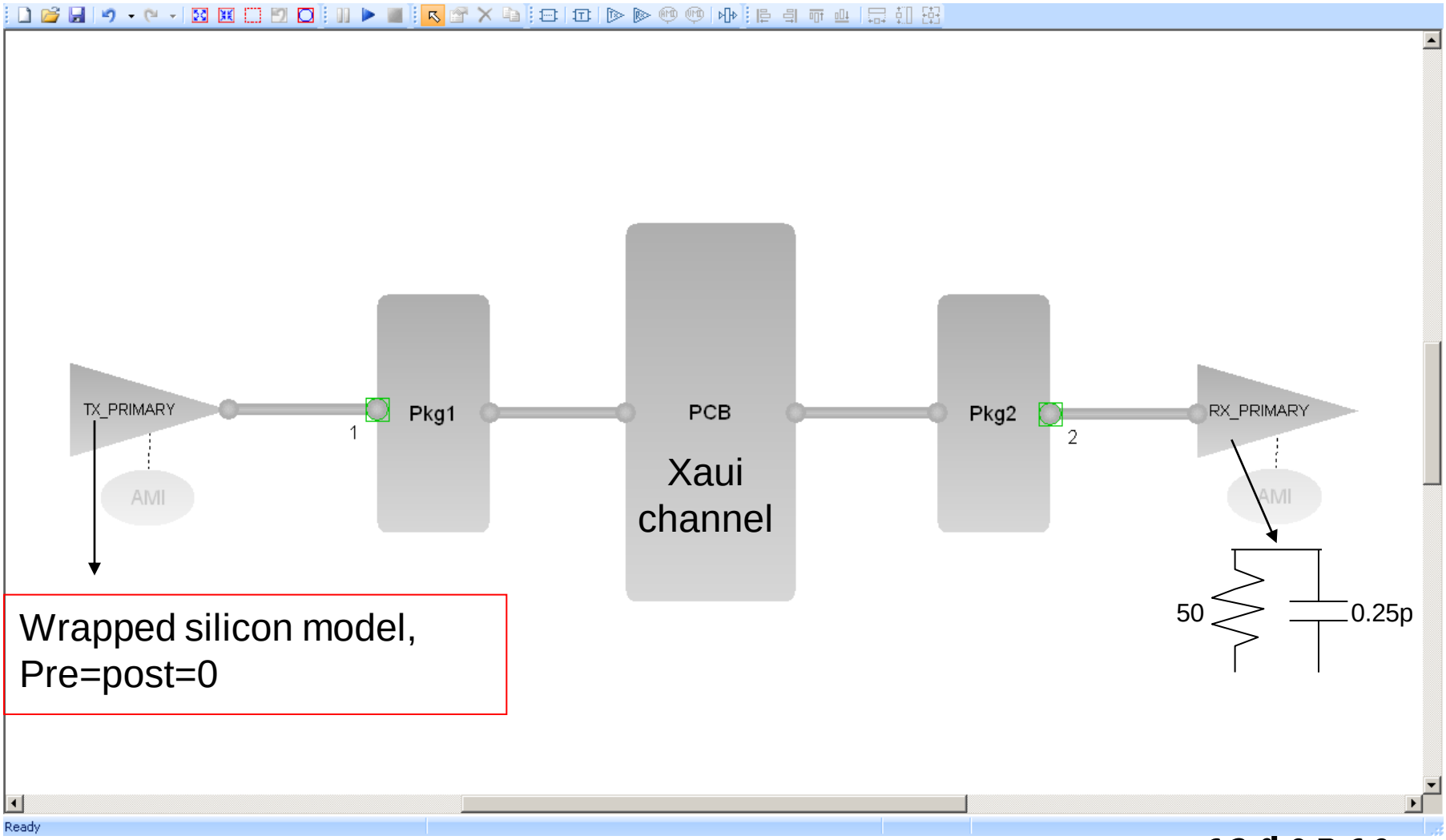
cadence

Transmitter Equalization - FFE

- FFE stands for *Feed Forward Equalizer*
- Typically used in Tx
- Mathematically
  - $y_n = \Sigma\, w_i * x_i$
  - Xn – input
  - Yn – output



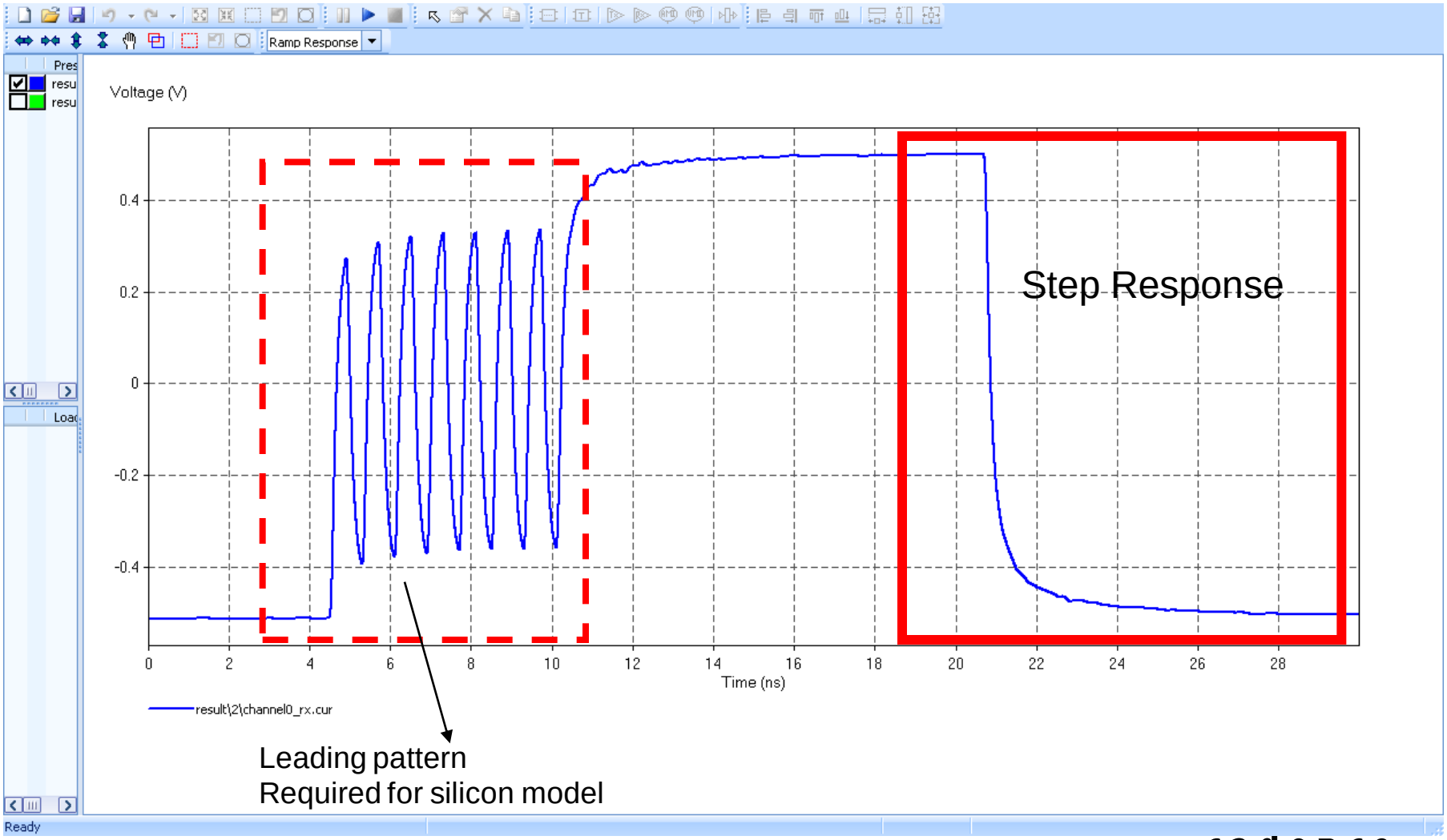
Test System: PCB=Xaui channel
Rx= simple terminator



Wrapped silicon model,
Pre=post=0

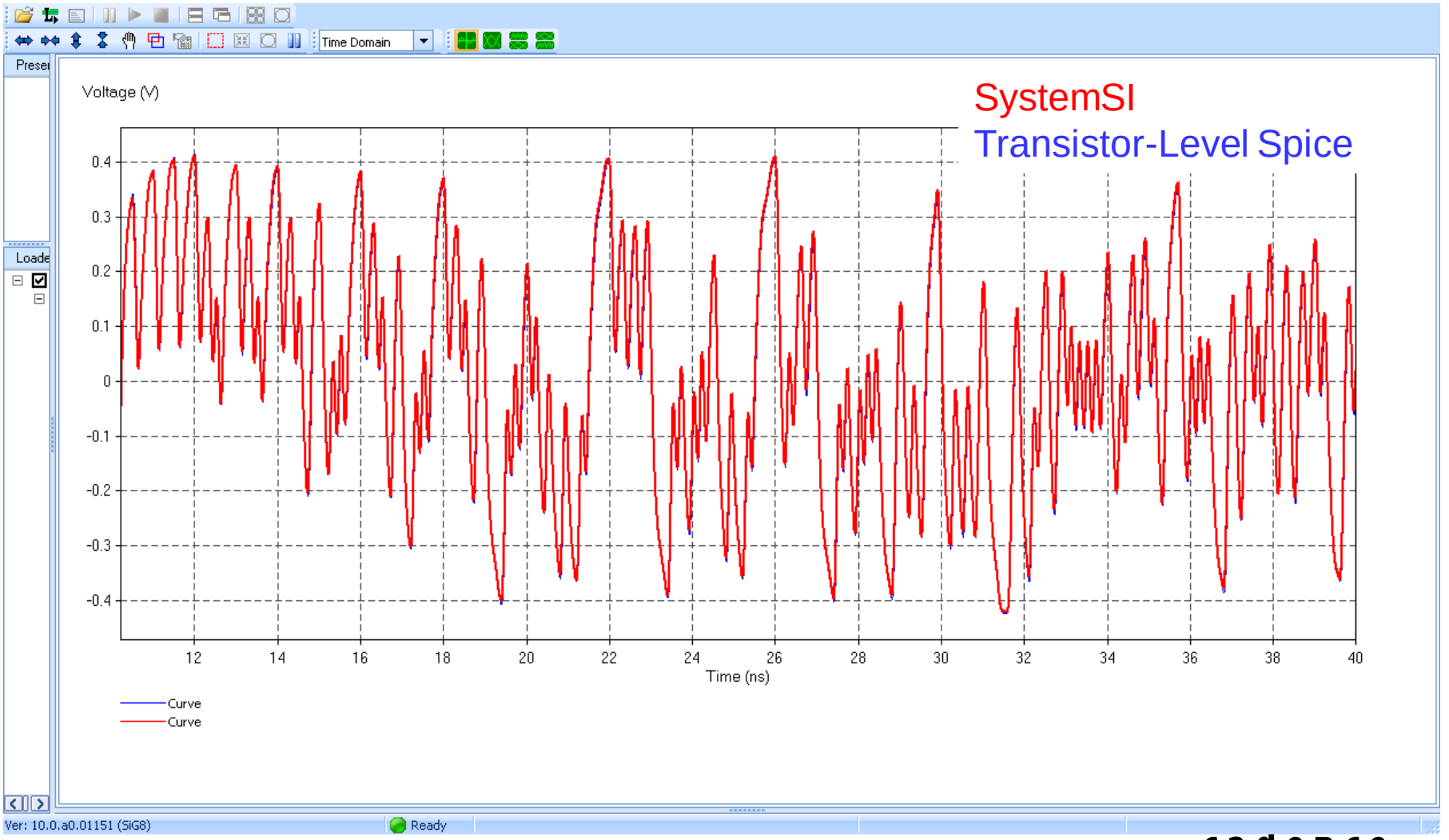
cadence

Characterization Step Response (Tx pre=post=0)



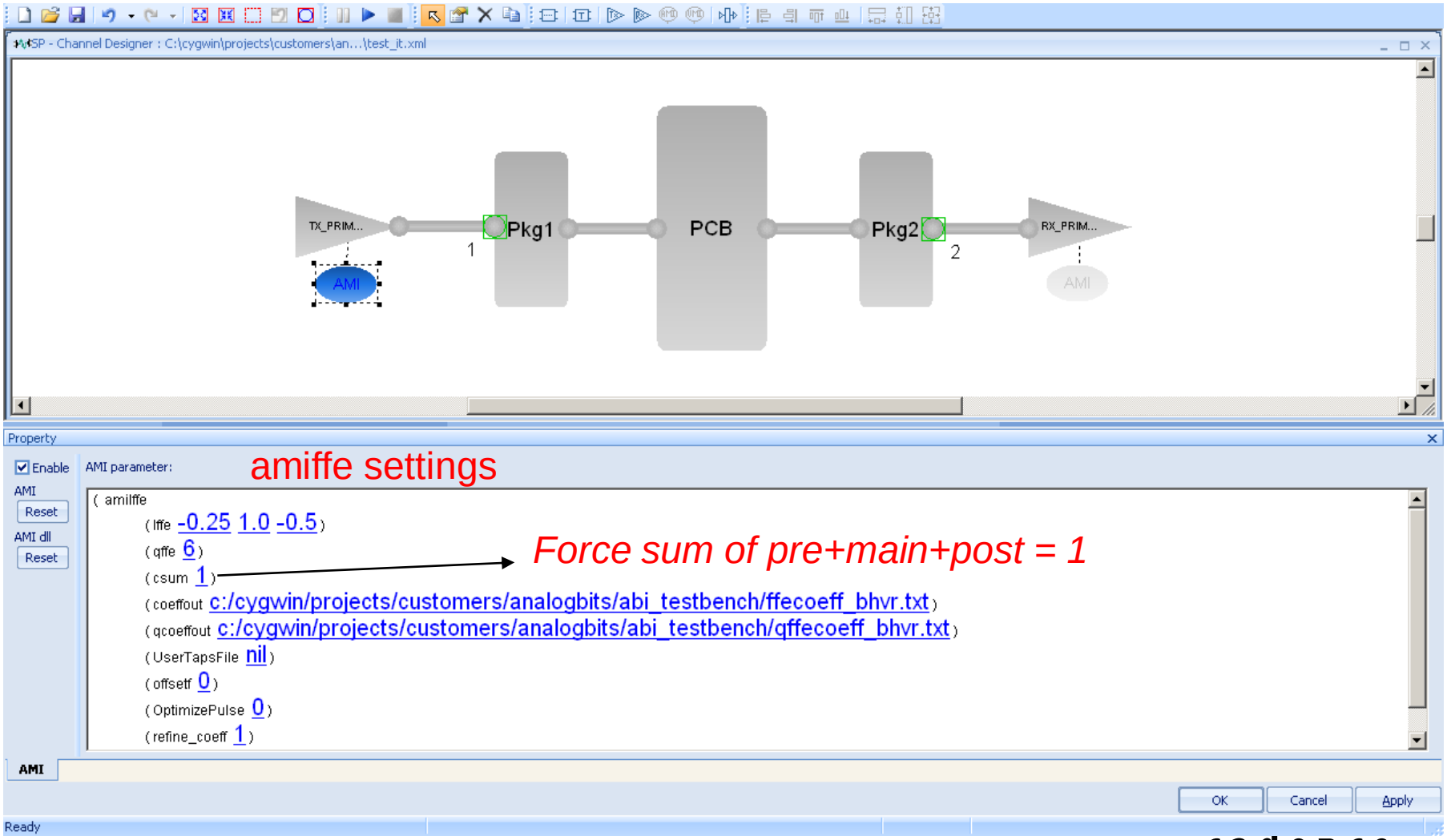
cadence

Channel Simulation vs. Transistor-Level Spice
10 Gbps – PRBS 21



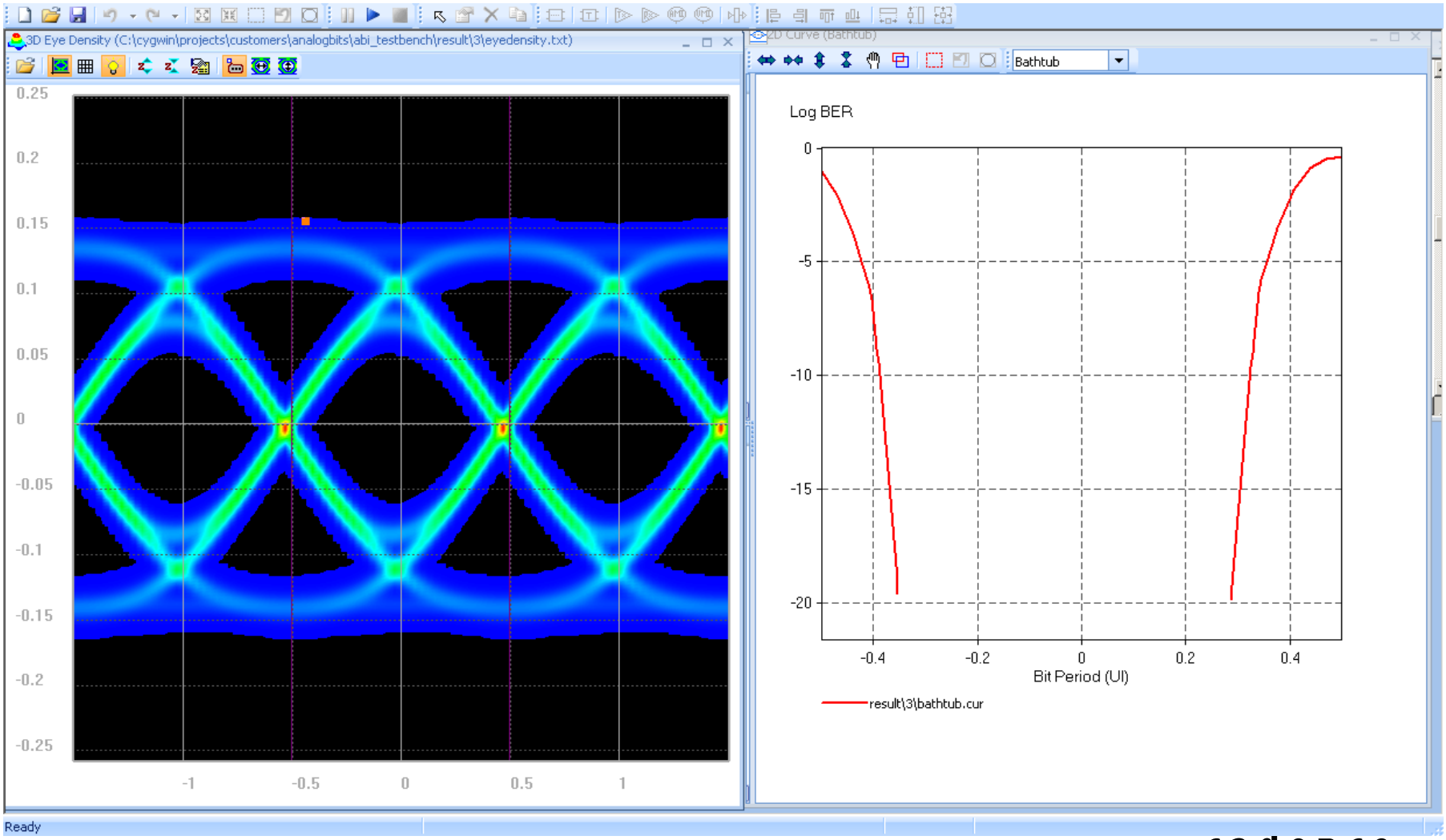
cadence

Test System: PCB=Xaui channel
Rx= simple terminator
Tx= behavioral Spice circuit + AMI for FFE



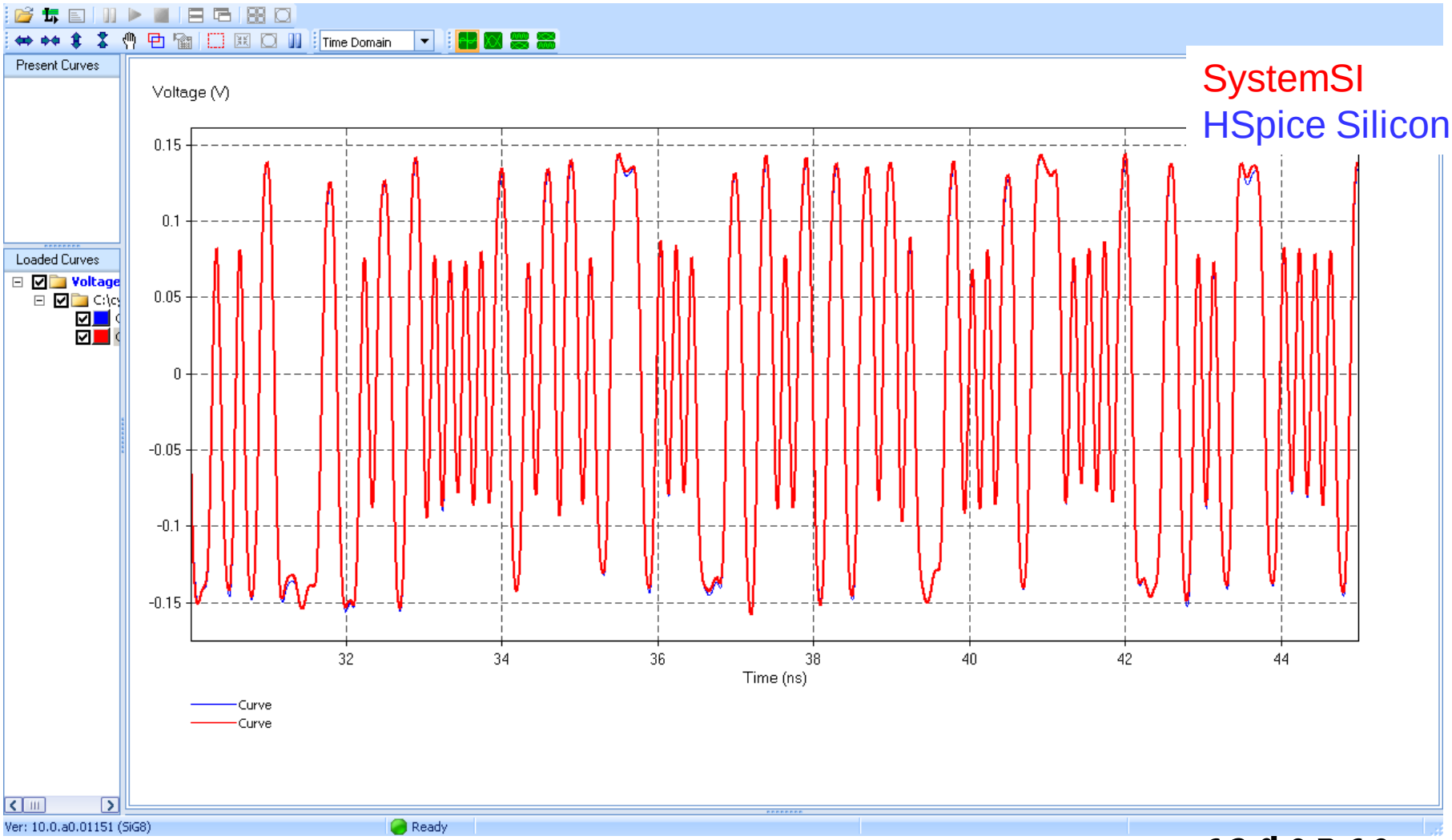
cadence

Test System Results



cadence

SystemSI vs. Transistor-Level Spice with Tx Equalization

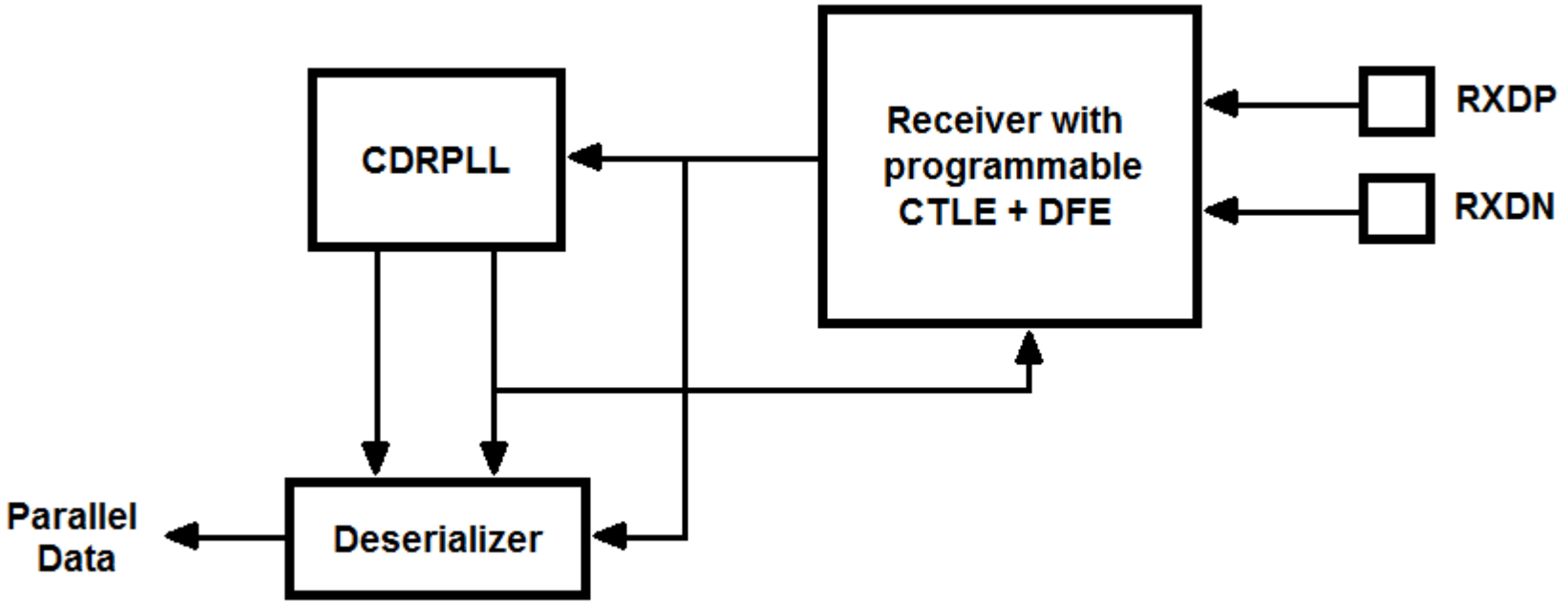


cadence

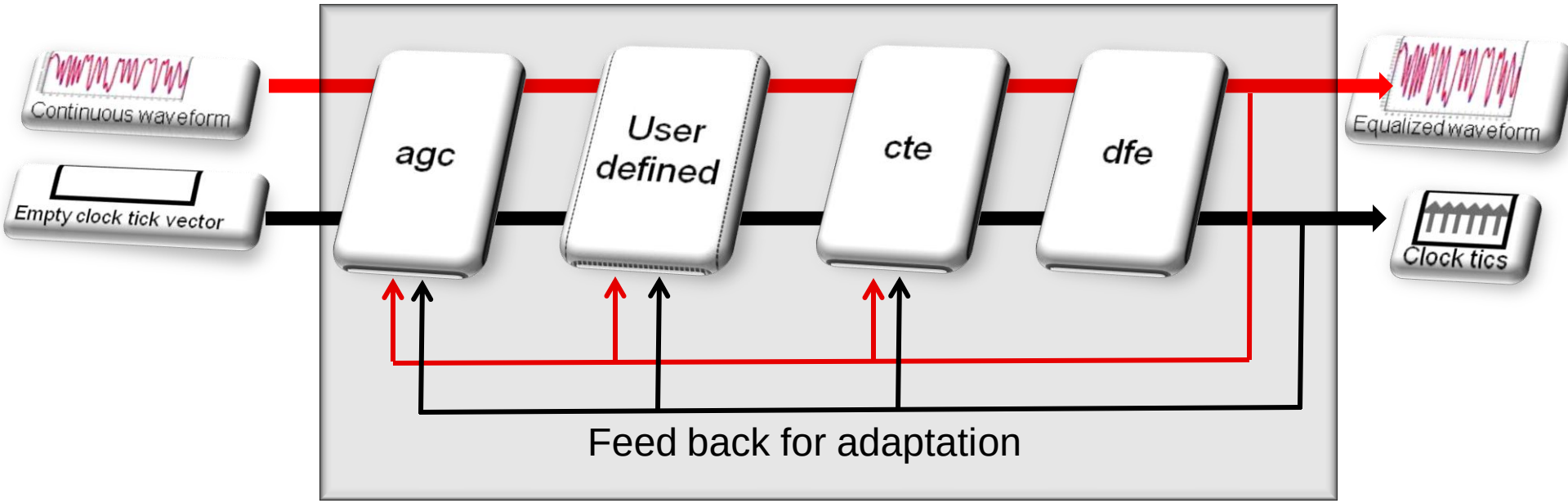
Case Study > Analog Bits Receiver (Rx)

- Rx is considerably more complex
- Novel Rx architecture
  - Nonlinear Rx with feedback
  - Includes
    - Automatic gain control (AGC)
    - Continuous time equalizer (CTE)
    - 1 tap Decision Feedback Equalizer (DFE)
  - 63 possible CTE ‘codes’
  - Automatic adaptation for those codes
  - DFE adaptation

Rx Block Diagram



Rx AMI Generic Architecture



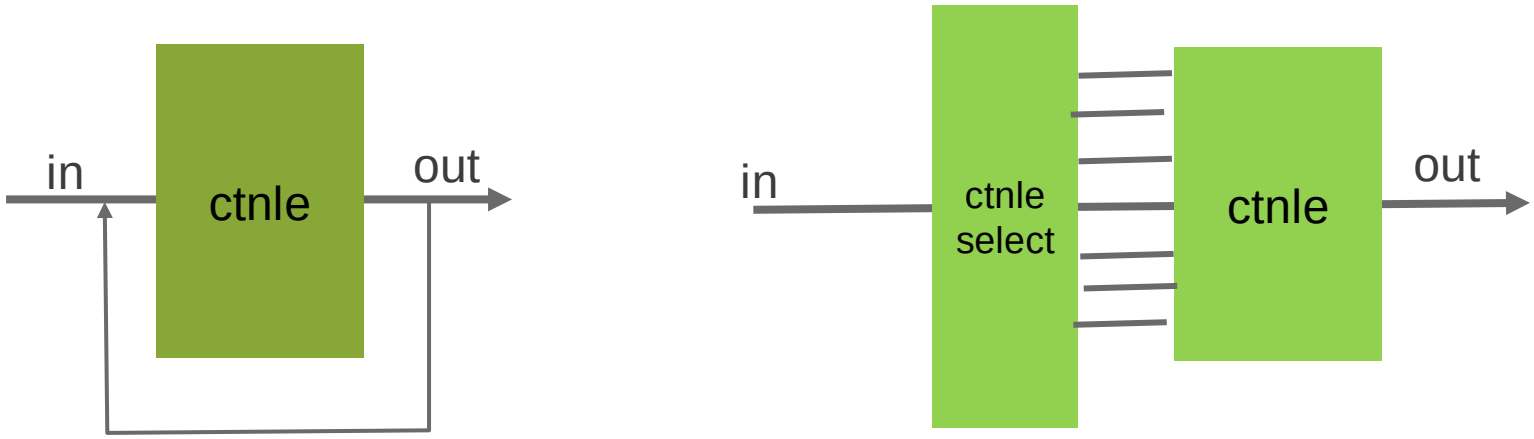
Note: There is no limit on the number of cascaded blocks

Rx AMI Model Challenges

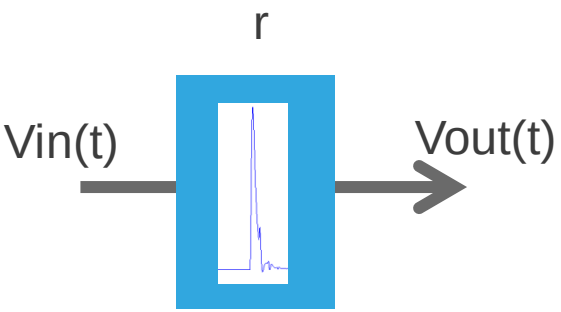
- Model/map nonlinear CTE (CTNLE) to an AMI model with reasonable performance
- Implement complex CTNLE adaptation scheme
- Integrate Tx and backchannel Tx adaptation
  - Backchannel adaptation is being proposed as an IBIS standard as BIRD 147

Nonlinear ‘CTNLE’

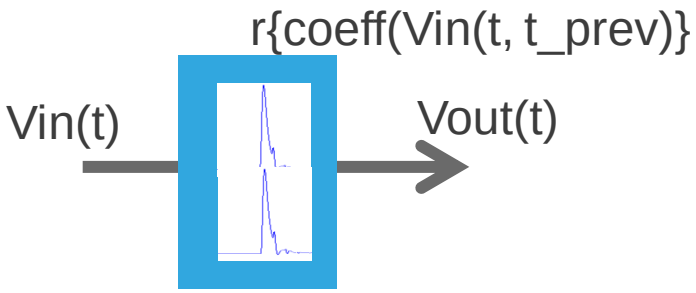
- Map to ‘piecewise’ input voltage dependent step responses
  - step response represent the cte at time ‘t’ and voltage v_in(t)



Novel ‘Dynamic’ Convolution Algorithm with Time Dependent Impulse Response

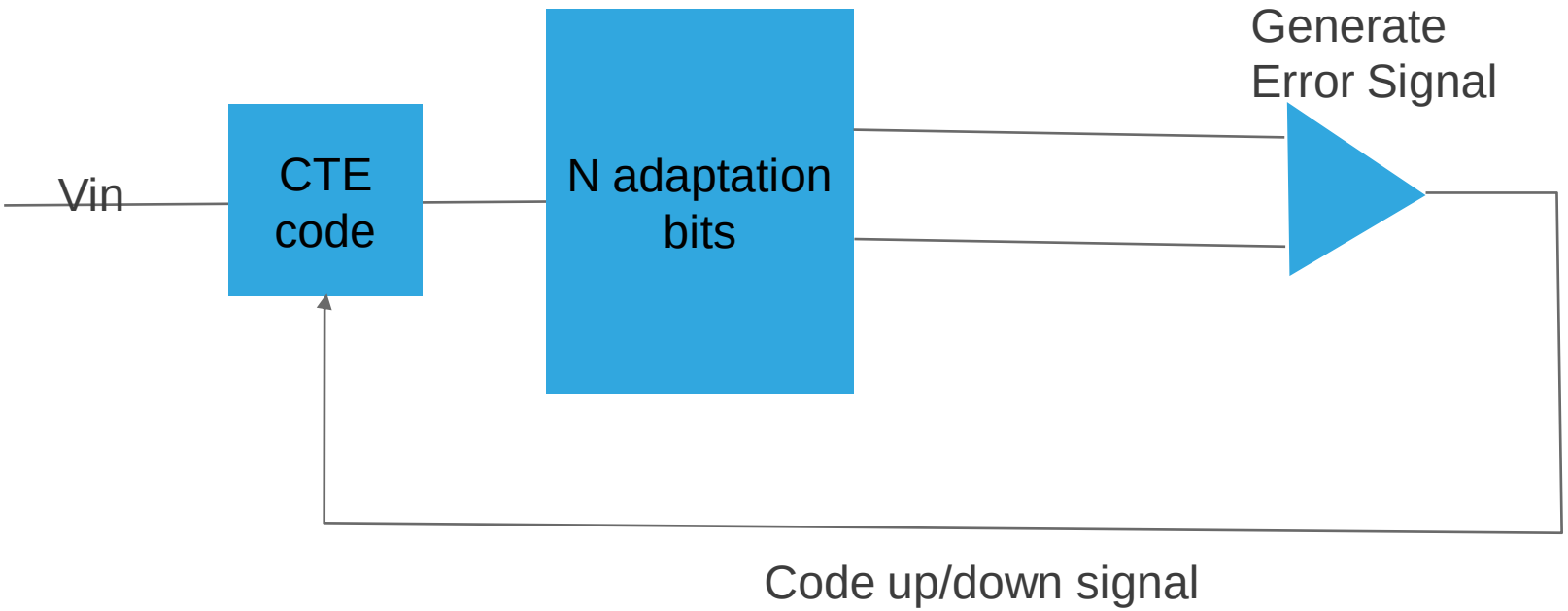


Vout(t) = Vin(t) * r

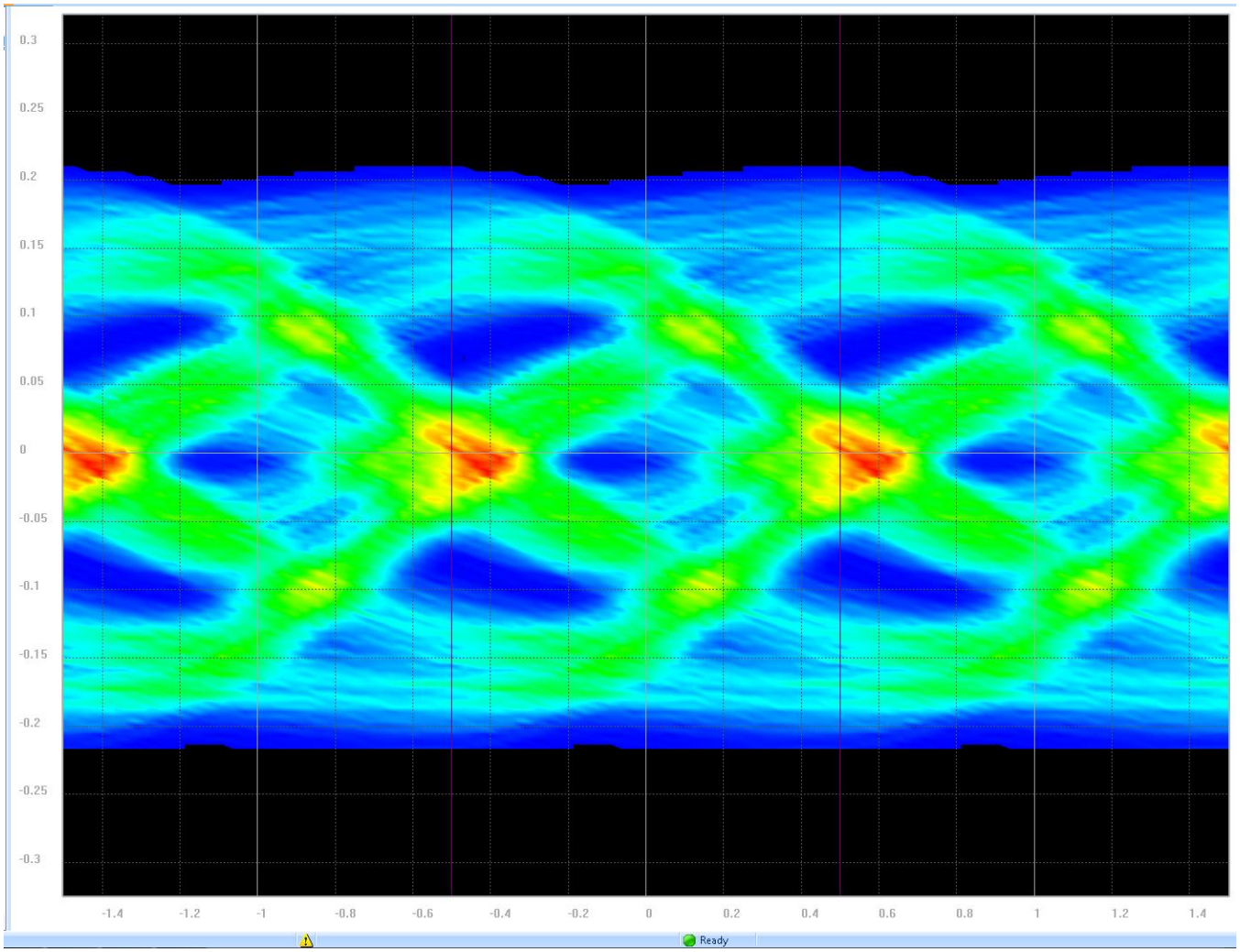


Vout(t) = Vin(t) * r{coeff(Vin(tm t_prev))}

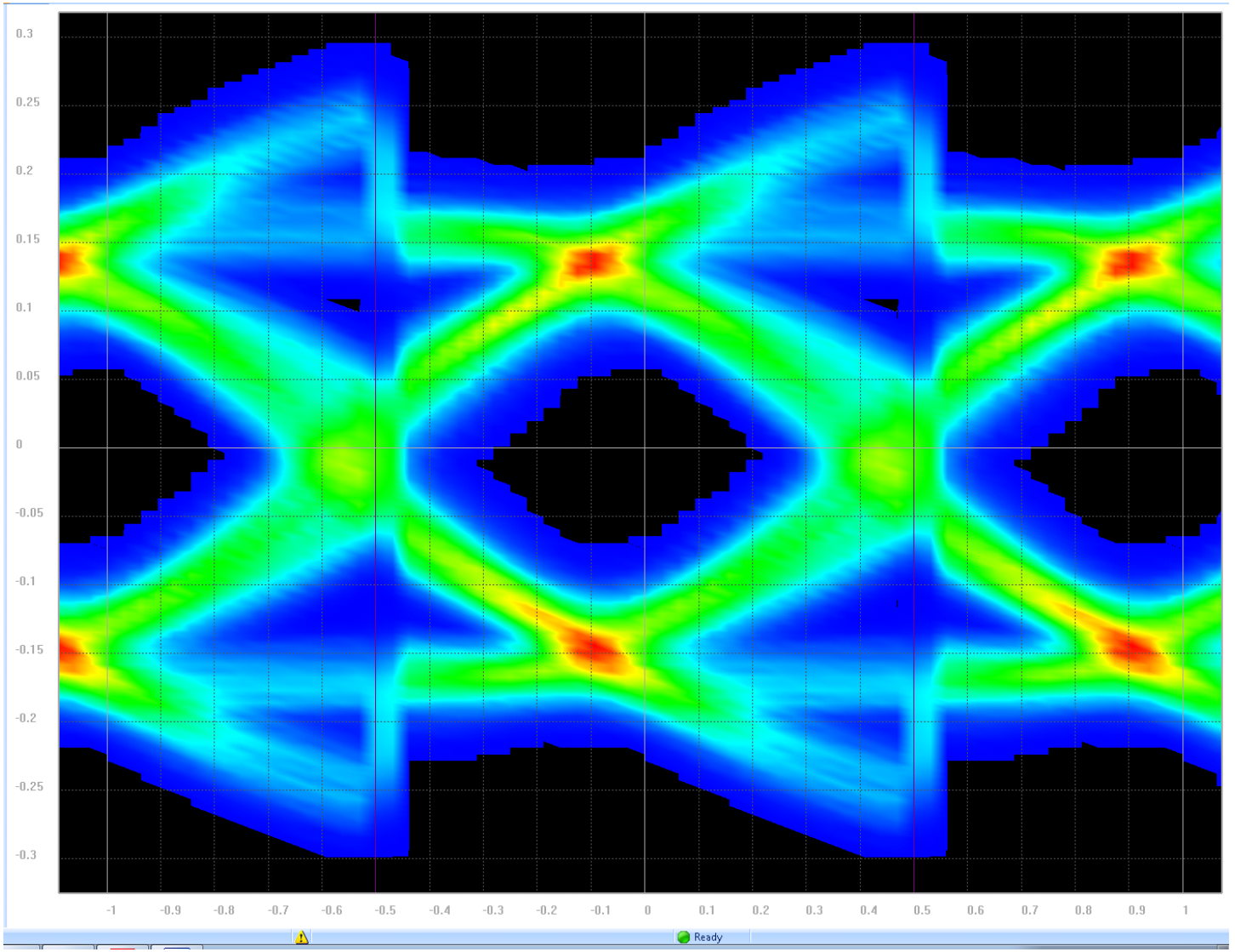
CTNLE Adaptation



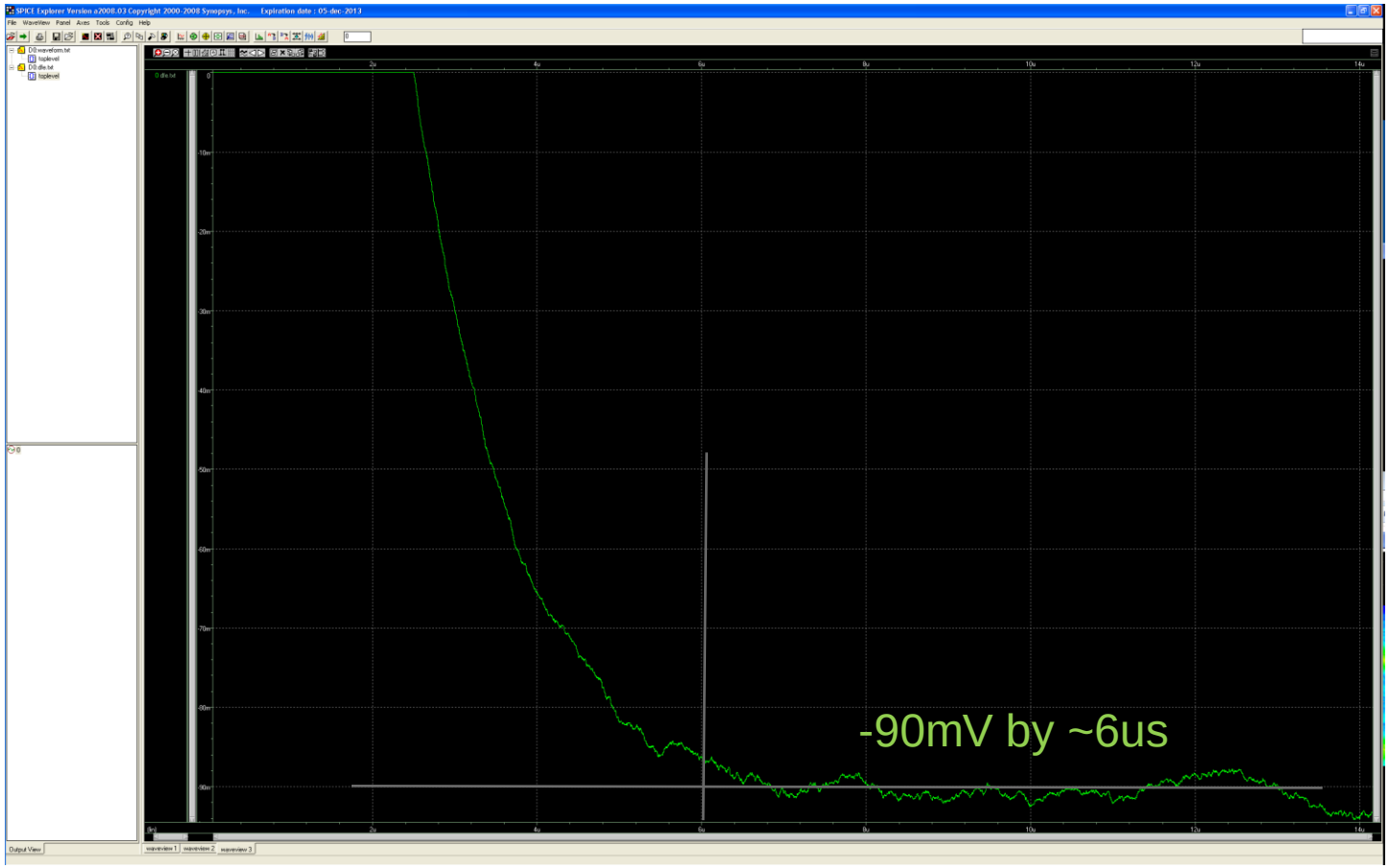
AMI Operation -- Input to AMI Model



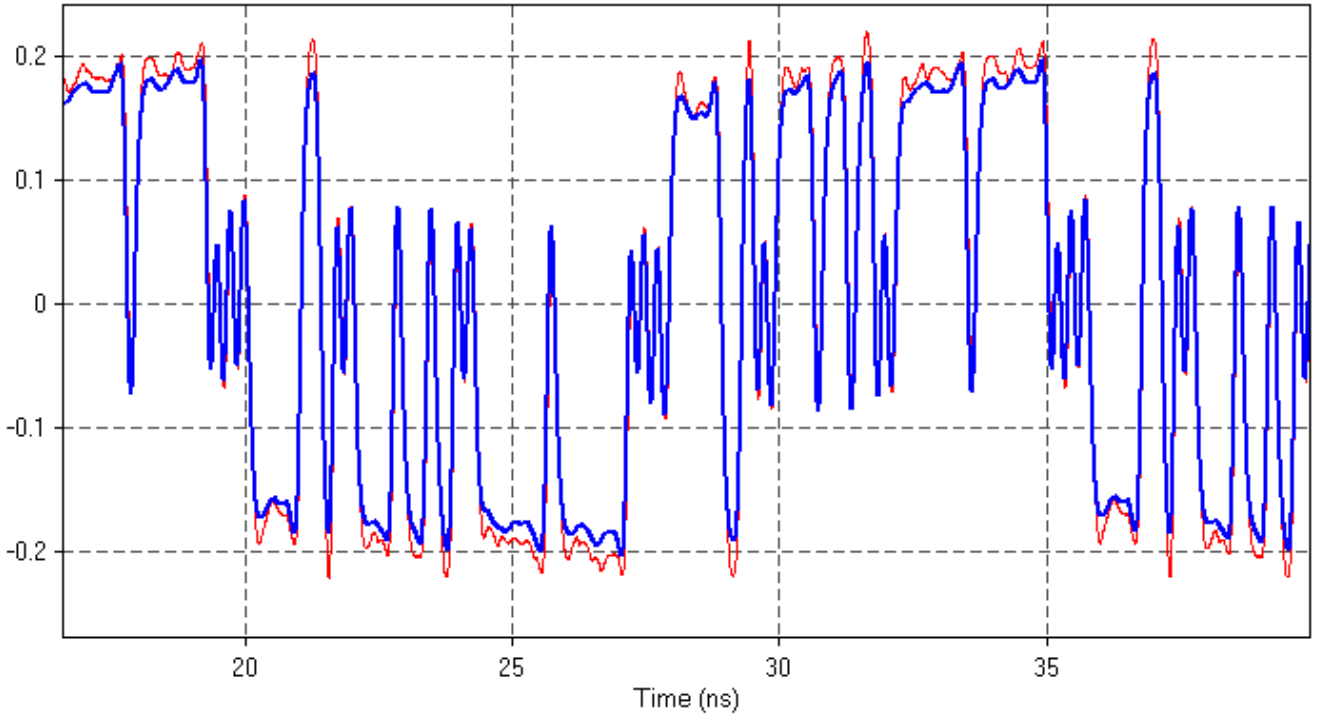
AMI Operation -- Output of AMI Model



AMI Operation -- DFE Adaptation



SystemSI vs. Transistor-Level Spice with Rx Equalization



Summary

- IBIS-AMI is today's standard format for system-level SerDes modeling
- A different type of modeling expertise is required to develop AMI models
- Modeling the adaptive CTNLE functionality in the Analog Bits Rx is the most challenging AMI effort we have undertaken to date
- Transistor-level accuracy can be obtained with high-capacity channel simulation to predict BER using AMI modeling, even for the most complex EQ architectures


cadence®