cādence®

VIA Telecom and Cadence

"Encounter Conformal Low Power helps us find and fix low-power implementation errors early in our process. With complete verification coverage from RTL to GDSII, we're reducing the risk of missing critical problems as well as having to do respins."

Frank Hsu, ASIC Design Manager, VIA Telecom

The Customer

VIA Telecom is a leading fabless semiconductor company that focuses on developing low-power code division multiple access (CDMA) baseband processors for mobile applications. The company's latest single-chip CDMA baseband processors support an array of dual-mode technologies, including CDMA2000, 1xEVDO, and CDMA2000/GSM. To support its global customer base of handset makers, VIA Telecom maintains International Design Centers around the world. Handsets based on the company's processors can be found in products in more than 20 countries around the world.

Frank Hsu, an ASIC design manager at the company, oversees the methodology for delivering netlists to the back-end team, as well as the timing closure and production test processes. Their charter is to maintain low power consumption as well as timely delivery of their products.

The Challenge

VIA Telecom's handset manufacturer customers face increasing competitive pressure to deliver unique mobile devices that consume little power and have long battery life. These OEMs are also experiencing time-to-market demands that are shortening their design cycles. To keep the pace with its customers, VIA Telecom needed to move away from its manual process for verifying the power intent of its digital baseband processor designs.

"We recognized that, in order to be an agile supplier to our OEMs, we needed to adopt an automated low-power flow," said Hsu. "Our manual process was not only inefficient in terms of time and resources, but it was also vulnerable to human error. We needed to strengthen our methodologies so that we could accelerate our schedules and also maintain product quality."

Business Challenges
- Deliver low-power baseband processors in a highly competitive market
- Meet customers' increasingly aggressive product development cycles

Design Challenges
- Automate manual process for verifying power intent of processor designs

Cadence Solution
- Encounter Conformal Low Power
- Encounter Digital Implementation System
- Encounter RTL Compiler
- Incisive Enterprise Simulator

Results
- 30% faster product development process
- Ability to take on 25% more projects with same resource level, which translates into new business for the company
- Ability to achieve first silicon success

Seeking a proven solution along with strong support, Hsu and his team turned to Cadence. Hsu noted that he and his team were influenced by Cadence's support for the creation of a low-power format standard for the industry. In 2006, Cadence launched the Power Forward Initiative with several other leading semiconductor companies, developing the Common Power Format (CPF) and eventually contributing it to Si2.

When Hsu and his team sought their solution, Cadence was the only vendor at the time to provide tools that were proven in their support of the CPF standard. Cadence's low-power flow uses CPF from design to verification and implementation.

The Solution

VIA Telecom implemented Cadence® Encounter® Conformal® Low Power, which enables the engineers to create and validate power intent in the context of their design. Merging low-power equivalence checking with structural and functional checks, the tool enables full-chip verification of power-efficient designs. Support from local Cadence applications engineers helped the team adapt the new flow into their legacy process smoothly and efficiently.

"Encounter Conformal Low Power helps us find and fix low-power implementation errors early in our process," said Hsu. "With complete verification coverage from RTL to GDSII, we're reducing the risk of missing critical problems as well as having to do respins."

" We're pleased to have 100% coverage for first silicon success, and we consider Cadence to be an important partner in our success. Cadence's best-in-class technologies align well with our business goals, turnaround time requirements, and our quality expectations. "

The company also uses Cadence Encounter Digital Implementation System for physical implementation of its design and Cadence Encounter RTL Compiler for top-down global register-transfer level (RTL) design synthesis. In addition, the company uses Cadence Incisive® Enterprise Simulator—another key component of Cadence's low-power flow—for automated testbench creation, low-power and metric-driven verification, and mixed-signal verification.

The Results

By automating its power verification process, VIA Telecom has reduced the development time for its digital baseband processors by 30%. With the same amount of engineering resources, the company can take on 25% more projects because of its more efficient flow, which translates into an ability to take on new business.

"We're pleased to have 100% coverage for first silicon success, and we consider Cadence to be an important partner in our success," said Hsu. "Cadence's best-in-class technologies align well with our business goals, turnaround time requirements, and our quality expectations."

Summary and Future Plans

Happy with its success on the digital side, VIA Telecom has adapted its Cadence low-power flow to its process for small mixed-signal devices. To further increase productivity, the team plans to evaluate Cadence Tempus™ Timing Signoff Solution, which delivers up to 10X faster timing analysis. The team also wants to automate the validation of its mixed-signal, low-power designs.

Said Hsu, "Through the adoption of the Cadence low-power flow with Encounter RTL Compiler and Encounter Conformal Low Power at the front end, we experienced a painless and smooth transition away from our manual process. In the future, we'd like to investigate other Cadence offerings. Cadence has provided us with fast and responsive support—that is key for us with any EDA tool."

cādence®

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud and connectivity applications. **www.cadence.com**