STMicroelectronics and Cadence

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Gianluigi Boarin, Design Manager, Automotive Products Group, STMicroelectronics

The Customer

STMicroelectronics's Automotive Products Group (APG), based in Castelletto, Italy, is a leading developer of semiconductor devices for automotive application areas ranging from powertrain and safety to car body and infotainment. The group's customers include some of the world's leading automotive manufacturers.

Gianluigi Boarin, APG design manager, leads a team of engineers who design automotive systems on chip (SoCs) that are tailored to each customer's unique specifications. Their SoCs are typically mixed-signal devices and they are often asked to deliver demanding low-power implementations.

The Challenge

As their customers' automotive designs evolve, so do the requirements for the SoCs developed by Boarin and his team. Changes are expected and happen irregularly. Regardless, the team must meet aggressive delivery schedules.

"It is not unusual to need to change the specifications after first silicon because something doesn't comply with the rapidly evolving system specifications," said Boarin. "These changes often require us to re-spin the device within a short timeframe."

Because automotive designs undergo a long qualification process—up to nine months—APG's customers want to receive product that's as close to final silicon as possible. To accommodate the engineering change orders (ECOs) more efficiently, Boarin and his team wanted to automate register-transfer level (RTL) ECOs for pre- and post-mask layouts. Said Boarin, "In the automotive world, the start of a design to production can take a few years, so good first silicon is important. If we can avoid changes to the base layers, we can reuse first silicon—that's our main advantage."

Business Challenge
- Get automotive semiconductor products to market quickly, while adapting to frequently changing customer specifications

Design Challenge
- Automate RTL ECOs for pre- and post-mask layouts

Cadence Solution
- Encounter Conformal ECO Designer

Results
- 4 months average estimated savings in product development time
- Significant mask-cost savings per design
- Up to 30% productivity gain for design engineers

The Solution

APG turned to Cadence® Encounter® Conformal® ECO Designer to solve its challenge. "We found Encounter Conformal ECO Designer to be an efficient solution that offered complete functional ECO automation, including the analysis and generation of optimized ECO logic changes right into our place-and-route netlist that is then used for back-end processing," said Boarin.

Encounter Conformal ECO Designer minimizes manual intervention and also reduces time-consuming iterations associated with ECOs. By quantifying the designer's intent, the tool provides an early estimate of ECO feasibility. Through its abstraction techniques, the tool can reduce verification time for multi-million-gate designs.

"We can run Conformal on customer netlists, and they can do their layout. We do the IP. We provide the RTL," said Boarin. "Even though we need to make changes to the RTL (due to specification changes), we can have the RTL of our IP 90% complete, so the customer can proceed with schematics and layout using the old flow, without worrying about RTL re-spins. We can send new RTL code and perform a post-mask fix, saving at least three weeks on the design cycle."

" This Encounter ECO tool also works at the physical level, which is a perfect fit for our needs. It's good for driving faster layout closure and successful timing signoff."

At times, the team receives RTL code from its customers using their own or third-party IP. Using the Encounter tool, the team can easily implement this IP at the top level, generate synthesis, do the layout, modify data from the RTL code, and generate the new netlist for the customer.

The APG team has been using Encounter Conformal ECO Designer for about two years. "This Encounter ECO tool also works at the physical level, which is a perfect fit for our needs. It's good for driving faster layout closure and successful timing signoff," said Boarin.

The Results

By automating its RTL ECOs with Encounter Conformal ECO Designer, ST's APG team is saving as much as three to four months in development time on some designs. The team also is saving the cost of half a mask set per design. The cost savings stems from having to make only metal-layer changes at second silicon, to accommodate changes in product specifications, and being able to reuse the remaining wafers.

"We've received very good support from Cadence. Several months ago, we had a design where we discovered a problem that was replicated across different modules, after we released the base layers and the mask," explained Boarin. "With Encounter Conformal ECO Designer and Cadence expertise, the problem was resolved, we didn't miss a milestone, the new mask arrived before the wafers, and all of this was transparent to the customer."

Summary and Future Plans

Overall, automating its RTL ECOs with Encounter Conformal ECO Designer has enabled ST's APG division to stay on top of customer needs in its high-pressure industry. "Encounter Conformal ECO Designer has enhanced our design flow," said Boarin. "We're building layers with the confidence that bugs can be fixed by the Conformal tool. And we're shortening our design time in the process."

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