Pattern-based analytics to estimate and track yield risk of designs down to 7nm

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ABSTRACT

Topological pattern-based methods for analyzing IC physical design complexity and scoring resulting patterns to identify risky patterns have emerged as powerful tools for identifying important trends and comparing different designs. In this paper, previous work is extended to include analysis of layouts designed for the 7nm technology generation. A comparison of pattern complexity trends with respect to previous generations is made. In addition to identifying topological patterns that are unique to a particular design, novel techniques are proposed for scoring those patterns based on potential yield risk factors to find patterns that pose the highest risk.

Keywords: topological pattern matching, design for manufacturability, pattern analysis

1. INTRODUCTION

As integrated circuit feature sizes continue to decrease putting increasing pressure on patterning technology, design rule restrictions for physical designs have increased dramatically[1]. In many cases this has had the effect of increasing the design regularity. In addition, it has focused attention on areas of the design that deviate from the more common and regular design styles as these 'outliers' may not be considered during the patterning process development and therefore may have poor process margin.

In recent years new software tools have become available to analyze layouts based on topological patterns[2,3]. Combined with techniques for processing large amounts of data, these tools have shown that they are capable of cataloging all unique pattern topologies in a layout and comparing the results against the pattern set from a different design. This presents opportunities for making quantitative comparisons of design complexity across process technologies, metal layers, and design types among other applications.

Once a set of patterns has been determined to be unique to a particular layout it is helpful to have a methodology for filtering the patterns to identify those that pose the most likely risk for manufacturability. This work will propose a flow for identifying these high risk patterns based on topological complexity and dimensional factors and demonstrate correlation to patterning risk for an example data set from a 7nm design.

Section 2 will review the concepts of topological pattern cataloging. In Section 3, previous work on analyzing trends in topological pattern complexity from node to node will be extended to the 7nm generation while Section 4 will study pattern complexity at different levels in the metal stack. A flow for cataloging topological patterns in a layout, comparing them to a database of known patterns, and analyzing the unique patterns for potential yield risk will be presented in Section 5, and finally conclusions are presented in Section 6.

2. TOPOLOGICAL PATTERN CATALOGING

Early pattern matching engines used a Three-Value Logic (TVL) method for describing patterns[4]. These patterns could then be kept in canonical representation in a Pattern Database (PDB)[5]. However, we have established in our previous work that by using a new topological representation we can additionally quantify the complexity of vast numbers of patterns very easily[3]. In addition to the complexity, we have the ability to search, replace, optimize, correlate and run further analytics on these patterns. Cataloging a universe of patterns for the same design across each technology node can reveal interesting trends. Different designs from the same generation can also be compared to identify differences and commonalities.

The topological pattern representation uses scanlines that cross the extraction window for all edges of all layers (Figure 1). The cataloging process can quickly scan reference designs and store these topological patterns in a database. We systematically scan a window across an entire design where the choice of the window size is important. In every window, we break-down and identify every pattern and sub-pattern that exists in that design with dimensions. A full catalog of all patterns with dimensions is stored in a database (Figure 2).

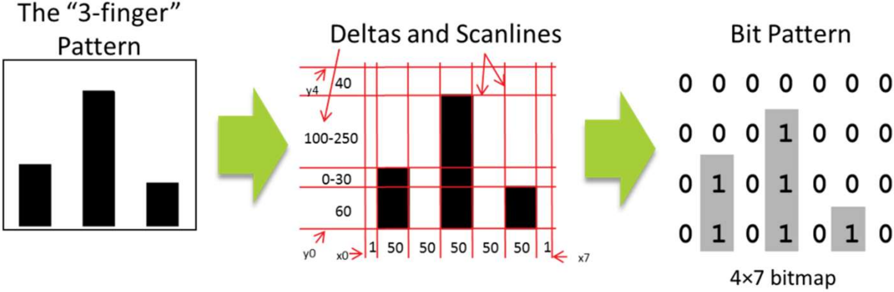


Figure 1. Topological pattern description

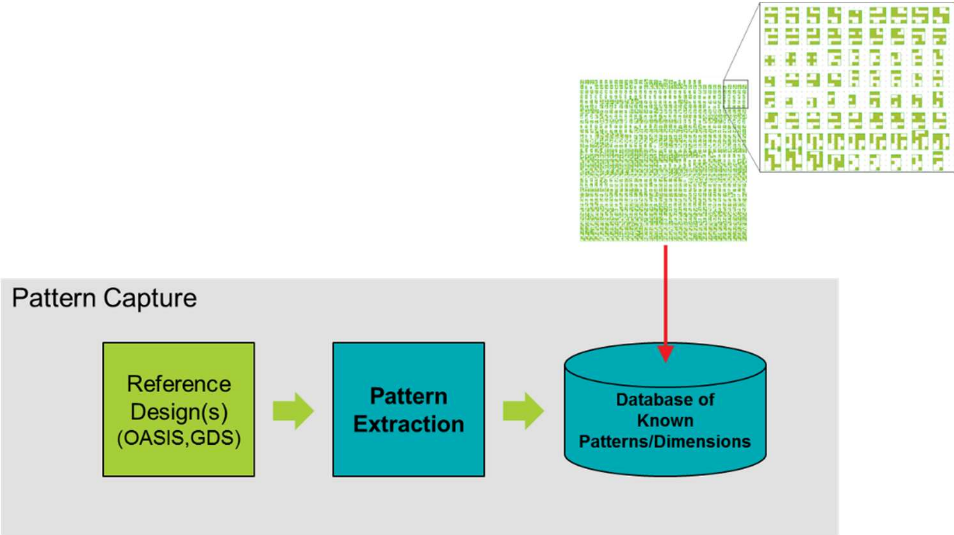


Figure 2. Pattern capture flow

Not all patterns for a given window size have the same complexity. The total number of scanlines alone can help contribute to a meaningful cost function to quantify the complexity. Figure 3 shows some example topologies of varying complexity. When we look at the pattern topologies along with their corresponding dimensions we can analyze the data further to isolate new and high risk patterns. This ability to identify and highlight layout differences is very powerful with many use cases. For example, OPC engineers can quickly find regions that deserve more analysis. Process and failure analysis teams can use this information to feed forward monitoring point. Generally this data gives an entire team an indication of how difficult a new tape-out will be, especially when ramping up a new process.

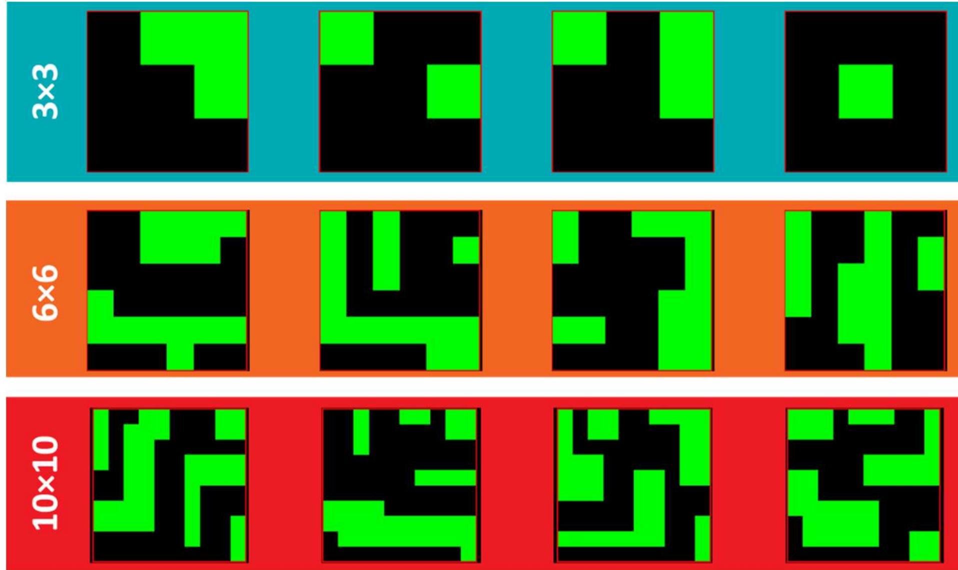


Figure 3. Examples of topological patterns of varying complexity.

3. EVOLUTION OF LAYOUT TOPOLOGICAL COMPLEXITY

Previous work[3] used the pattern cataloging process described in Section 2 to analyze a digital circuit block implemented in three different process technology generations – 28nm, 20nm, and 14nm. This work extends that analysis to include the 7nm generation. In each case the same RTL was used to synthesize the physical implementation for the specific process. The first three '1x' (i.e., minimum pitch) metal layers were analyzed using a window size corresponding to three metal pitches (scaling the size according to the minimum metal pitch for each technology).

Figure 4 shows the distribution of unique pattern topologies among different complexity classes across different process nodes. For each heat map, the simplest topology captured (3×3) is shown in the bottom left and the most complex (10×11) is in the upper right. Note that since pattern rotation or mirroring is not considered, a new topology on the lower half of Figure 4 would look the same as the upper half (i.e., a 4×5 pattern is the same as a 5×4) and has therefore been omitted for clarity. In addition, Table 1 shows both the number of unique topologies and the total number of unique patterns (i.e., specific dimensional variations of a topology) for each version of the design.

There is a clear decrease in the design complexity from node to node. There is a very large decrease from 28nm to 20nm, most likely due to the increased design restrictions that resulted from a change from single exposure to double exposure patterning processes. In addition there was increased usage of local interconnect layers at 20nm that shifted some of the complexity from the 1x metal layers to the new local interconnect layers. Although the metal patterning process and design rules were virtually identical between the 20nm and 14nm generations there is still a significant decrease in layout complexity in the transition to 14nm. This may be a result of the increased regularity in the front-end-of-line (FEOL) layers due to the adoption of FinFET devices with a discrete number of fins.

The 7nm generation shows another very large decrease in 1x metal complexity. The reason for this is that the 7nm process studied here uses a self-aligned double patterning (SADP)[6] process that is strictly one-dimensional with fixed line width and space values. As a result both the total number of unique topologies and the complexity of those topologies dropped by approximately two orders of magnitude.

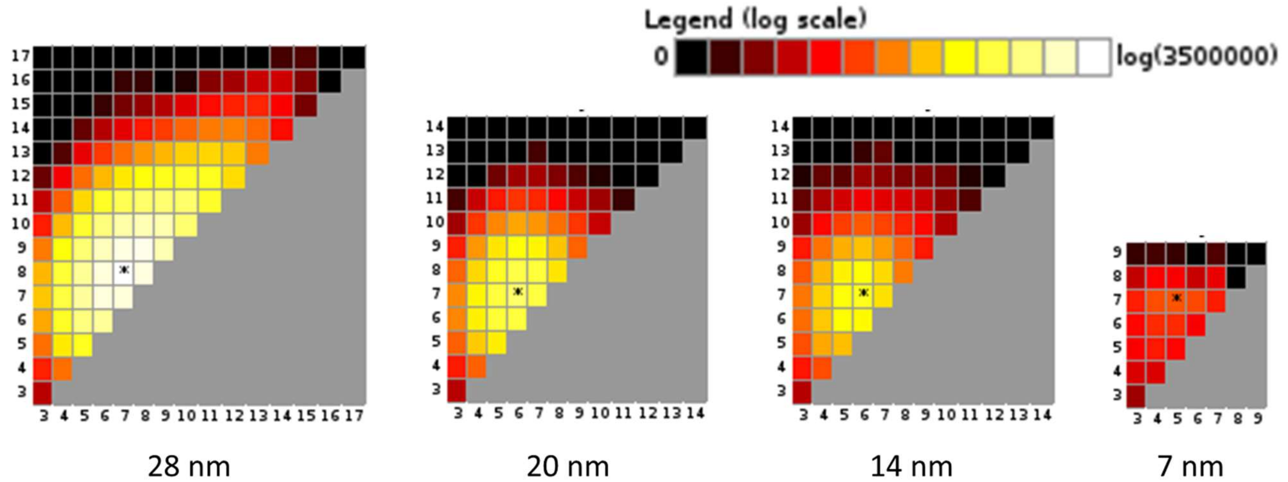


Figure 4. Extracted pattern topology counts for the same digital circuit block implemented in 28nm, 20nm, 14nm, and 7nm process technologies. Note that the color scale is logarithmic.

Table 1. Total count of unique patterns in the same digital circuit block implemented in three different technology generations. The first three 1x metal layers are considered with a window size corresponding to three minimum metal pitches in each technology.

Technology Node	Total Unique Topologies	Total Exact Patterns
28 nm	20,763,677	286,593,810
20 nm	835,025	39,977,934
14 nm	242,633	17,634,752
7 nm	4,964	197,257

Additional analysis of the unique pattern topologies in a given layout can give insight into the design regularity. The distribution of unique pattern instances for the 7nm digital logic block is shown in Figure 5. Clearly the design is dominated by a few topologies with relatively high counts and the distribution has a long tail of patterns with very low counts (although again the counts are orders of magnitude smaller than previous technology generations). This indicates that there may still be opportunities for layout regularization if the topologies with very low instance counts can be converted to more common topologies. This can reduce the number of cases that the patterning process needs to be optimized for and improve overall manufacturability.

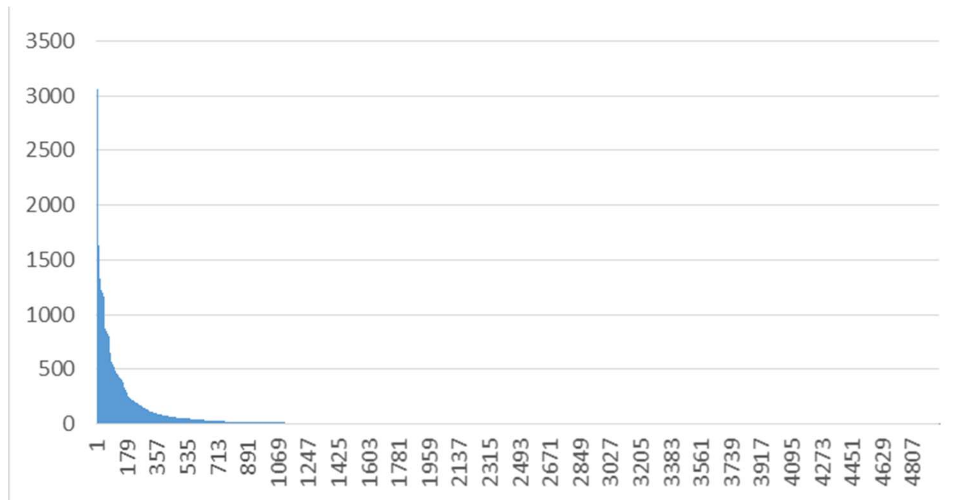


Figure 5. Distribution of instance counts for unique pattern topologies in a 7nm digital logic block.

4. TOPOLOGICAL COMPLEXITY TRENDS ACROSS THE METAL STACK

4.1 Methodology Overview

In this section we explore trends across the metal stack. Specifically, in this analysis we capture successive two-layer patterns across the stack; for example, we get all via layers with corresponding metal above and metal below. The analysis is "anchored" on every via or cut and a fixed-size pattern is extracted around this anchor of size 4 tracks in both x and y.

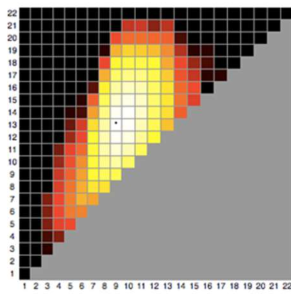
4.2 Trends in 20/14nm

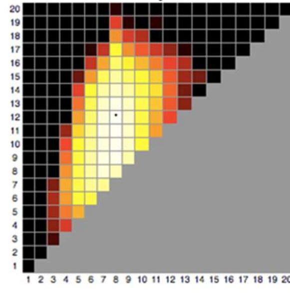
A summary of the Mx/Vx trends for 20nm and 14nm is shown in Figure 6. Each of the heat maps plot the count of the number of topologies for each x/y scanline combination as a separate bin. As shown in the scale bar in the figure, the count for each bin is expressed as a color on a log scale from 0 to log(maximum); a smaller count shows as a darker red (until it turns black) and a higher count shows as a brighter yellow (until it turns white). The highest count x/y scanline combination is denoted with an asterisk ('*').

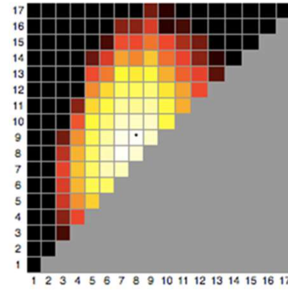
The 20nm and 14nm test cases are actually quite similar which is expected given that these layers share the same design rules. That said, it is clear that 14nm has a small reduction in the maximum scanlines in x/y; for example, V2/M3 for 14nm goes up to 16x16 complexity bin whereas for 20nm this goes up to a higher 18x18 complexity bin. Therefore the maximum complexity within a 4 track by 4 track window has been reduced at 14nm.

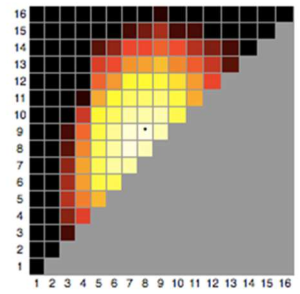
Another interesting observation is the larger number of low complexity bins at 20nm. This would indicate a better usage of available real estate with fewer sparse low complexity patterns for Mx/Vx layers.

14NM



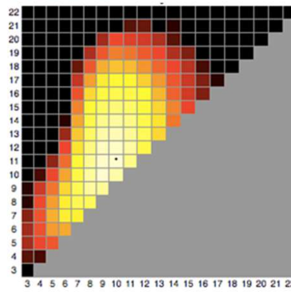


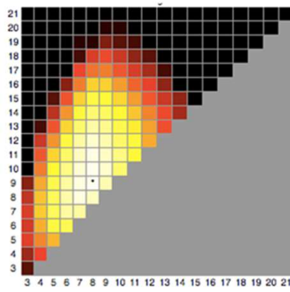


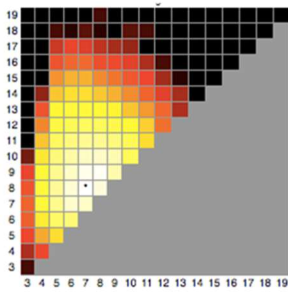


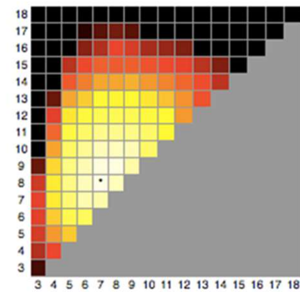
V1/M1 V1/M2 V2/M2 V2/M3

20NM









V1/M1 V1/M2 V2/M2 V2/M3

Figure 6: Comparison of Mx/VxPatterns between 14nm and 20nm

4.3 Trends in 7nm

The next part of the analysis focused on 7nm trends. As described earlier, the general trend is toward a significant reduction in complexity. In that context an effort was made to explore how that complexity was distributed across the layer stack. A summary is shown in Figure 7. Statistics for unique topology counts as well as exact patterns counts are plotted for each layer. Recall for any particular topology, there can be multiple specific exact pattern instances of that topology with different specific dimensions in x/y. The peaks of complexity are, as expected, at the interface between layers where ground rules have changed (transition vias), for example at V1/M1 and at V3/M4.

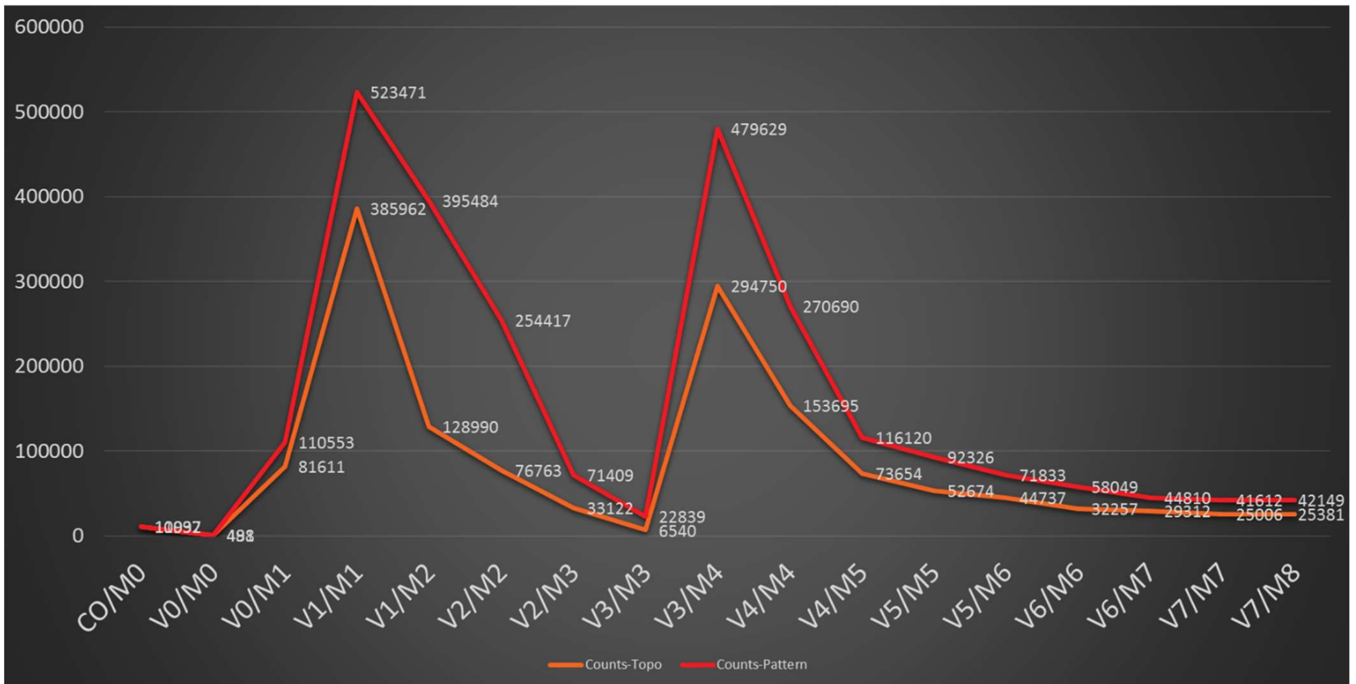


Figure 7: Topology and Pattern Count Statistics for 7nm MOL/BEOL Layers

Figure 8 shows heat maps plotting the count of the number of topologies for each x/y scanline combination as a separate bin across the 7nm stack. This is similar to heat maps shown previously but without any pattern rotations, which explains why M2 topologies have heat maps that are rotated relative to M3 topologies.

The M1 layer combinations (V0/M1 and V1/M1) clearly have the highest complexity and greatest entropy in terms of the number of different topological combinations; they exhibit both the brightest bins and greatest spread in terms of the number of bins. That said, much of that variation can be explained by looking at the patterns themselves, such as the example shown in Figure 9. This pattern is a 17x14 topology from V1/M1. The fact that the metal is wider than the via results in a larger number of additional scanlines in the x direction to account for the metal overlap surrounding each via.

The other layer combinations exhibit relatively fewer numbers of bins. In particular note how the M2 patterns are clustered around 9 scanlines in y whereas the M3 patterns are clustered around 9 scanlines in x. This is representative of the fact that almost every track is filled; the 9 scanlines therefore represent 4 minimum separations and 5 wires in a 4 track window. That said, even though the number of topologies is small, there are still a large number of variants for each topology, but only in one dimension. The common 9 scanlines are fixed to min space and width, but across the other dimension there can still be a large number of variations.

It is also interesting to look at cases that are not the common 9 scanline variant. An example is shown in Figure 10. This is a 10x11 topology from V2/M3. Note the jog in the wire that causes the introduction of the extra scanline. The block that was analyzed was not yet DRC clean and this analysis highlighted those cases.

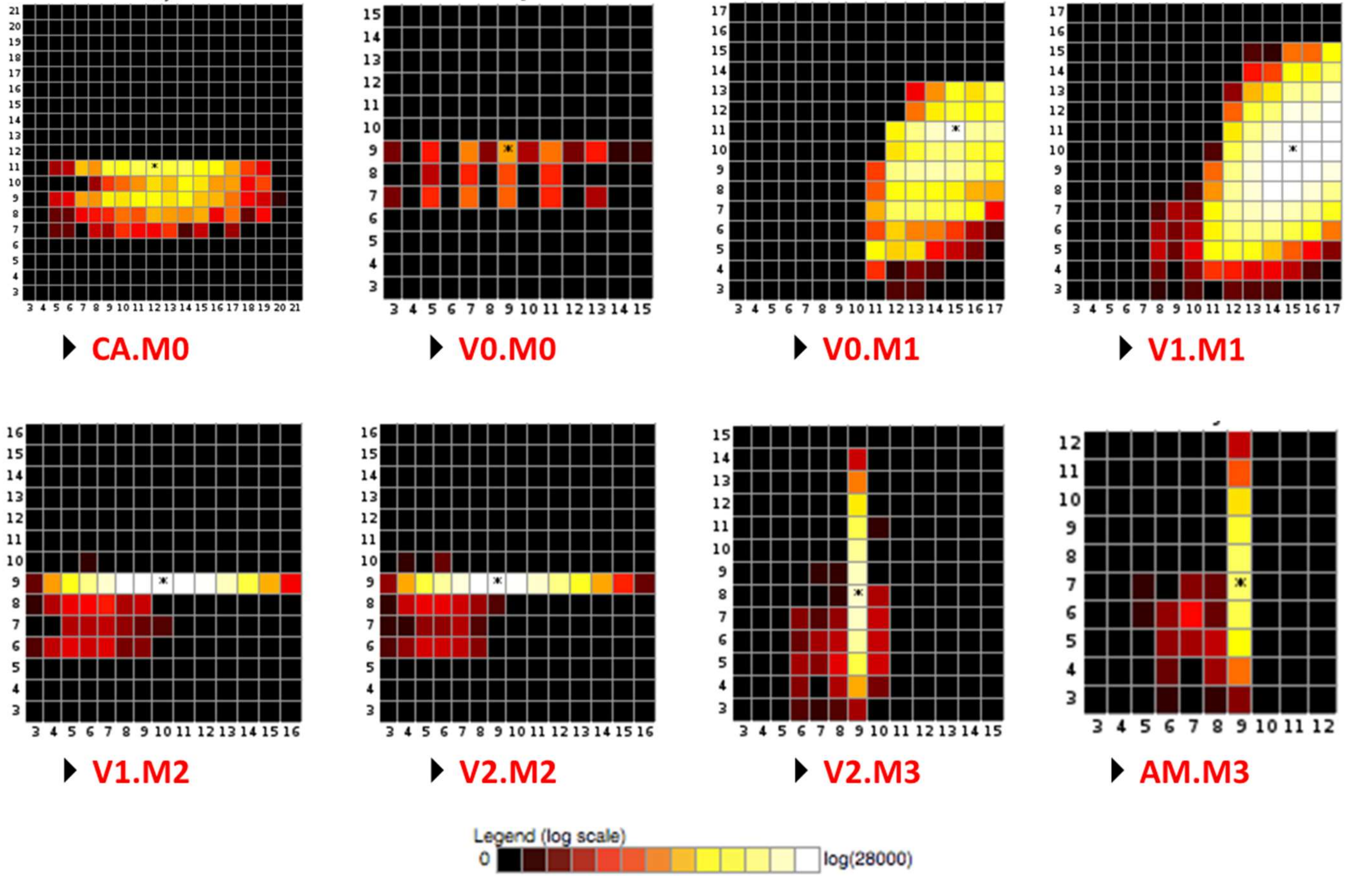


Figure 8: Evolution of Complexity across 7nm Stack

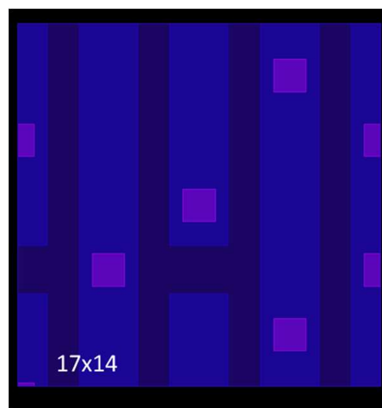


Figure 9: Sample High Complexity 17x14 V1/M1 Pattern

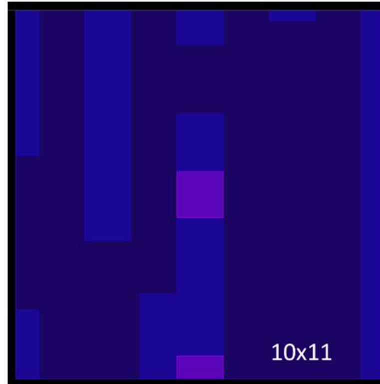


Figure 10: Sample Irregular 10x11 V2/M3 Pattern

5. LAYOUT DIFF AND ANALYTICS FLOW

5.1 Review of layout diff methodology

For this work we implemented a new flow called Diff and Analytics (DNA). This flow is used to analyze designs with the pattern-centric view described earlier and a flow diagram is shown in Figure 11. Here, patterns are cataloged for each design using pattern classification. The 'Diff' step is introduced to reduce the set of cataloged patterns by identifying new patterns that exist in the target design but are not in the base design(s).

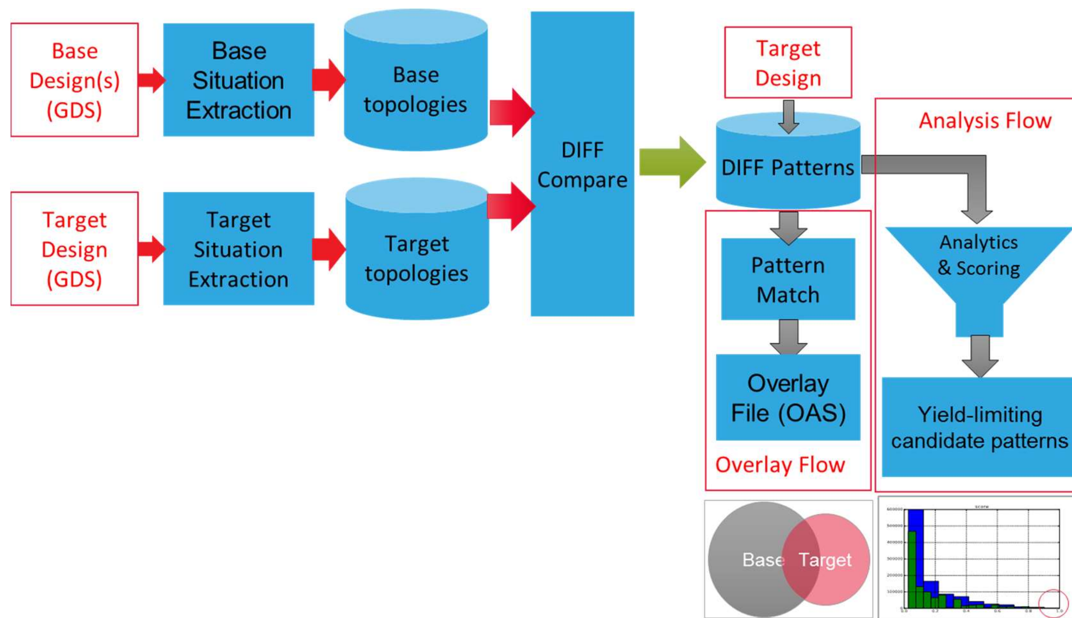


Figure 11: Diff and Analytics Flow Overview

5.2 Example: Common metal layers in 20/14nm and 7nm

In this study, the Diff method is applied to see the differences between common metal layers (i.e., metal layers with the same design rules) of a design block at 20nm/14nm and 7nm technology nodes. Figure 12(a) shows the differences in

terms of pattern topologies or signatures. Here, we see around 45% of 7nm pattern topologies have an overlap with the existing topologies previously seen in the design block for 20nm/14nm. As shown in Figure 12(b), more than 90% of the exact patterns are different for the 7nm design block when compared to the equivalent design for 20nm/14nm. This result leads to the observation that even though there is a good overlap (greater than 50%) of pattern topologies, the delta variations or dimensional values are still very different. Therefore, most of the patterns (greater than 90%) in the 7nm target design are new or "unknown" patterns which were not seen in the 14nm/20nm base designs.

	Target (Not in Reference)	Intersecting	Reference (Not in Target)
All Target Signatures	451,276		
Signature Counts	255,443	195,833	1,418,550
All Reference Signatures		1,614,383	

	Target (Not in Reference)	Intersecting	Reference (Not in Target)
All Target Patterns	8,506,983		
Pattern Counts	8,021,110	485,873	40,357,476
All Reference Patterns		40,843,349	

Figure 12 (a) Mx Topology Comparisons between 7nm and 14/20nm, (b) Mx Exact Pattern Comparisons between 7nm and 14/20nm

5.3 Overlay flow

In order to extract the locations of new "unknown" patterns identified through the 'Diff' process, we ran a pattern matching tool on the target design layout. This results in the overlay file with the matched boxes for all "unknown" patterns on the target design. The generated overlay file can further be used to perform simulations within the overlay regions to significantly reduce the turnaround time of a model-based verification flow. Also, the generated overlay file can be used for monitoring the design-process weak points in the fab. In this study, we planned to use the generated overlay file to correlate it with simulation verified "hotspots".

5.4 Analysis flow

One of the critical steps in the DNA flow is to perform risk analyses on patterns. After reducing the pattern set to new "unknown" patterns, we further can reduce the pattern set by running analytics. In this work we extracted pattern features including pattern complexity (a topological metric) and counts of critical dimensions (a DFM metric) to compute a risk score.

As shown in Figure 13, the complexity of the patterns is defined as the total number of scanlines or signature matrix size in x and y dimensions (i.e., the number of bits in the bitmap representation). The pattern complexity is a topological metric[3].

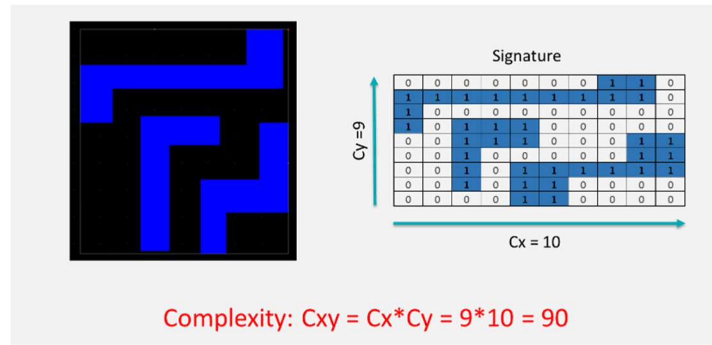


Figure 13: Pattern Complexity Calculation

Additionally, counts of critical dimensions (*ccd*)[7] may be defined. This is a user-defined metric and is based on design-process weak point learning and/or engineering judgement. One can define critical dimensions as simple rules that have some correlation with design-process weak points. For example, on metal layers the set of critical dimensions may include "line-ends", "min-space" and "min-width" ranges and/or 2D rules like "inner" and "outer" corners. In Figure 14, we show one such scheme for determining *ccd*. In this example, the pattern has 2 "line-ends", 3 "min-space", 6 "min-width" and 5 "inner-corner" critical dimensions. Therefore, the total value of the *ccd* metric for this pattern is 16. Note that it is also possible to define these *ccd* rules as patterns and to discount them at the boundary.

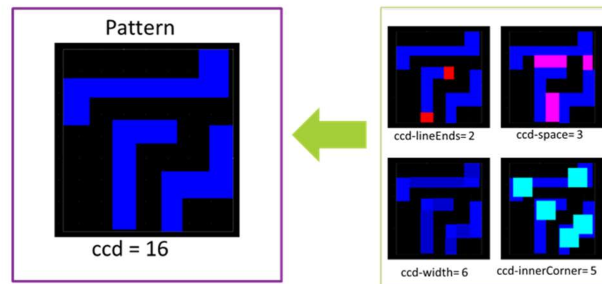


Figure 14: Count of Critical Dimensions

5.5 Pattern scoring methodology

Using these features and an empirical scoring method which is defined as a product function of the complexity and *ccd* population distributions, a risk score is computed for the 2X metal layer patterns of the 7nm design. Figure 15 shows the distribution of the computed *ccd*, complexity and risk score. Here, the risk score assigns relatively higher risk to patterns which have both high complexity and *ccd* in the overall pattern population set.

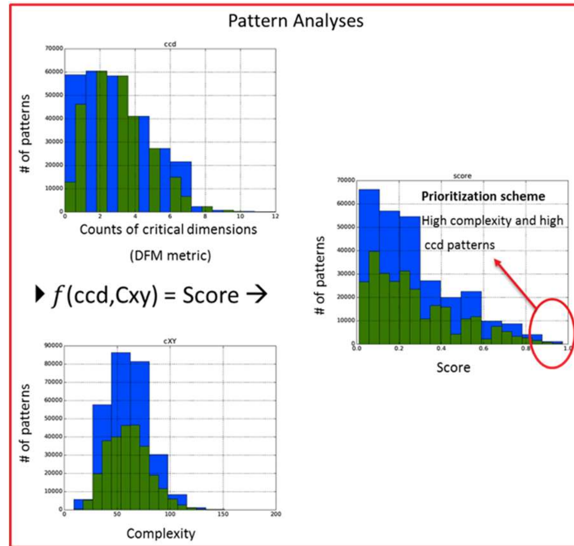


Figure 15: Via-Anchored Pattern Analysis

5.6 Validation of pattern scoring with lithography simulation

The validation scheme for the computed risk score involved correlating simulated “hotspots” with patterns and thereby their risk score. In this work, we use rigorous optical proximity correction (OPC) models to mimic the optical lithography and resist development process effects. The process variability bands (PV bands) demonstrate the printability limits due to variation in process parameters such as exposure dose, focus, and mask errors. Capturing process effects helps to improve design layouts by controlling patterns sensitivity to process window variations. The generated PV bands are checked for hotspot cases like critical width (pinching), critical spacing (bridging) and via coverage ratios.

After correlating simulation based defects to patterns, we computed the fraction of the defect related pattern population in each scored bin to the overall pattern population in that bin. As shown in Figure 16, the computed risk score is shown on the x-axis and the percentage of defect patterns with respect to the overall pattern population in the scored bin is shown on the y-axis. A strong correlation between the risk score and the defect pattern population is observed. This implies that with the increase in computed risk score we have relatively higher probability of patterns posing systematic yield risk.

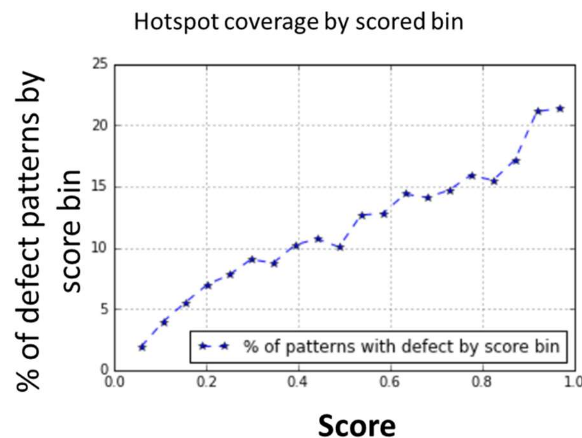


Figure 16: Simulation Hotspot Coverage

Figure 17 illustrates dense-isolated line transition regions, where PV bands show process vulnerability in terms of marginal necking and pinching. This behavior suggests that RET modules such as assist feature might need further optimization to increase the image fidelity in these locations.

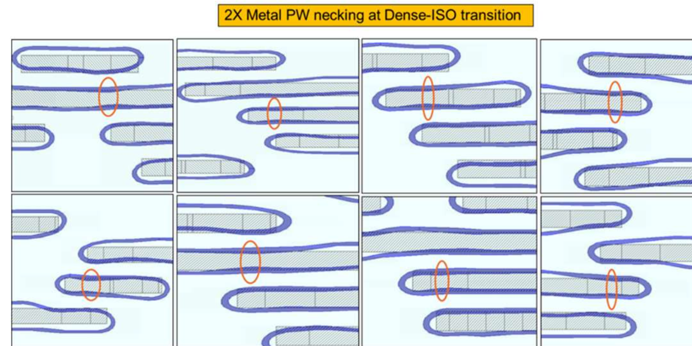


Figure 17: Examples of lithography hotspots on 2x metal layers.

6. CONCLUSION

In this paper we have extended our previous work[3] on comparing design trends using pattern complexity analyses to the 7nm technology node. We observed that the complexity has been reduced significantly for Vx/Mx layers in 7nm due to the introduction of the self-aligned double patterning process at for the Mx layers. We also introduced the Diff and Analytics (DNA) flow to compare two or more designs and to compute risk scores in order to prioritize patterns with high yield risk. We applied the DNA flow for 7nm 2x metal layers (the single-exposure layers with the tightest pitch), and compared 4-track sized patterns to the equivalent layer in the 14nm/20nm node. Here, we found nearly 50% topologies that are newly introduced in 7nm. However, more than 90% of the patterns seen on these 2x routed metal layers at 7nm are unique to those seen in the same layers at the 14nm/20nm nodes due to the introduction of new delta (dimensional value) variants. We also computed their risk analyses scores using pattern features corresponding to a count of 'critical dimensions' (*ccd*) and complexity. After validation with simulation-based results we observed a strong correlation between the computed risk score and the probability of patterns posing systematic yield risk. This methodology may be used to efficiently analyze a new design and identify not only those patterns which have never been seen before but also to filter those results for the patterns that may pose the most significant patterning risk.

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