Methodology for analyzing and quantifying design style changes and complexity using topological patterns

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ABSTRACT

In order to maximize yield, IC design companies spend a lot of effort to analyze what types of design styles are needed and used in their layouts (standard cells, macros, routing layers, and so forth). This paper introduces a novel methodology for full chip high performance topological pattern analysis and the applications of this methodology towards analyzing design styles in order to quantify and measure design changes and the degree of layout regularization. This new approach allows engineers to perform a full profiling across all patterns that exist in design and without needing to explicitly specify what patterns to analyze.

1. INTRODUCTION

The continued increase in complexity of integrated circuit (IC) manufacturing processes to achieve improvements in area scaling, power, and performance along with the adoption of system-on-chip (SOC) architectures in which diverse circuit blocks are combined onto a single chip has led to a corresponding increase in IC physical design (layout) complexity. The relationship between layout complexity and chip yield has been difficult to quantify systematically but it has long been known that some layout patterns are more likely to fail than others.

Design rule checks (DRC) have been used to verify the compliance of a physical design to the design rules and presumably ensure manufacturability. However, the design rules primarily consist of checks for one-dimensional constraints (line width or space, for example). In approximately the 65nm generation it became clear that as patterning processes became more challenging there were certain two-dimensional layout patterns that exhibited high failure rates despite meeting all design rule criteria.

Pattern matching engines were introduced over a decade ago and have since seen broad adoption as a tool to augment conventional DRC with two-dimensional checks for specific layout patterns that can be forbidden in the design.[1] The early implementations of these pattern matching engines were based on a three-value logic (TVL) approach. More recently topological pattern analysis has been introduced.[2,3] This methodology has proven to have powerful new applications in quantitatively analyzing layout complexity and in comparing two designs.

Section 2 will introduce the concepts of topological pattern analysis. This approach is then used to systematically extract all unique layout patterns as described in Section 3. The set of extracted patterns for two different layouts can then be analyzed to identify commonalities and differences quantitatively. This process is discussed in Section 4. Finally, a summary and conclusions are presented in Section 5.

2. TOPOLOGICAL PATTERN ANALYSIS

The approach used in this study is based on an analysis of topological patterns. Topological patterns are a compact representation of a layout clip which separates the pattern topology from its dimensional constraints. This is illustrated in Figure 1. The bitmap intuitively captures the basic topology in a simple visual representation. In this example, a single bit is used to represent whether the location contains space or geometry. This approach is extended to multiple layers by increasing the number of bits at a location in the bitmap. The dimensionality of this bitmap is a summary of the

complexity of the pattern. The height and width of each bit of the bitmap is captured as a dimensional constraint that is summarized as two vectors, one for the x dimension and one for the y dimension.

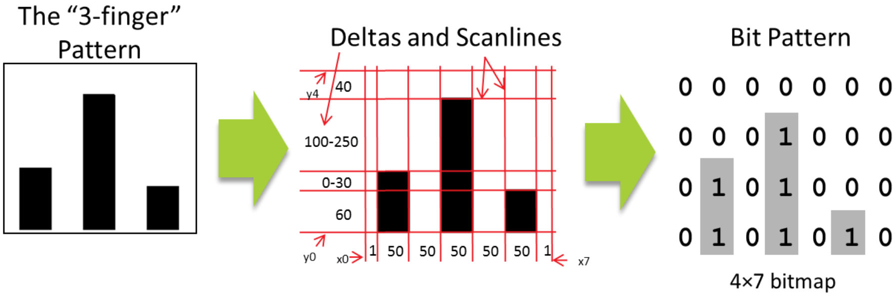

Figure 1. Topological pattern description

A pattern with 10x10 bits is more complex than one with 3x3 bits and correspondingly more difficult to manufacture. Some additional examples of topological patterns (represented in layout space) are shown in Figure 2 for 3x3, 6x6, and 10x10 patterns. Note this purely illustrative and there is no restriction that patterns must be square.

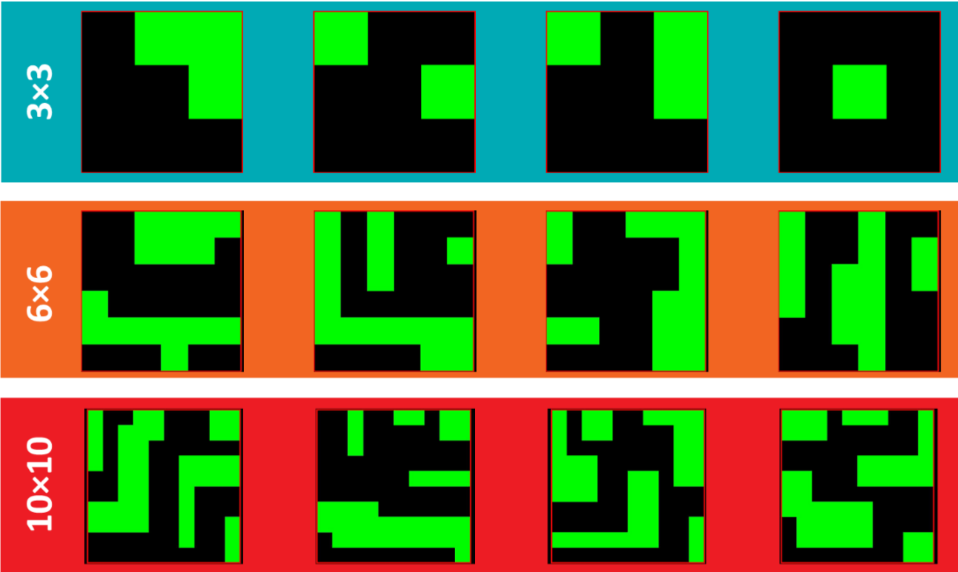

Figure 2. Examples of topological patterns of varying dimensionality

An analysis of a layout is performed by systematically scanning a fixed window across the entire design and extracting every pattern and sub-pattern that exists within that window. This pattern capture flow is illustrated in Figure 3. In this manner a full catalog of all patterns with their dimensions can be created and captured to create a database that represents the full design space of that layout (up to the specified window size). These patterns are stored as a database of topological patterns. The figure illustrates this concept by showing the patterns in the database tiled out as a matrix of individual patterns of varying dimensions dimensionality. Performance is critical to this type of methodology and in this study full chip 1x metal layers (i.e., the metal layers with the minimum pitch supported by the process technology) were fully captured in < 8 hours with only 32 CPUs.

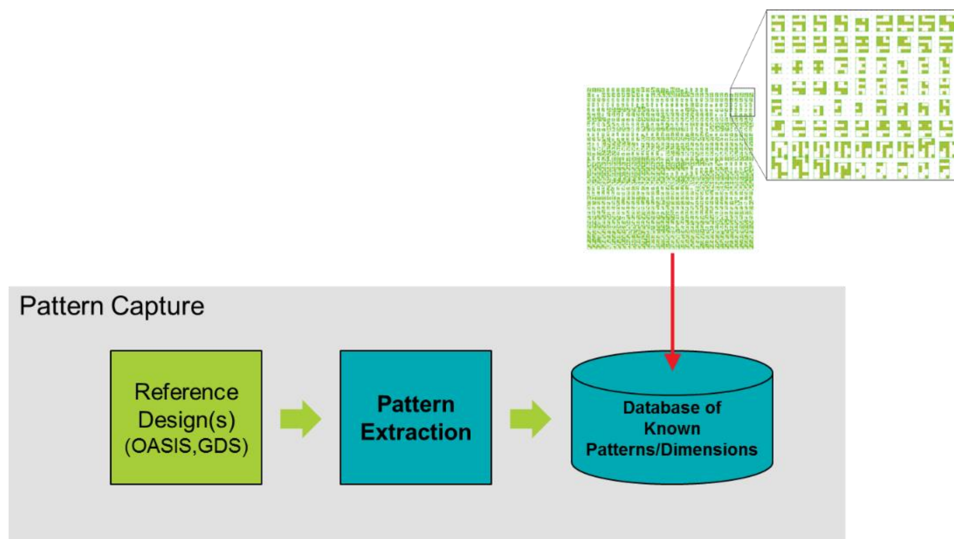

Figure 3. Pattern capture flow

Once a database of patterns has been harvested, these databases can be easily manipulated. Databases of multiple designs can be merged, compared, and analyzed. Topological pattern bitmaps are stored in a canonical form so that they are invariant to mirror and rotation, allowing the merging process to properly account for duplicate patterns. The process of comparing a database against a layout is illustrated in Figure 4. This same approach can be applied to database to database comparisons and to multi-layout or multi-database comparisons.

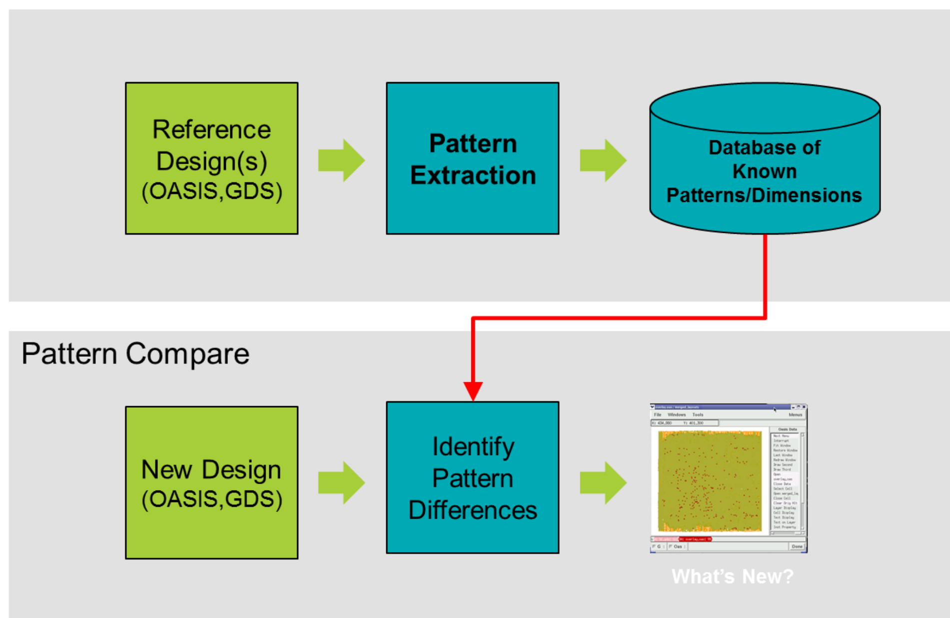

Figure 4. Database to Layout comparison flow

In this approach, one of each representative pattern depicting something that is “new” can be highlighted and flagged in the new design. An example is shown in Figure 5. A location is marked if it is either topologically different or dimensionally different. Topologically different means that a pattern was seen whose topologies had never been seen before. Dimensionally different means patterns whose topologies have been seen, but whose dimensions are different from what has been seen before.

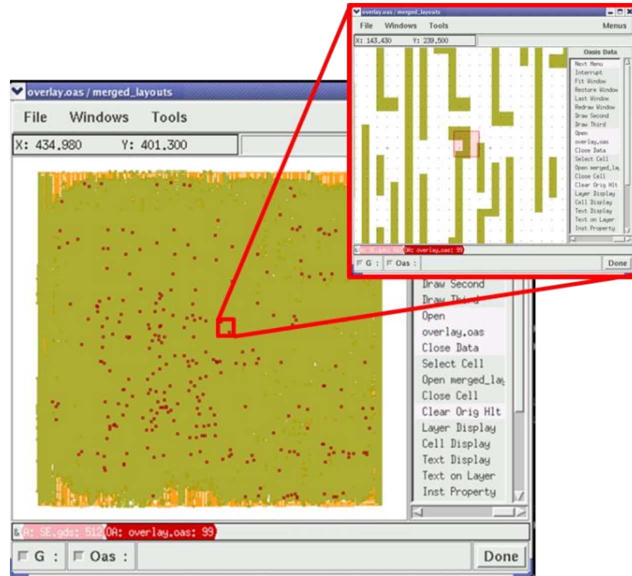

Figure 5. Automatic identification of representative layout differences

A case study of this type of analysis is shown in Figure 6. In this example, a digital block (identified by the arrow) from the design was captured as a reference and all patterns extracted into a database. This database was then compared against the full design. Each red point in the figure is a representative pattern present only in the full design that was not present in the digital block. This ability to identify and highlight layout differences is very powerful with many use cases. OPC engineers can quickly find regions that deserve more analysis. Process and failure analysis teams can use this information to feed forward monitoring point. Generally this data gives an entire team an indication of how difficult a new tape-out will be, especially when ramping up a new process.

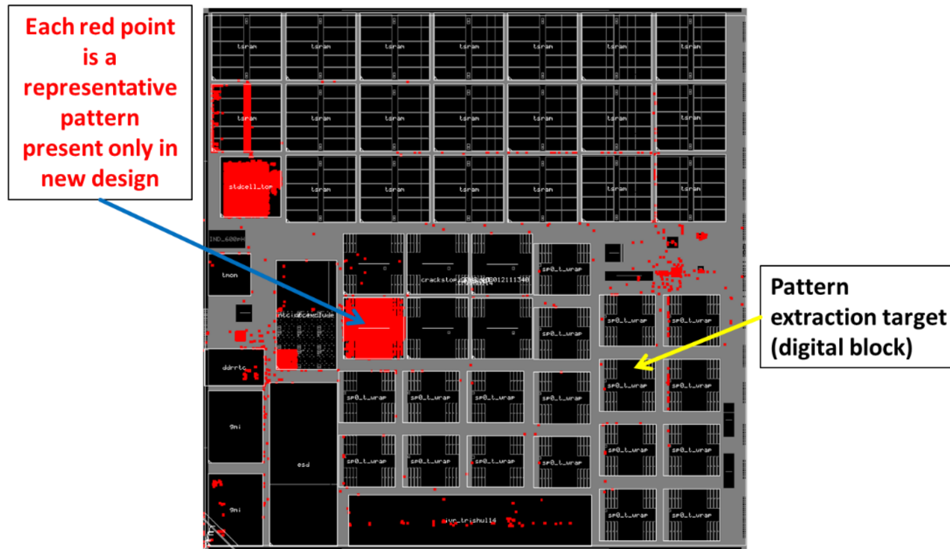

Figure 6. Case study of for identification of representative layout differences

Note how differences become visually apparent. For comparison, the purposes of different regions of the full layout are highlighted in Figure 7. Note especially how the region with core generated with different router settings is highlighted. Further, the region where a different standard cell library was used is also highlighted.

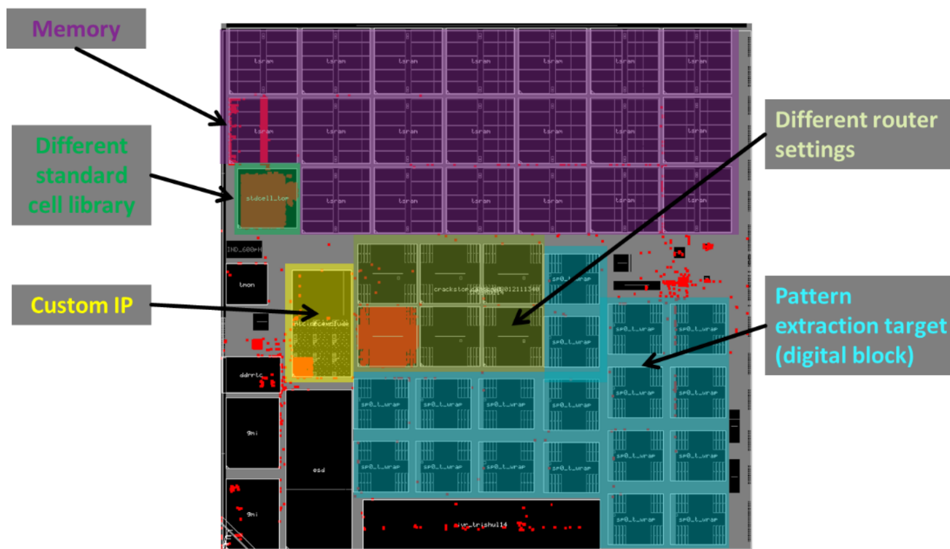

Figure 7. Case study of for identification of representative layout differences (with descriptions of each block)

3. LAYOUT PATTERN EXTRACTION

The pattern extraction process was used to analyze a digital circuit block from the 14nm technology generation. The first three 1x metal layers were analyzed using a window size (diameter) corresponding to three metal pitches. Inexact matching was used and results from all three metal layers were aggregated. A total of 242,617 unique pattern topologies were identified.

Figure 8 shows the distribution of unique pattern topologies among different complexity classes. The simplest topology captured (3×3) is shown in the bottom left and the most complex (10×11) is in the upper right. Note that since pattern rotation or mirroring is not considered a new topology the lower half of Figure 8 would look the same as the upper half (i.e., a 4×5 pattern is the same as a 5×4) and has therefore been omitted for clarity.

For the design being analyzed, the most common pattern topology class was the 6×7 with just over 40,000 unique pattern topologies. There is also 'neighborhood' of other common topology classes surrounding the 6×7 class but dropping off quickly for more complex pattern topologies—for example, 8×8, 7×10, and 6×10 classes all have very few unique topologies in this design.

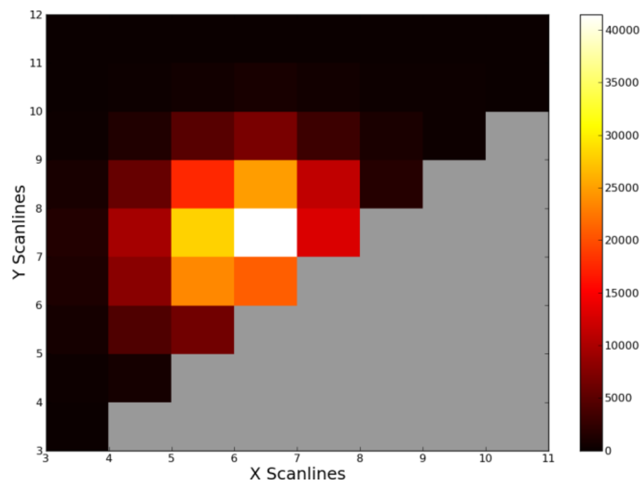

Figure 8. Unique pattern topology counts for a 14nm digital circuit block implemented in a 14nm process technology.

This analysis shows which pattern topology class had the largest number of unique topologies but does not account for the fact that the total number of possible topologies is a function of the topology complexity (i.e., the number of scanlines in each direction or, equivalently, the total number of bits in the bitmap representation). For example, the absolute number of unique 3×3 topologies may be small compared to the 6×7 class, but the total number of possible 3×3 topologies is also much smaller. Table 1 shows the total number of possible patterns for several topology classes as well as a 'reduced' unique topology count in which duplicates and non-physical topologies are removed.

Table 1. Total possible pattern topology space sizes for several pattern topologies (starting with 3×3) based on simple combinatorial methods to enumerate each possible topology. The right column shows the 'reduced' space obtained by eliminating duplicates due to mirroring or rotation as well as any topologies that are not physically realizable (e.g., 'bowtie' shapes). The value in parenthesis represents the percentage of the total possible space that is composed by the 'reduced' space.

X	Y	Total Possible Space	Reduced Space
3	3	512	38 (7%)
3	4	4,096	299 (7%)
3	5	32,768	1,716 (5%)
3	6	262,144	9,044 (3%)
3	7	2,097,152	49,610 (2%)
3	8	16,777,216	267,390 (2%)
3	9	134,217,728	1,452,652 (1%)
3	10	1,073,741,824	7,864,304 (1%)
4	4	65,536	1,900 (3%)
4	5	1,048,576	43,428 (4%)
4	6	16,777,216	479,491 (3%)
4	7	268,435,456	5,202,792 (2%)
5	5	33,554,432	500,948 (1%)

With the unique pattern topology counts for a given physical design and the total possible size of the topology space (Table 1) it is possible to determine the fraction of the available topological space occupied by the layout. Figure 9 shows the fraction of the topological space occupied by a 14nm SOC layout as a function of the topological complexity. While the total available topological pattern space for simple classes such as 3×3 is almost fully utilized the usage drops off quickly as the pattern space expands.

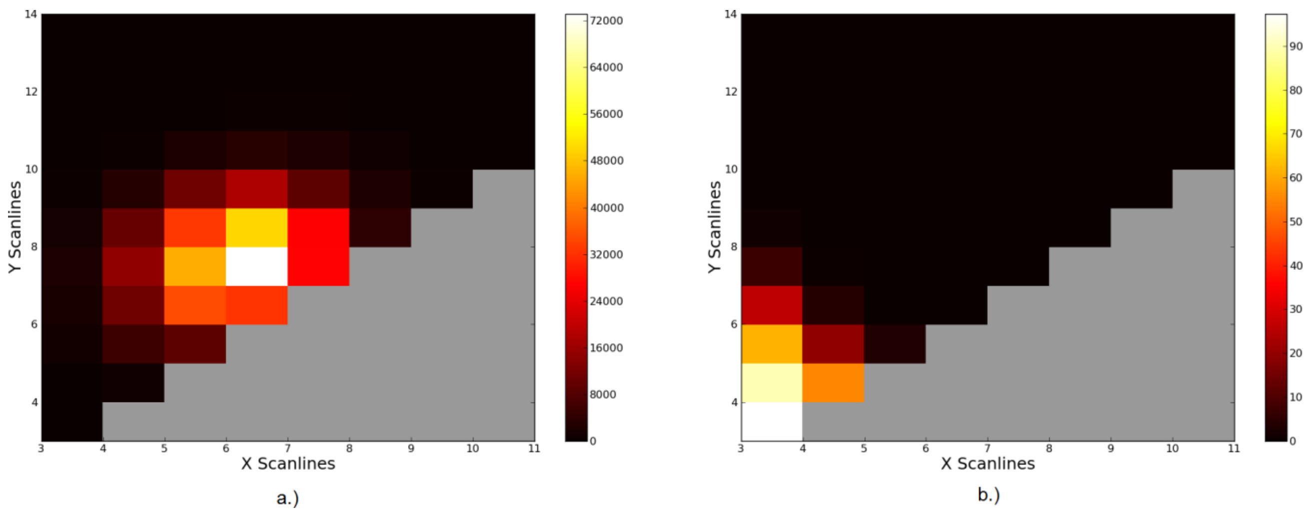

Figure 9 a.) Unique pattern topology count by topology class for a 14nm system-on-chip (SOC) showing a peak count at the 6×7 topology class. b.) Fraction of the total available pattern space (right column in Table 1) utilized by the topologies in the SOC expressed as a percentage. The available topology space for simple classes such as 3×3 is highly utilized but this utilization decreases rapidly as the topological space size increases.

Additional analysis of the unique pattern topologies in a given layout can give insight into the design regularity. The distribution of unique pattern instances for the same digital logic block analyzed in Figure 8 is shown in Figure 10. Over half of the unique pattern topologies have 10 or fewer instances in the layout, and roughly one third of the unique topologies have only a single instance in the layout. This indicates that there are significant opportunities for layout regularization if the topologies with very low instance counts can be converted to more common topologies. This can reduce the number of cases that the patterning process needs to be optimized for and improve overall manufacturability.

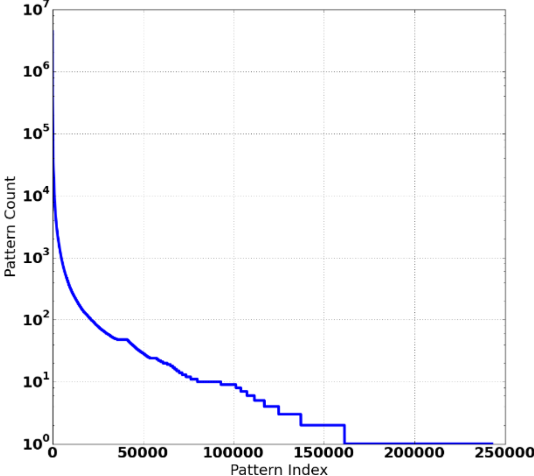

Figure 10. Distribution of instance counts for unique pattern topologies in a 14nm digital logic block.

Finally, the topological pattern extraction was used to study the evolution of design complexity from technology generation to generation. The same 14nm digital logic circuit block from Figure 8 was also implemented in 28nm and 20nm process technologies. The pattern extraction process was repeated scaling the window size to three minimum metal pitches as defined in each technology and the first three metal layers were considered together in each case. The results are shown in Figure 11 below. The total unique pattern topology counts for each technology are also shown in Table 2.

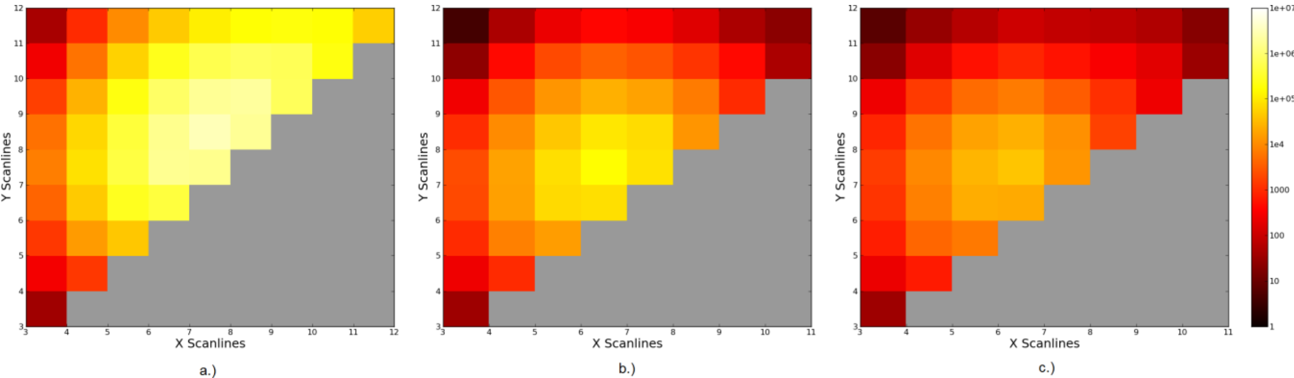

Figure 11. Extracted pattern topology counts for the same digital circuit block implemented in a.) 28nm, b.) 20nm, and c.) 14nm process technologies. Note that the color scale is logarithmic.

Table 2. Total count of unique patterns in the same digital circuit block implemented in three different technology generations. The first three 1x metal layers are considered with a window size corresponding to three minimum metal pitches in each technology.

Technology Node	Total Unique Patterns
28 nm	20,718,038
20 nm	835,017
14 nm	242,617

This data shows a general decrease in design complexity from 28nm to 20nm to 14nm. The most significant change occurs from 28nm to 20nm, where there is a decrease of more than one order of magnitude in the total number of unique pattern topologies. In addition, the pattern class with the highest count of unique patterns shifts from 7×8 at 28nm to 6×7 at 20nm, indicating that the more complex pattern topologies are becoming less common at 20nm compared to 28nm.

The most likely explanation for such a significant difference is twofold. First, the transition from single patterning lithography at 28nm to double patterning at 20nm led to stricter design rules (for example, small metal "jogs" were no longer allowed) and therefore increased regularity. Note that in this analysis the metal layers were treated as a single "gray" layer—that is, decomposition or "coloring" was not considered and only the target metal pattern on the wafer was analyzed. A second factor responsible for the large decrease in metal pattern complexity was the adoption of local interconnect for intra-cell connections. This shifted a significant portion of the tight connections within a cell from the first and second metal layers to the local interconnect, allowing for improved regularity of the metal patterns.

An additional decrease by a factor of approximately four is observed between 20nm and 14nm. Although the back-end-of-line (BEOL) design rules for the metal layers are very similar between the two, 14nm saw the introduction of FinFET devices as a replacement for planar transistors. This led it increased regularity of the front-end-of-line (FEOL) layers due to the discrete device width nature of FinFET transistors and it is likely that this increased regularity carried over to the first metal layers to some degree.

4. TOPOLOGICAL LAYOUT COMPARISON

Once the pattern extraction process is complete and unique pattern topologies are identified it becomes possible to compare the set of patterns from two different designs to find out which patterns are different between the two. In this case, 'different' can have two meanings: a pattern topology can be unique to only one design, or the pattern topology may be common between the two designs but have dimensional values that are unique to only one design. For example, at the end of Section 3 it was shown that a digital design implemented in 14nm had approximately one-fourth the number of unique pattern topologies as the same circuit implemented in a 20nm technology. This raises the question of whether the patterns found in 14nm are also found in 20nm (i.e., they were carried over from the previous generation) or if they are new patterns that have not been seen before.

By comparing the extracted pattern databases for the two designs it is possible to answer this question and the results are shown in Figure 12. In this case, roughly two-thirds of the patterns in 14nm were also found at 20nm while the remaining one-third are new patterns.

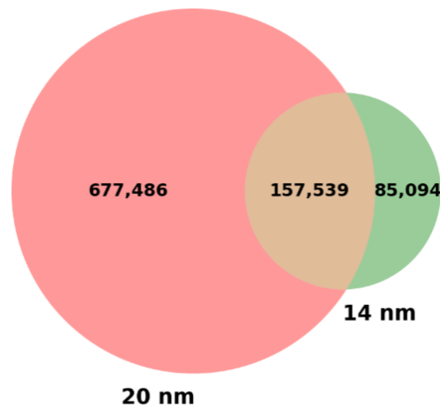

Figure 12. Venn diagram showing the relationship between unique pattern topology sets for a digital circuit block implemented in a 20nm process technology and the same circuit implemented in 14nm.

A similar application is to compare extracted pattern sets between designs of the same technology generation. For example, it may be of interest to compare the patterns that exist on a test chip with the patterns for the lead product to see how many new patterns there are. This analysis was performed on a 14nm test chip and a graphics processing unit (GPU) product designed for the same technology and the results are shown in Figure 13.

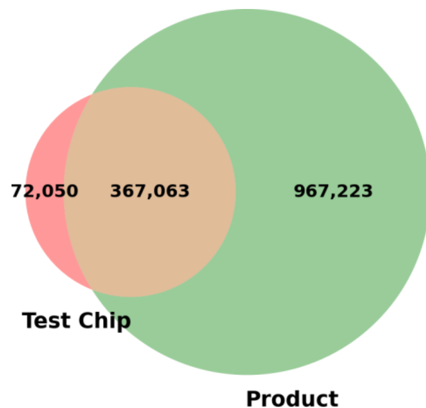

Figure 13. Venn diagram showing the relationship between extracted pattern topology sets in a 14nm test chip and product. This analysis considered three 1x metal layers with a window size of three minimum metal pitches.

As Figure 13 shows, there are significant differences between the test chip and the product with respect to the extracted pattern topologies. On one hand, a large majority of the patterns contained in the test chip design are also present in the product layout. This indicates that the test chip is representative of the product design style. However, there are a large number of additional patterns in the product design that were not present on the test chip. This represents a manufacturing risk if the product patterns were not verified on a different chip.

While there is no guarantee that the new patterns will fail, they do represent new patterns that may not have been seen in the fab before and therefore the process may not be optimized to pattern them successfully. Additional analysis may be required to understand the distribution of pattern counts for the new patterns. For patterns with high usage rates, the best option may be to inform the fab as soon as possible so that efforts can be made to validate the pattern in simulation and adjust the design targeting and optical proximity correction (OPC) as needed to ensure manufacturability. In the case of patterns with low usage in the design a better approach may be to eliminate the pattern from the design (replacing it with another pattern that is already validated in silicon and/or occurs more commonly).

It is also informative to compare extracted pattern sets for different product types to compare design style differences. Figure 14 shows such a comparison for three 1x metal layers from a 14nm GPU, a central processing unit (CPU) and an accelerated processing unit (APU) SOC containing CPU cores and GPU capability as well as Northbridge, memory controller, display interface controllers, and a host of other content. This represents a wide variety of design styles and purposes including digital logic, memory, analog/mixed-signal, and other types. As a result the extracted pattern topologies should be expected to cover a wide range of typical styles for the technology node.

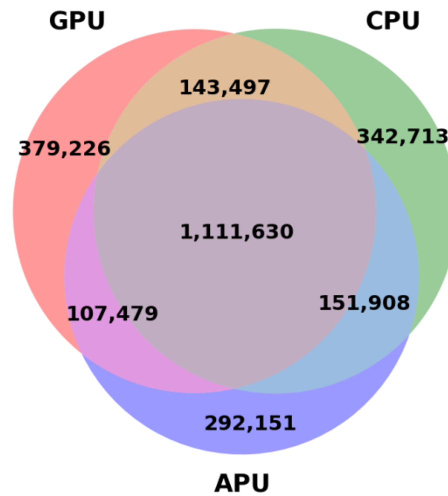

Figure 14. Venn diagram showing the relationship between extracted pattern topology sets in a 14nm CPU, GPU, and APU. This analysis considered three 1x metal layers with a window size of three minimum metal pitches and inexact topology matching was used.

As might be expected there is broad overlap in the extracted pattern sets among the three product types. However, there are significant differences as well. There are hundreds of thousands of topologies that are found in two of the product types but not the third, and over one million topologies that are unique to only one product type. Note that Figure 14 uses inexact topology extraction—that is, only differences in topology are considered and not differences in the dimensions of individual topology instances. When specific dimensional values are included in the analysis through exact topology extraction the differences become even more dramatic as shown in Figure 15.

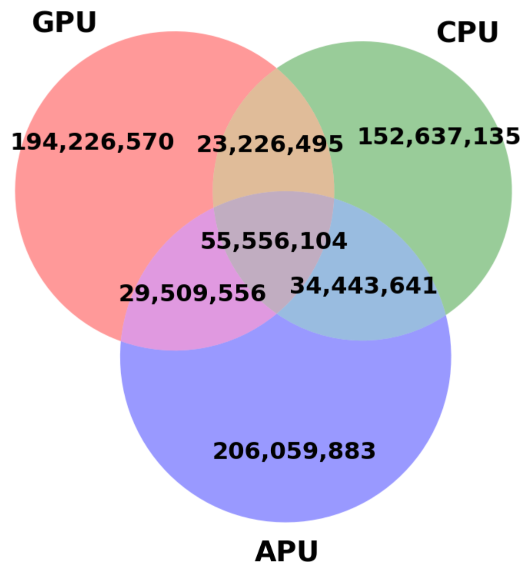

Figure 15. Venn diagram showing the relationship between extracted pattern topology sets in a 14nm CPU, GPU, and APU. This analysis considered three 1x metal layers with a window size of three minimum metal pitches and exact topology matching was used to consider dimensional as well as topological differences between patterns.

Significant differences in pattern topologies used can even be seen between different chips of the same product type and implemented in the same process technology. Figure 16 shows a comparison between the extracted pattern topology sets for two GPU products implemented in the same 14nm process technology.

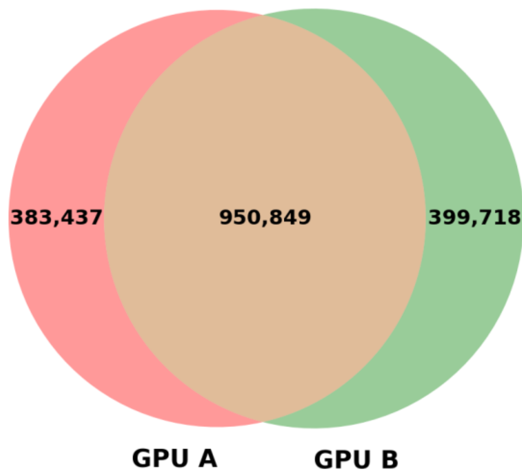

Figure 16. Venn diagram showing the relationship between extracted pattern topology sets in two different 14nm GPU products. This analysis considered three 1x metal layers with a window size of three minimum metal pitches.

Both chips consisted primarily of digital logic and memory blocks. The designs were completed at approximately the same time and used a nearly identical digital design flow and the same RTL for many of the circuit blocks. Again, as expected, there is broad overlap between the pattern topology sets for 1x metal layers between the two. However, there are also significant differences. In this case, the differences are primarily due to the fact that the two products are targeted for slightly different market segments. One chip is focused on a high-performance market and therefore used

wider power rail features, while the other GPU is targeted at a mobile market where cost and power are the key considerations and as a result narrower power rails were used. The differences in the power grid resulted in different solutions from the router tool and these differences show up as unique pattern topologies in the comparison in Figure 16.

5. CONCLUSION

In summary, topological pattern analysis provides a powerful tool for measuring and comparing physical design complexity. The use of pattern extraction to identify all unique pattern topologies (with or without specific physical dimensions) was demonstrated, and a measureable decrease in 1x metal design complexity from 28nm to 20nm to 14nm was observed. This confirms the expectation that layouts are becoming more regular as the number of physical design restrictions increases. A sample distribution of unique topology usage shows that the distribution has a "long tail," i.e., many patterns that are used very infrequently compared to the more common patterns.

The extracted pattern topologies were used to compare layout and identify differences and commonalities. Significant differences were observed between a test chip and a product as well as between different products in the same process technology. This information may be used to identify potential risks for manufacturability that should be monitored and controlled in the fab. In addition, "outlier" patterns may be targeted for removal from the design, improving the overall design regularity.

6. FUTURE WORK

The approach described in this study demonstrates that it is possible to quantify and compare pattern topologies for full chip designs. There are a number of futures studies based on this approach. This approach can be applied to other layers including studies of multi-layer pattern topologies. Of particular interest are the front end of line layers, especially studies of how these layers are used in standard cell layout design. Additionally, there is a rich area of exploration regarding further analysis of the areas that have been highlighted as different. Some simple approaches include further categorization of those differences by frequency of usage. More complex approaches include applying a combination of pattern matching, DRCs, and simulation to further refine and highlight patterns that are potential yield limiters.

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