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Addressing Test Cost Challenges in LPCT Designs

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As companies strive to achieve higher quality and reliability for their products, and as package sizes and the number of available pins continue to shrink, there is also a persistent need to keep test costs down. Low Pin Count Test (LPCT) is one solution that Design for Test (DFT) designers turn to, and in many cases, might be the only one available to address these conflicting requirements. The overall test vector set applied during wafer and manufacturing test is often dominated by Automatic Test Pattern Generation (ATPG) patterns for digital and mixed-signal designs. Reducing ATPG test data volume and test time can significantly impact the overall test cost of these products. Cadence® Encounter® Test SmartScan offers a unique LPCT scan compression architecture to meet these challenges.

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Why LPCT?

There are several factors driving designs to LPCT solutions, including the number of digital pins available, the use of very-low-cost testers (VLCTs), multi-site testing, and limited test pin budget.

In many mixed-signal designs and especially in automotive and micro-controller units (MCUs), package sizes are getting smaller and the number of pins being bonded out are fewer. As most of these pins are shared by analog, power, and ground, the digital pins available for test are at a premium.

Companies are also increasingly adopting VLCTs to keep their test hardware cost down. There is limited memory and probe pins on these kinds of testers. Sometimes, even though the number of pins on the package dedicated to manufacturing test might be higher, due to the cost of probes during wafer test, very few of them are actually used.

Multi-site testing is a technique where a large number of dies are tested in parallel to increase silicon test throughput. The stimuli is stored on the tester and applied concurrently to all the dies on the test board and compared against the response data. To achieve multi-site testing of 16X, 32X, 64X, or 128X, the number of tester-contacted pins must be very low. The overall tester data and the test time saved by switching to multi-site test are enormous.

As the number of IP cores used in a system-on-chip (SoC) design grows, additional requirements are placed on complex test methodologies such as hierarchical test compression. Test access to individual cores via the test bus helps to quickly isolate problems on the tester. The test pin budget allocated for the SoC is shared between all of the cores.

Limitations of Conventional Test Compression

Scan test compression is the most commonly used DFT architecture to reduce ATPG patterns test time and test data volume. Traditional compression structure includes a broadcast/XOR network of the scan-input pins and XOR/multi-input shift register (MISR) logic on the scan-output pins. The long-scan chains are broken up into a number of scan channels, also known as stumps, and connected to the compression logic. The ratio of the number of scan channels to the external fullscan chains is referred to as the target compression ratio. When the scan chains are properly balanced, they can achieve test time and test data volume reduction close to the target ratio. In many designs using an XOR compression architecture, DFT engineers can expect to achieve 100X compression efficiency, and with MISR compression, up to 200X compression efficiency.

The compression efficiency and the fault coverage is reduced as the number of scan data pin pairs available are less than five, as shown in Figure 1. The data correlation on the scan-input increases, resulting in fewer unique values feeding the channels. The probability of data aliasing on the scan-output also starts increasing, which can result in failures being masked out, thus leading to lower reliability of the test patterns.

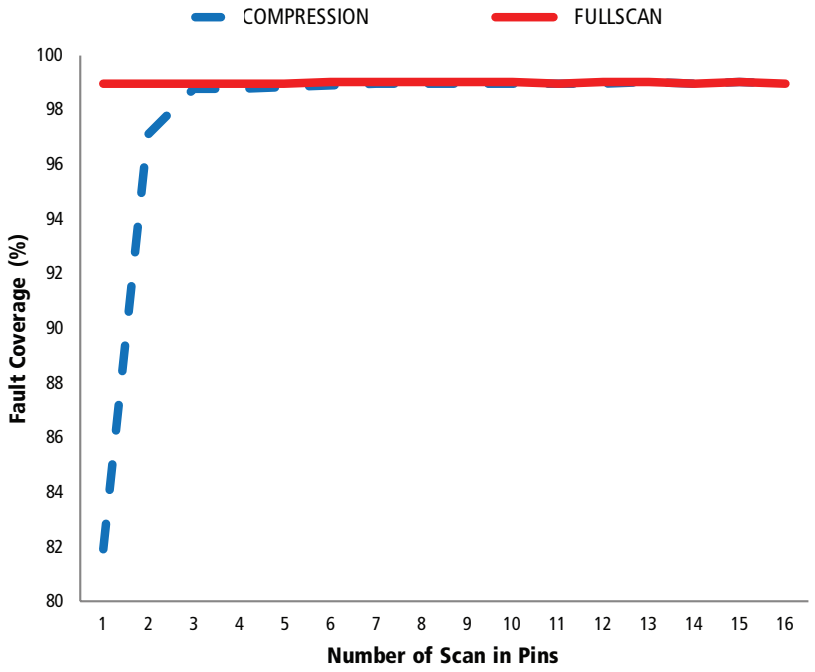

Figure 1: Lower number of scan-in pins results in lower coverage achieved

LPCT designs requiring scan compression to reduce test time and test data volume cannot directly implement the traditional architectures and expect to maintain a high quality of test.

Encounter Test SmartScan

Cadence Encounter Test offers a new scan compression solution—Encounter Test SmartScan—to address the growing challenges of LPCT designs. The Encounter Test SmartScan architecture provides all of the advantages of XOR compression (high efficiency, very good QoR, easy to diagnose) via a single scan-in/scan-out pair. Two N-bit shift registers are introduced to deserialize and serialize the compressed test data, as shown in Figure 2. It takes N cycles to load the input shift register (deserializer) with the compressed data for a single bit-slice of the scan channels. Once the deserializer is loaded, the scan clocks are fired and data is transferred into the internal scan channels. Similarly, the output serial shift register (serializer) does a parallel capture of the functional response data from the internal scan channels and serially shifts it out.

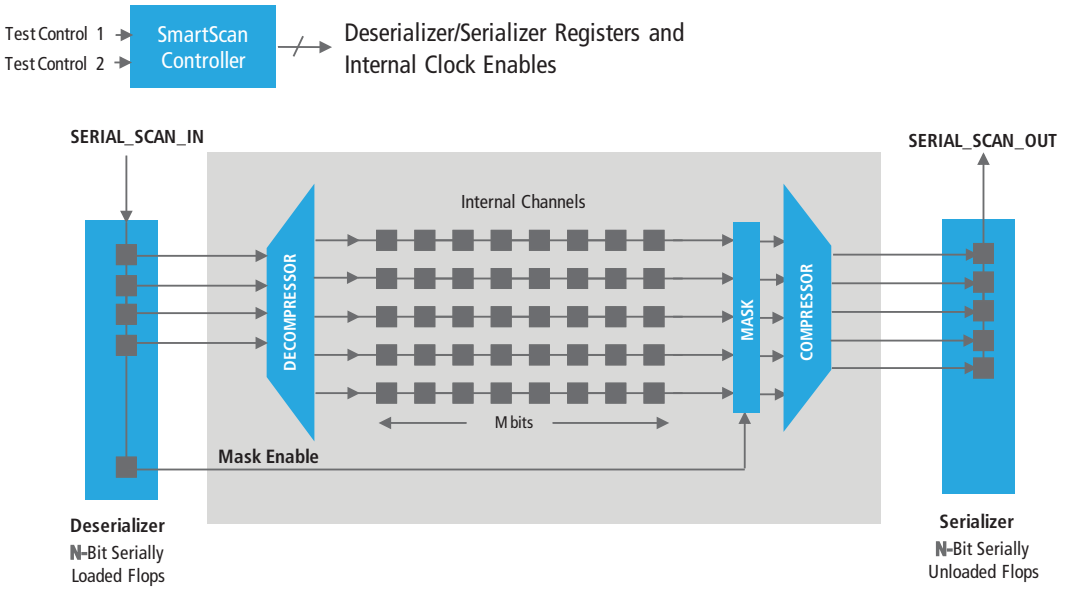

Figure 2: Encounter Test SmartScan compression

One of the key aspects of the Encounter Test SmartScan architecture is that the test patterns are generated using the N-bit wide parallel scan interface by bypassing the de/serializer registers, as shown in Figure 3. These patterns are then re-targeted to the Encounter Test SmartScan serial interface by translating each scan cycle of the parallel interface pattern into loading and unloading the de/serializer registers. In addition to the serial patterns, the parallel interface patterns can be directly applied at the automated test equipment (ATE) if the chip package provides for these pins to be available for test. If the design does not contain these pins, the parallel interface is modeled for test-generation purposes. The test control signals required to switch between parallel and serial interfaces can be internally decoded from on-chip test logic.

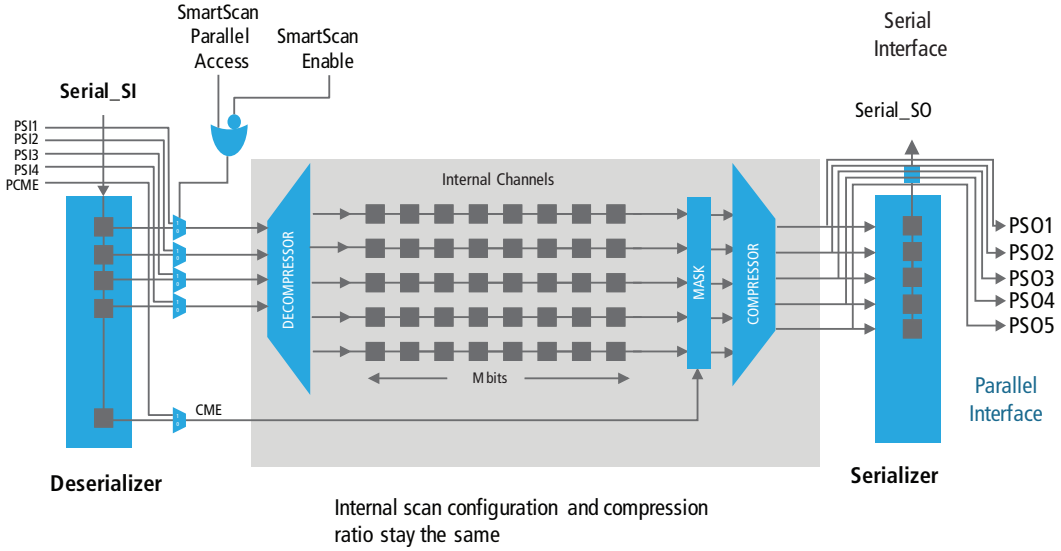

Figure 3: Encounter Test SmartScan compression showing parallel and serial interface

The advantages of using this parallel interface are manifold:

- Because mainstream DFT verification and pattern generation process are independent of the Encounter Test SmartScan hardware, the Encounter Test SmartScan logic is verified in the context of post-ATPG pattern retargeting, and thus avoids expensive re-iteration of DFT verification and ATPG flows due to any errors in its implementation

- Large reduction of scan data correlation that would be otherwise caused by having only very few pins drive the compression logic directly
- Since the internal scan configuration is identical between the serial and parallel interfaces, a one-pass ATPG run is sufficient and the pattern quality is identical
- Debug and diagnosis is minimally impacted as Encounter Test diagnostics can isolate tester failures using the parallel interface by simply translating serial pattern fails to the corresponding parallel cycles

Figure 4 illustrates the advantage Encounter Test SmartScan has on fault coverage and test time on an automotive design. The design has one scan-input/scan-out pair available for scan test. If conventional XOR compression is used, due to the correlation effects, the quality of ATPG patterns is drastically lower compared to using a single-scan chain (fullscan). However, the test time impact in fullscan mode is very high due to much longer chain length. By adding an 8-bit wide Encounter Test SmartScan logic into the design, the fault coverage achieved can be very similar to the fullscan mode with a much lower test time. The test time for each Encounter Test SmartScan pattern is eight times longer than a single compression pattern, due to the deserializer shift. If the tester can supply a clock that is up to eight times faster than scan frequency, then the overhead due to the deserializer shift is nullified and the total test time is further reduced.

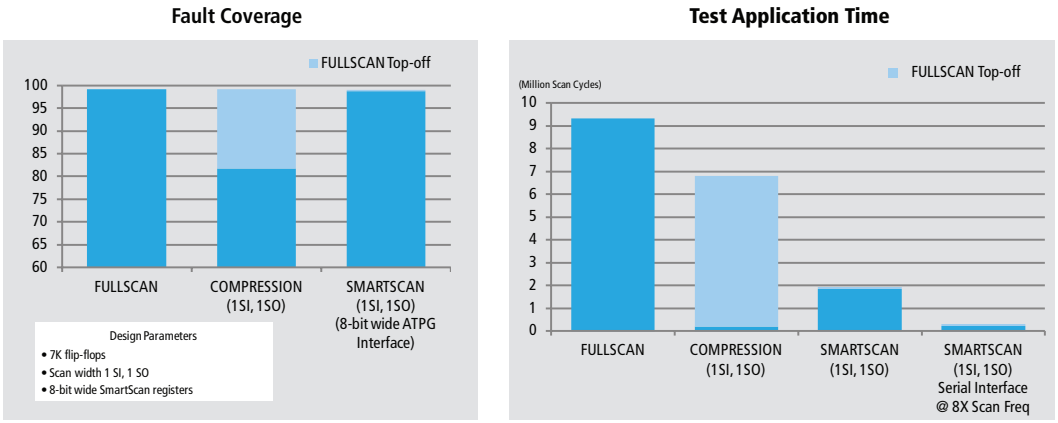

Figure 4: Results from an automotive design

Insertion and Validation of Encounter Test SmartScan

Insertion and connection of the Encounter Test SmartScan logic into the front-end design netlist is fully automated within the Encounter RTL Compiler cockpit. A single logic-synthesis and DFT-insertion run script is used in the Encounter RTL Compiler to achieve the best area, timing, power, and test coverage results. The Encounter RTL Compiler generates all the downstream run scripts to verify design equivalence with Cadence Conformal® LEC, generate parallel interface patterns and retarget them for Encounter Test SmartScan interface, and provide fault coverage metrics with Encounter Test True-Time ATPG. A flow is also provided to validate the ATPG patterns in Cadence Incisive® NcVerilog simulation, as shown in Figure 5.

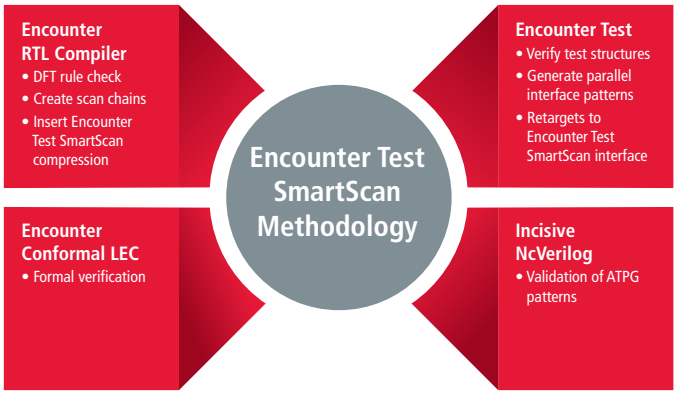

Figure 5: Overview of Encounter Test SmartScan methodology using Cadence tools

Conclusion

Encounter Test SmartScan compression from Cadence is an ideal solution to help meet the LPCT challenges by providing the ability to target high-quality ATPG patterns via a single scan-input scan-output interface. The ease of use, one-pass Encounter Test SmartScan insertion, ATPG, and diagnosis makes it an effective technique in reducing the test cost for mixed-signal, automotive, and MCU designs.

Further Information

Learn more about Cadence's DFT offering at www.cadence.com/products/ld.