QuickView Signoff Data Analysis Environment

Easy-to-use, high-performance, and standalone chip-finishing system

Cadence® QuickView Signoff Data Analysis Environment is an easy-to-use, high-performance, and standalone chip-finishing system that supports multiple formats of design, layout, and manufacturing data. The QuickView Signoff Data Analysis Environment loads large layouts (GDSII, OASIS®, LEF/DEF, and manufacturing formats) in seconds and provides a rich set of debugging features, including net connectivity tracing, visualization, overlay, and GDSII/OASIS editing.

Overview

With the QuickView Signoff Data Analysis Environment's high capacity, users can load extremely large layouts in seconds. The QuickView Signoff Data Analysis Environment's signoff analysis environment allows users to place multiple layouts in one canvas and perform a range of chip-finishing functions.

The QuickView Signoff Data Analysis Environment is tightly integrated with the Cadence Physical Verification System (PVS) platform, and offers similar use models and flows to PVS in Cadence Encounter® and Cadence Virtuoso® platforms in a standalone capacity. It also works with third-party implementation and verification tools. The QuickView Signoff Data Analysis Environment's high performance offers design and manufacturing teams a fast and extensible environment for efficient tapeout and chip finishing.

Benefits

- Multi-format display enables viewing and superimposing of design data in any of its intermediate representations throughout the chip-finishing process
- High-performance, high-capacity data viewing with powerful options allows the full range of display, from deep sub-micron features to full reticle-level or full wafer databases
- Intelligent overlay and graphical XOR capabilities make graphical comparisons of data easy by providing an additional element of decision support
- Graphical verification of reticle designs based on the actual data used in mask manufacturing eliminates expensive jobdeck errors and improves the predictability of cycle times
- Flexibility enables coordinate scaling, offsetting, rotation, and/or mirroring for overlaying and comparing multiple datasets

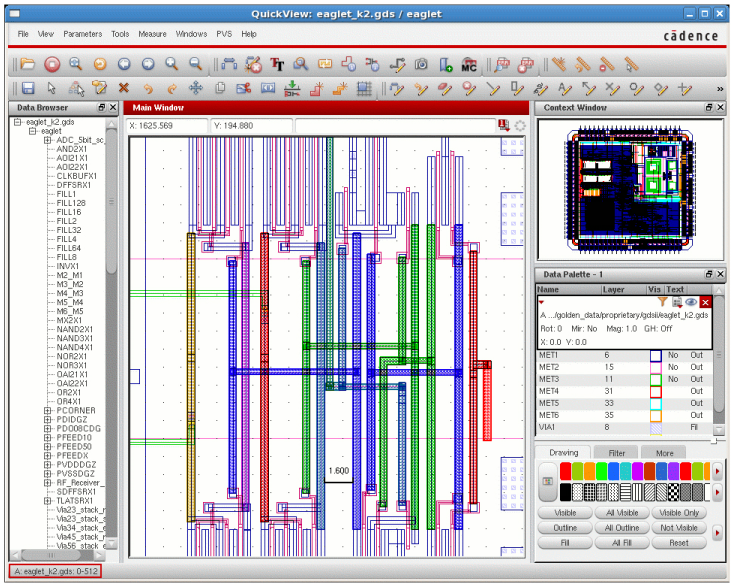

Figure 1: QuickView Signoff Data Analysis Environment

- Enables fast and powerful measurement and analysis
- Error browsing offers efficient and generic means of displaying and stepping through DRC error diagnostics results
- Overlay of common image formats allows graphical comparison with design and manufacturing data.s
- Accepts industry-standard formats
- Includes a full-featured macro language for the development of custom viewing and data inspection applications

Features

Multiple layout formats

- Supports multiple layout formats:
  - GDSII
  - OASIS
  - LEF/DEF
  - OpenAccess
  - LAFF
  - GL/1
- Can be viewed concurrently to verify changes, alignment, or interaction without the worry of cell name collisions
- View and inspect in any mirrored, rotated, scaled, and offset combination
- Supports advanced query and automatic stepping functions for locating and inspecting cell references, geometries, and annotations
- View in normal or reverse tone
- Rapid access to general statistics

PVS integration

- PVS integration enables job submission and DRC, XOR, LVS, and ERC debuggers within the single environment
- Error browsing and LVS/ERC data (cross) probing is interactive even for large layouts and error databases
- Imports and applies Virtuoso Tech files to loaded data

Multiple manufacturing formats and jobdecks

- Supports leading manufacturing formats:
  - MEBES through Mode 5 (data, jobdecks)
  - JEOL 1.0, 1.1, 2.1, 3.0, and 3.1 (data and jobdecks)
  - Toshiba VSB 11and 12 (data and jobdecks)
  - HL800, HL900, and HL950 (data)
- Stripe and segment boundaries, as well as virtual addressing, may be superimposed on the pattern data
- Can be viewed and inspected in any mirrored, rotated, scaled, and offset combination
- Supports advanced query and automatic stepping functions for locating and inspecting cell references, geometries, and annotations
- Rapid display of complete mask or reticle data in fractured format using manufacturing-ready jobdecks and appropriate data files

Robust signoff analysis environment

- Connected geometries can be identified, highlighted, and analyzed based on layer-to-layer connectivity definitions
- Provides point-to-point path analysis through identified connected geometries
- Merges multiple databases
- Converts between common database formats
- Replaces cells in one GDSII DB with cells from another GDSII DB
- Supports direct geometrical modifications to GDSII data and saves the output

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or internet—they can also provide technical assistance and custom training
- Cadence-certified instructors teach more than 80 courses and bring their real world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet

For more information, log on to www.cadence.com or email k2_support@cadence.com

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