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Expanding Manufacturing Verification to the Real World with LBIST

By Dale Meehl, Cadence Product Engineer

To achieve and exceed the key quality metrics for automotive devices, such as safety standards ISO 26262 and AEC-Q100, engineers are rethinking how Design for Test (DFT) methods can be re-used to test their designs throughout the chip's lifespan. This requirement has driven resurgence in the need for logic built-in self test (LBIST), a mechanism that tests the functional logic of a chip. Cadence® Encounter® Test LBIST offers a unique solution in this space.

Contents

Overview

As an increase in growth of automotive digital logic occurs, a growing need for field-level testing is becoming a requirement. Temperature, movement, and silicon aging are stressing and challenging mission-critical designs that don't have the luxury of having a clean room tester environment to validate that the logic is still functioning as originally tested. The ability to perform field-level tests to ensure the digital logic is still functioning correctly is emerging as a safety standard.

LBIST is a mechanism that tests the functional logic of a chip in a way similar to that of the more common memory BIST (MBIST), which tests the RAM and ROM contents. The LBIST macro includes a pseudorandom pattern generator (PRPG) and a multiple-input shift register (MISR). The LBIST macro generates stimulus derived from a seed in the PRPG and provides known stimuli to all the scan elements through scan channels. A built-in state machine then allows capture clocking to occur (static and at-speed testing) to test the users' logic. The captured values are then scanned into the MISR, where the values are combined with the prior captured values. The final MISR's "signatures" are checked to verify the expected operation of the circuit.

The Need for LBIST

With the explosion in the growth of the automotive semiconductors industry comes an associated and intense focus on high silicon quality and reliability. The last thing anyone wants is a brake system failure due to a latent silicon defect, and concerns over reliability are driving changes in the testing requirements for these chips. The electronics must meet certain safety standards set forth by the automotive manufacturers, such as ISO 26262 and AEC-Q100, which outline acceptable failure rates for key functionality. Electronic providers must detail how their hardware and software will meet these standards before they are accepted.

To achieve and exceed the key quality metrics for automotive devices, engineers are rethinking how DFT methods can be re-used to allow the testing of their designs throughout the chip's lifespan. This requirement has driven a resurgence in the need for LBIST. In an automotive chip, on-board LBIST can enable a very effective system power-on test that ensures the silicon is functioning as required each time the vehicle is started, with LBIST logic coverage typically falling in the range of 75-80%.

In a typical application, if the LBIST test signals a silicon failure, an associated error code is posted to the vehicle computer and the "check engine" light comes on. In this way, LBIST provides the means to quickly and easily identify potential safety issues without needing dedicated and complex equipment at car dealerships.

Another benefit of LBIST is that it provides a low pin interface and very small test data volume when testing the chip on the tester. With pin interfaces down to the JTAG pins + oscillator input, multi-site testing can be used to provide an efficient and high first-pass quality check of the silicon.

The Benefit of Testpoints

Because LBIST uses PRPG, it is often difficult to achieve high coverage without the addition of control or observation points in the design. Adding testpoints for controllability or observability is something designers often shy away from, as it adds silicon area and timing delay to the design. But adding testpoints has been proven to be a viable solution when these testpoints are optimally chosen and placed. Using a tool to choose the location of these testpoints and their relative value is needed.

The process of using random resistance fault analysis (RRFA)—such as that available in the Cadence Encounter Test DFT Architect product as an add-on option to Encounter RTL Compiler—and automation to insert the suggested testpoints makes the process of increasing test coverage for LBIST a simple step. Analysis can be performed early in the design process and used to determine whether testpoints are needed. For smaller automotive designs, even a couple of test points can provide a large coverage improvement.

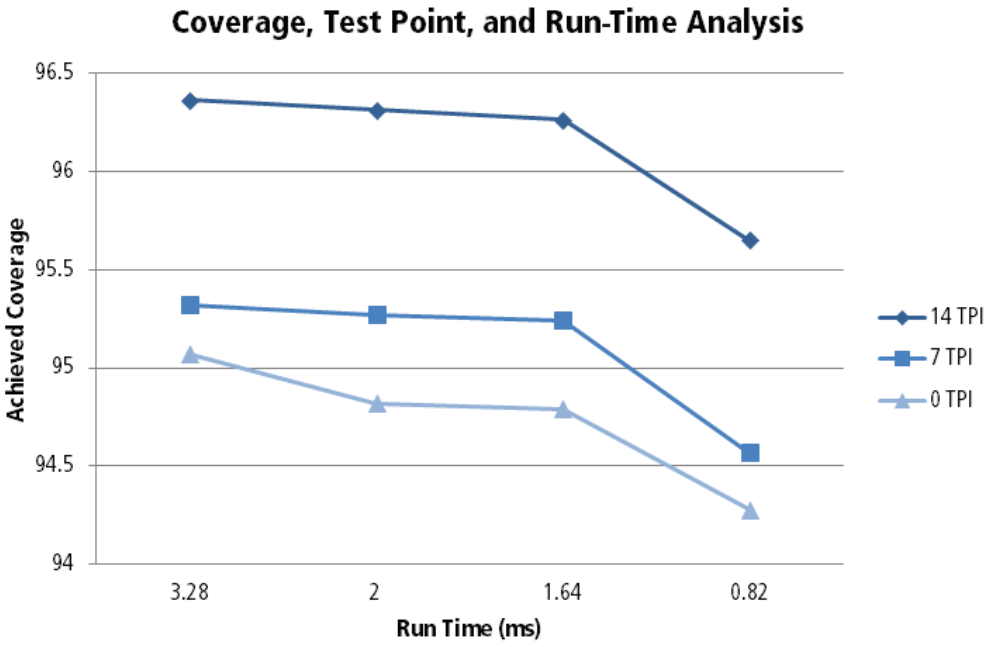


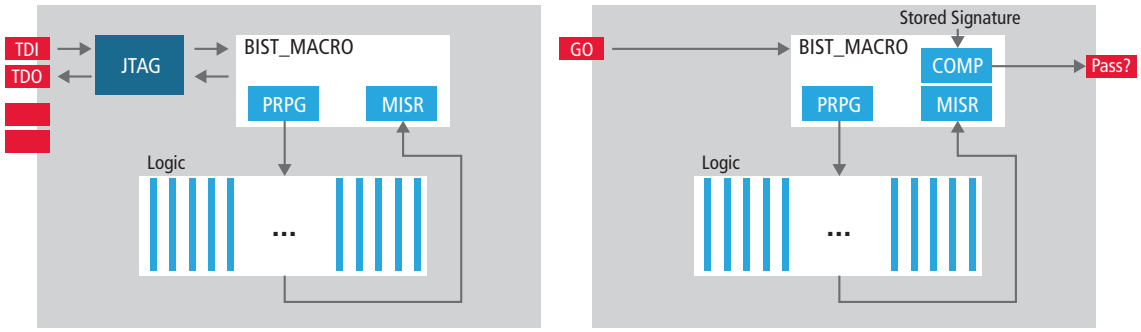
Figure 1: LBIST coverage at different run times and test points inserted

Types of LBIST Supported

The Encounter Test LBIST Option to Encounter RTL Complier supports two different interfaces to LBIST, Direct Access LBIST and JTAG LBIST.

Direct Access LBIST is easily executed by holding a pin high. The MISR signatures are compared with stored internal values and a simple go/no-go response is provided to determine if LBIST has finished successfully. The smallest form factor for the Direct Access LBIST macro starts with 100 flip flops (1650 2-input NAND equivalent gates) and upward. This solution is common in the automobile industry as it provides a simple interface with high-quality results.

As implied by the name, JTAG Access LBIST uses the JTAG interface and protocols to start and execute LBIST. The signatures are compared off-chip in a higher level service processor or board-level devices. The JTAG solution allows the means to customize the LBIST parameters in the silicon to run different testing scenarios. The smallest form factor for the JTAG Access LBIST starts from 160 flip flops (2380 2-input NAND equivalent gates) and upward. In order to achieve a fast-running LBIST, the LBIST macro area must be increased to accommodate more scan channels and ideally shorter ones.



JTAG Access LBIST

- LBIST is started using JTAG commands
- Signatures are read and compared using TDO
- Allows for changing:
  - PRPG seeds, channel masking, and OPCG clocking
  - Number of iterations, scan length, capture window, scan frequency

Direct Access LBIST

- LBIST is triggered by holding a pin high
- Signatures are compared with stored internal values
- Receive a go/no-go response
- No customization in the hardware

Figure 2: LBIST types comparison

LBIST Design Insertion and Validation

Insertion and connection of the LBIST macro into the front-end design netlist is fully automated within the RTL Compiler (RC) cockpit. A single logic synthesis and DFT insertion run script is used in RC to achieve the best area, timing, power, and test coverage results. RTL Compiler also generates all the downstream run scripts to verify design equivalence with Cadence Conformal® LEC, generate test patterns, signature, and fault coverage metrics with Encounter Test True Time ATPG, and MISR signature verification with Cadence Incisive® ncverilog simulation.

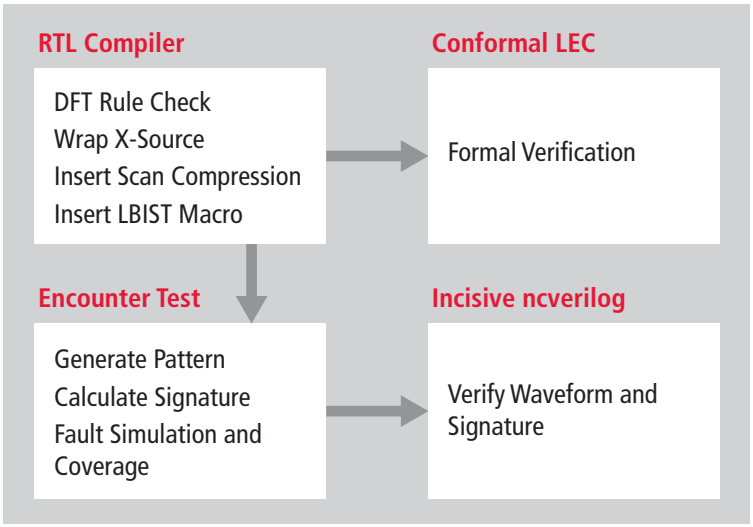


Figure 3: LBIST insertion and validation flow

Conclusion

In summary, the Cadence Encounter Test LBIST solution is ideal for field and system testing throughout the product life cycle, as well as fast manufacturing test bring up. The direct access LBIST implementation makes it unique for mixed-signal and pin-limited designs such as automotive. With small area overhead and the ability to target specific run times, designers can achieve their test goals in system environments.

Further Information

Learn more about Cadence's design for test offering at www.cadence.com/products/ld.

For case studies and more information on the benefits of testpoints, please refer to the tech brief "Meeting Failure Rate Goals in Automotive Electronics" at www.cadence.com/rl/Resources/technical_briefs/DFT_tb.pdf.

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