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# Faraday Technology and Cadence

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Kun-Cheng Wu, Associate Vice President, SoC Development and Service, Faraday Technology

## The Customer

Faraday Technology Corporation (Faraday) is a leading fabless application-specific integrated circuit (ASIC) and silicon intellectual property (SIP) provider. It is one of the few leading ASIC / system-on-chip (SoC) vendors with a comprehensive, self-developed IP portfolio. These IP blocks help lower customers' integration risk and IP licensing costs, while shortening time to market. Furthermore, with its many years of experience in IP development, Faraday is equipped with robust IP customization flexibility and capabilities to meet customers' specific requirements, in terms of power, size, and performance.

Established in 1993, Faraday has been acknowledged and applauded for its expertise and capabilities, with thousands of successful designs in a wide range of applications, covering consumer electronics, video (security surveillance), multimedia, flat-panel displays, communication, networking, and PC peripheral/storage, along with hundreds of millions of ASIC chips shipped annually worldwide.

SoCs are undoubtedly becoming more complex and more integrated. To help customers tackle their SoC design challenges, Faraday provides expertise in the areas of IP, IP integration, IP verification, and hardware/software co-design at the system level, rather than at the chip level only. Faraday also takes the system level into consideration at the initial design stage, and provides Faraday-developed SoC platforms. The objective is to deliver high-quality and reliable solutions within the most competitive schedule. Until now, these platforms have facilitated many projects, including a highly complex, 300-million-gate SoC at the 40nm process node.

### Business Challenge

- Produce prototype of highly complex, 300-million-gate SoC—the 1st such effort in Taiwan—in 7 months
- Grow business through ability to develop large-scale chip designs

### Design Challenges

- Shorten verification and analyses processes
- Process large database for huge SoC design
- Manage and integrate different technologies across industries

### Cadence Solution

- First Encounter® Design Exploration and Prototyping
- Encounter® Digital Implementation System
- Encounter Conformal® Equivalence Checker
- Incisive® verification platform
- Sigrity™ packaging and PCB signal and power analysis solutions
- Verification IP Catalog

### Results

- Completed complex design from data-in to tapeout within 7 months
- Reduced one iteration for timing optimization, extraction, analysis and verification of physical design down to 4 days
- Expanded design capacity by 10X

## The Challenge

With the rise of cloud computing and the Internet of Things, there is more interlinking of people, devices, and data. Thus, the future is likely to see continued strong demand of network processors by professional industries. In 2011, Faraday undertook a 4G base station processor design project for a tier-one company. This is a large-size chip of more than 300 million logic gates. In terms of chip size, it is the first such effort for a Taiwanese company.

This project encompassed front-end chip design to back-end implementation and manufacturing. This project truly tested Faraday's design and management capabilities for large-scale projects. Compared to the typical 12-million-gate USB3.0 chips, or the 25-million-gate projector chips on the consumer market, in this big-scale effort, the challenges were significant.

This chip utilizes more than 100 internally designed and third-party IP, 5 6G SERDES IP, over 1,000 FCBGA package pins, and more than 20 process corners. At the same time, to be able to achieve a successful tapeout within seven months, every step had to be executed with the highest efficiency. For example, to run timing closure, the process from timing optimization to RC extraction, signal integrity (SI) analysis, and static timing analysis (STA) check had to be shortened to complete within four days. As another example of the challenges faced, in back-end verification, physical verification of the GDS files, as large as 70GB, had to be completed within two days.

Kun-Cheng Wu, associate vice president of SoC Development and Service at Faraday, explained, "We have encountered three major design challenges, including managing a large database for a huge SoC design, striving for the highest efficiency to complete implementation and verification, and performing heterogeneous integration in different fields."

> *"We leveraged UVM technology for both IP-level and system-level verification. Together with Cadence's VIP solution for interface, peripheral, and memory models, we achieved our goal of verification closure with good confidence on various SoC/IP products."*
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> *Ken Liao, Associate Vice President, Digital System and Platform, Faraday Technology Corporation*

Due to these design requirements, Wu said, "Faraday first implemented a hierarchical design system. This system allowed Faraday to integrate more efficient design procedures and the largest integrated design methods during the development stage. These efforts enabled us to overcome our challenges. And above all, using EDA tools effectively definitely played a very important role."

## The Solution

Throughout this entire process, which included front-end SoC design to back-end chip development, Faraday utilized many solutions from Cadence, including: the Verification IP (VIP) Catalog, First Encounter Design Exploration and Prototyping, Encounter Digital Implementation System, Encounter Conformal Equivalence Checker, Incisive verification platform and Sigrity packaging and PCB signal and power analysis solutions.

Ken Liao, associate vice president of Digital System and Platform at Faraday, was responsible for the front-end chip design, and said, "We worked closely with our customers during the front-end SoC design work. We repeatedly discussed specifications such as SoC infrastructure, chip memory, and performance. With such a large-scale and complex project, we needed to ensure that our customers could trust us to develop the best SoC, which plays a very critical role in silicon-embedded devices."

He added, "We leveraged UVM technology for both IP-level and system-level verification. Together with Cadence's VIP solution for interface, peripheral, and memory models, we achieved our goal of verification closure with good confidence on various SoC/IP products."

When embarking on the back-end design part, the first problem Faraday resolved was prototyping and feasibility analysis. As Wu pointed out, "Using the hierarchical approach and partitioning guidelines reduced the number of days needed to run the 300-million-gate design prototyping process from two weeks to only three to five days."

Faraday used Encounter Digital Implementation for its floorplan analysis process. Wu commented, "As for the back-end design process, we were running against time. Every run needed to be completed in the shortest time possible and we had to be able to correct mistakes. During the entire design process, the Cadence team gave us plenty of support and recommendations. Their immediate support was extremely important to Faraday."

He also pointed out, "For example, the top instance count of this design is 8 million. If we used optDesign to execute it, we would need 160 hours. But using optVirtual, we reduced the time to only 16 hours. And, after further reducing the instance count to 3.5 million with enhanced partitioning, we cut the time to only four hours. It was a 40X improvement in speed increment."

"It was the same for the pre-CTS-opt stage. In 2011, Cadence's latest GigaOpt technology was not yet available. But Cadence provided us with its beta version of AAE (Advanced Analysis Engine), which eventually became GigaOpt, for a test run. For the 3.5 million top instance count design, the execution time was shortened from 72 hours by using optDesign to 24 hours. This is also an amazing improvement."

"At that time, we frequently held meetings with Cadence's R&D team to discuss design, implementation, results, and functionalities. We hoped to be able to resolve our problems quickly. Cadence was always very supportive, and we consider it a perfect example of high-level R&D alignment for both companies."

## Results

To fulfill the three major concerns of "partition, integration, and efficiency", Faraday successfully achieved the completion of its 300-million-gate SoC project within seven months and entered into mass production. As Faraday also provides back-end manufacturing services on this chip, the company paid much attention to building a co-design environment from IC to packaging and PCB design. The co-design infrastructure aims to resolve the SI/power integrity (PI) issues. All these efforts have greatly increased front-end design efficiency and improved yield rate of manufacturing effectively.

Other than front-end functional verification and back-end placement-and-routing design, Faraday was able to reduce design time for its hierarchical formal check, IR drop analysis, packaging, and PCB power analysis processes with the help of the Cadence team and its professional chip design process. For Faraday, it is a resounding success, and realizes a 10X leap in design capacity.

## Summary and Future Plans

Wu expressed that, besides the superior design ability and experience vs. other competitors, excellent integration and management were the two main factors for the success of this project. This effort also fully demonstrates that Taiwanese businesses are able to take on more complex and larger-scale design projects. At the same time, with the expanding communications industry, large-size chip design needs are anticipated to increase. There is also the trend of the billion-gate SoC. Eyeing the great potential, Faraday will continuously deploy design capabilities based on its successful experiences on the 300-million-gate SoC design and be ready to undertake larger projects.

Faraday also knows that relying on design service providers alone is no longer enough to fulfill customers' needs. Thus, during this project, the support and assistance provided by the Cadence team was critical. In the future, Faraday will further enhance its relationships with EDA and IP partners, and together, be able to take on more difficult design projects.