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# Faraday and Cadence

"We've observed 3x fewer iterations of ECOs using Encounter Conformal ECO Designer. We've also seen a 50x reduction in the time it takes to implement project ECOs—from 3 days down to only 1 hour."

Huanyu Chen, Senior CAD Engineer, Faraday Technology Corporation

## The Customer

Faraday Technology Corporation is a leading fabless application-specific integrated circuit (ASIC) vendor and silicon intellectual property (SIP) provider. The cornerstone of Faraday's success is its capability to provide highly customized solutions for its customers. The company's proven and recognized ASIC, system-on-chip (SoC), and intellectual property (IP) design capabilities and services enable customers to realize their ideas in silicon—better and faster—and to gain a competitive edge through lower cost and higher product differentiation.

Since Faraday's launch in 1993, the company has provided professional ASIC design services, equipped with a well-developed ASIC infrastructure and team members with an average of more than 10 years of experience. Faradays in-house IP includes thousands of ARM-compliant central processing units (CPUs); high-speed input/outputs (I/Os); memory interfaces; and fundamental IPs such as libraries, memories, phase lock loops (PLLs), and regulators.

To meet the increasing demand for SoC ASIC design, Faraday has built a dedicated platform service team and SoC development flow and toolset to support the advanced development process and accelerate time to tapeout. So far, the company has launched many successful SoCs, including highly complex projects with gate counts in the 300 millions.

## The Challenge

Faraday's process must shield its customers from the pitfalls of running a successful ASIC design and enable them to consistently achieve time-to-design and time-to-market efficiency for mass production.

To this end, the company recognized the need to update its engineering change order (ECO) process in 2010. An ECO involves inserting a logic change directly into the netlist after an automatic

### Business Challenge

- Consistently provide highly differentiated ASIC, SoC, and IP designs to customers while achieving lower cost and faster time to market

### Design Challenges

- Automate the functional ECO process (including bug fixes and new feature introductions/deletions)

- Minimize the risk of quality issues and schedule slips

### Cadence Solution

- Encounter Conformal ECO Designer

### Results

- Achieved faster functional ECO implementation turnaround time by minimizing manual work and time-consuming iterations

- Gained the ability to implement complex ECOs, a task nearly impossible using the traditional manual process

- Achieved earlier netlist handoff to customers

- Reduced manufacturing costs and accelerated time to market for customers

tool has already processed it. An ECO may include anything from adding or removing logic in a design to a more subtle change such as cleaning up routing for signal integrity.

"ECOs help us deliver products to market as fast as possible with minimal risk to quality and schedule," says Huanyu Chen, senior CAD engineer, Faraday. "Advantages include an unchanged floorplan, preserved clock tree, saved mask, and shortened time to market. "

While extremely beneficial, ECOs can also be stressful and time-consuming. Traditional manual ECO flows are labor-intensive and limited in their ability to ensure that a product will function properly. Since designers usually don't know if a change made in the logical netlist can be executed in the physical netlist, completing a manual ECO process takes a great deal of time and effort. While performing manual changes on many levels, it's also difficult to accurately keep track of used spare cells and freed cells.

"A manual ECO flow starts by comparing the old netlist to the modified RTL using an equivalency checker," Chen explains. "A designer can then check out the differences and locate necessary changes in the netlist. After the time-consuming process of manual editing and rechecking, the netlist is ready for physical implementation."

Before correcting the physical implementation, the designer must use a place-and-route tool to determine the differences between the modified logical netlist and the physical def file. Then the designer must compare the new netlist to the modified register-transfer level (RTL) ECO.

*" The Cadence solution has significantly reduced our project costs and risk, and enabled faster time to market. The financial benefit of ECO automation using Conformal ECO Designer has been enormous for our company."*

### The Solution

As Faraday's functional ECOs become more complex in the areas of clock gating, ungrouping, sequential merge, boundary optimization, design-for-test (DFT) logic, and low-power logic, traditional manual ECO methods are no longer up to the task. The traditional methods are increasingly difficult and time-consuming to implement, introducing high risk to project schedules. For this reason, a proven, streamlined, and automated ECO is required.

"The mask costs millions of dollars, and an ECO is usually a key factor in the success of an entire project," Chen says.

To facilitate projects with higher confidence and efficiency, Faraday designers must be able to implement an ECO with gates on the mask and process them with a limited number of metal layers. By using

only metal layers and eliminating the need for base-layer changes while implementing ECOs, the customer is able to reduce costs and stay on schedule.

Faraday has a long history of adopting Cadence tools. So to address its ECO challenges, Faraday decided to implement Encounter® Conformal® ECO Designer. "Conformal ECO Designer allows our ASIC team to tackle difficult ECOs that would otherwise take a significant amount of time and may even be impossible to perform using traditional manual methods," Chen says.

Conformal ECO Designer offers functional ECO analysis and optimization, and generation capability. It combines proven equivalence and functional checks, and uses formal techniques to analyze, abstract, and implement ECOs.

"The Cadence solution implements RTL ECOs for pre- and post-mask layout, and offers early ECO prototyping capabilities for driving our critical yes/no project decisions," Chen says.

Conformal ECO Designer compares each logic cone in the design, determines which cones are different, and identifies what changes are required to complete the ECO. This minimizes the number of changes and reduces the impact on back-end processing, which accelerates turnaround time.

In the post-mask flow, ECO changes are mapped to available gates or freed gates. Conformal ECO Designer informs the user about any resource shortages.

"Using the Cadence solution, we can limit the changes to a cone of logic, which confines the number of changes to the physical design," Chen explains. "While we reduce the changes required by the place-and-route tools, we greatly minimize the overall complexity and risk of the ECO."

### Results

Since adopting Conformal ECO Designer in 2010, Faraday has successfully used the tool on more than 30 ASIC tapeout designs. The team has experienced amazing runtime when Conformal ECO Designer accepts the ECO setting.

"We've observed 3x fewer iterations of ECOs using Conformal ECO Designer," Chen says. "We've also seen a 50x reduction in the time it takes to implement project ECOs—from 3 days down to only 1 hour."

### Summary and Future Plans

Using Conformal ECO Designer, Faraday has developed a fast and efficient ECO flow to handle functional logic changes compared to its previous traditional manual process.

"The Cadence solution offers improved predictability, faster process time, high-quality results, and lower costs," Chen concludes. "Ultimately, our designers are able to process more ECOs and we're able to get finished products to our customers more quickly than ever before."

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