DATASHEET

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Conformal Low Power

Fast and accurate power intent verification and design checks

Cadence® Conformal® Low Power enables engineers to verify and debug multimillion-gate designs optimized for low power without complex and time-consuming gate-level simulations. It also enables power-aware equivalence checks. Conformal Low Power provides superior performance, full-chip capacity, and ease of use by combining low-power verification checks with world-class equivalence checking.

Conformal Technology

Designers need production-proven validation tools to shorten overall design cycle times and minimize silicon re-spins. Conformal verification technologies offer the most comprehensive and trusted solutions for equivalent checks, timing constraints management, clock-domain crossing synchronization checks, analysis and generation of functional engineering change orders (ECOs), and low-power design comparison and verification.

Conformal Low Power

Optimizing for leakage and dynamic power helps designers reduce energy consumption and lower packaging costs. While advanced low-power methods such as static and dynamic voltage and frequency scaling, power gating, and state retention offer additional power savings, they also complicate the verification task. Conformal Low Power enables low-power verification through the implementation process from RTL to the final signoff of the physical netlist.

Verification becomes more complex when most of the low-power functions are added to the gate netlist during synthesis and physical implementation. Most simulation-based verification occurs in the RTL phase, as the largest and most complicated designs cannot be verified by full-chip or gate-level simulations.

Conformal Low Power addresses these challenges directly. It combines proven equivalence checking, structural, and formal techniques to enable full-chip, low-power optimization, and verification. Conformal Low Power is available in XL and GXL offerings.

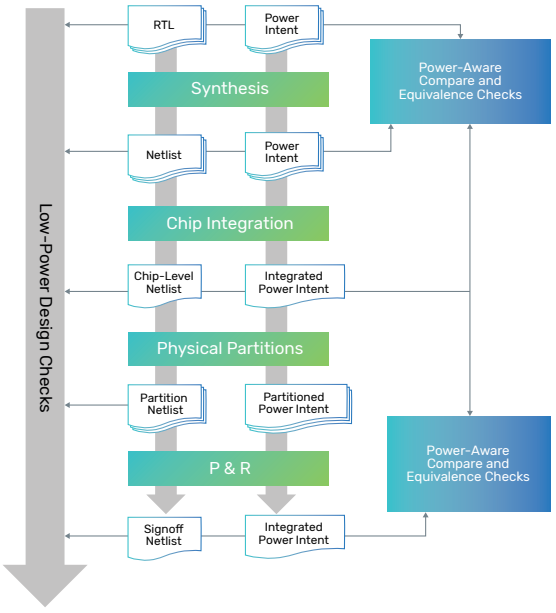

Figure 1: Low-Power verification flow with Conformal Low-Power

Benefits

- Minimize silicon re-spin risk
- Check power intent in syntax, semantics, and design specification before implementation
- Detect low-power implementation errors early in the design cycle
- Streamline identification of low-power design issues through a single unified cockpit for debugging power intent, RTL, logical netlist, and physical netlist power issues
- Verify multimillion-gate designs faster (by orders of magnitude over simulation-based approaches)
- Close the RTL-to-layout verification gap
- Reduce the risk of missing chip-killing bugs through complete formal checks that leverage independent verification technology

Features

Conformal Low-Power XL

The XL configuration combines logic equivalence checking for the most complex low-power SoCs and datapath-intensive designs with power intent and design checks for low-power verification.

Power intent verification and debug

Power intent quality checks will catch all syntactical and semantic issues in the design process. Cross-probing between error/warning messages, the design source (RTL/gate netlist), and the power intent file accelerates the debugging of these issues and the refinement of power intent.

Conformal Low Power provides independent verification of low-power designs in flows with a mixture of simulation, synthesis, and physical implementation tools. Additionally, it supports a consistent environment for power intent verification based on an interoperable subset of the power intent formats.

Equivalence checking

A low-power design will undergo numerous iterations during development, and each step might introduce logical bugs. Conformal Low Power helps you to identify and correct those logical bugs immediately by checking the functional equivalence of different versions of a low-power design at various stages. For example, it validates the post-synthesis netlist and instantiated power intent back against the verified-golden RTL and its associated power intent. Conformal Low Power also supports advanced dynamic and static power synthesis optimizations such as clock gating and signal gating, multi-Vt libraries, and de-cloning and re-cloning of gated clocks during clock tree synthesis and optimization.

Conformal Low Power supports both the Common Power Format (CPF) and Unified Power Format (UPF)/IEEE1801 specification languages. It uses the power intent for guidance to independently model how implementation inserts and connects low-power cells, level shifters, isolation, repeaters, state retention registers, and switch chain implementation into the design, enabling true low-power checking from the RTL level through the gate level. Conformal Low Power also provides power-aware equivalence checks that perform independent isolation function insertion to validate the revised design with the insertion done by implementation tools, power intent compare, power state table compare, and power grid consistency checks.

Structural and functional checking

Conformal Low Power supports multi-supply voltage (MSV) islands, coarse-grain power gating (PSO), coarse-grain ground switching (GSO), dynamic voltage and frequency scaling (DVFS), and state retention power-gating design techniques. It can also perform power domain structural and functional checks on an RTL design with power intent, a logical gate netlist (typically, post-synthesis), and a power-aware physical gate netlist (after place-and-route).

For RTL and logical gate netlist checking, you define the power intent: power domains, voltages, standby conditions, power modes, and power associations along with the low-power cells being used. Conformal Low Power then propagates the domains throughout the design hierarchy and identifies all domain boundary crossings. Finally, it reports the following information:

- Power and ground assignment-related problems and floating connections
- Level shifters: missing, redundant, or wrong connectivity
- Isolation cells: missing, redundant, wrong gate type or wrong isolation enable signal
- Retention cells: missing, redundant, wrong type, or wrong retention control signal
- Control signals that are not powered appropriately

Conformal Low Power supports special low-power cells, such as non-dedicated isolation cells, asynchronous set/reset latch-type isolation cells, multiple-stage shifter cells as well as combination isolation and level-shifter cells.

For physical netlist checking, Conformal Low Power accepts a Verilog power-aware netlist and Liberty models.

It uses top-level power pins, power and ground nets, power switches (MTCMOS), ground switches, voltage islands, power pin associations, and low-power cells to automatically derive the supply set assignments and crossings in the design. Conformal Low Power identifies the following issues:

- Incorrect power and ground connectivity, including shorts and opens
- Instance domain and supply set conflicts
- Missing, redundant, and incorrect power connection and wrong level-shifter types
- Missing, redundant, and incorrect isolation cell power connectivity
- Power control signals to power switches, isolation cells, and state retention registers that are not powered
- Incorrect power connection to low-power cells

Integrated environment

You can easily diagnose and review the tool setup and design profile with the intuitive and interactive IEEE1801 GUI, which provides the following features:

- The landing page provides the design profile information and low-power option configurations
- Supply network visualization supports the abstract supply network extracted from the power intent and the real physical netlist connections
- Hyperlink object reporting
- Power intent browser displays the hierarchical UPF instance scope in the UPF hierarchical scope tree
- Virtual cell schematic allows users to view the virtual low-power cells inserted from the power intent implementation strategies.

Conformal Low Power GXL

In addition to the features of Conformal Low Power XL, Conformal Low Power GXL adds support for transistor circuit analysis, abstraction and provides equivalence checking for custom designs, standard cell libraries, I/O pads, and embedded memories. Moreover, Conformal Low Power GXL also offers unique checks for circuit integrity. For example, to analyze SPICE circuits at the domain crossing, forward-bias junctions, open-source pin paths, and to examine the channel-connected path at the circuit view.

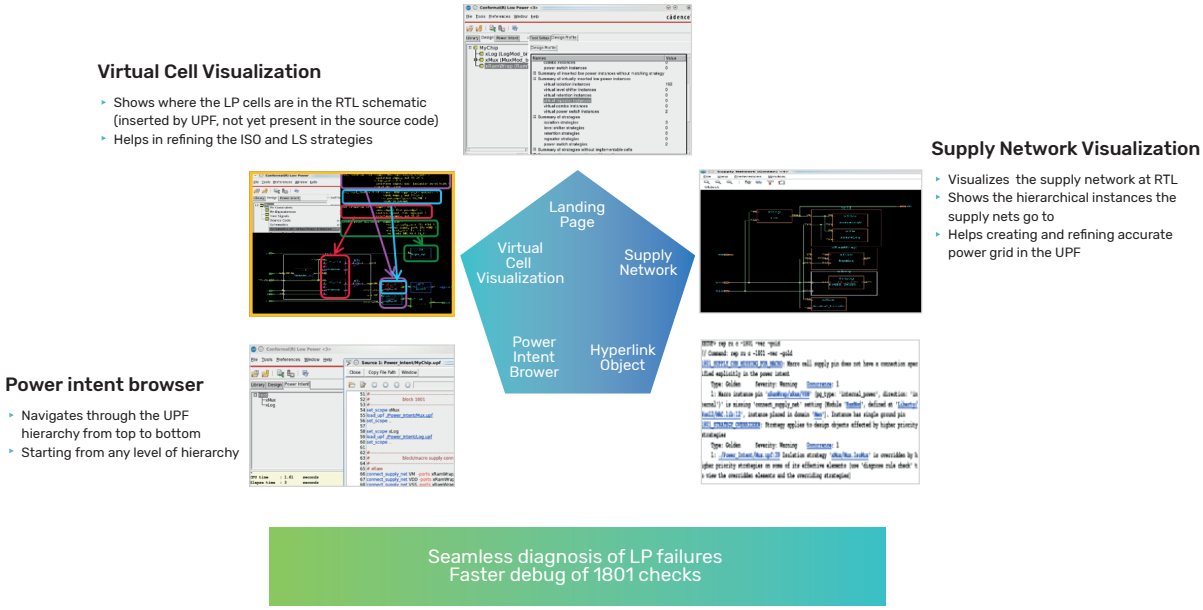

Figure 2: Conformal Low Power IEEE1801 GUI speeds diagnosis, visualization and reporting

Platforms

- Linux (64-bit)

Languages

- CPF
- UPF1.0, IEEE1801-2009 (UPF2.0), IEEE-1801-2013 (UPF2.1), IEEE1801-2015 (UPF3.0)
- Mixed language:
  - Verilog (1995, 2001)
  - SystemVerilog
  - VHDL (87, 93)
  - SPICE (traditional, LVS)
- Liberty

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