cadence®

Encounter Conformal Constraint Designer

Automated validation and refinement of timing constraints

Cadence® Encounter® Conformal® Constraint Designer automates the validation and refinement of SDC timing constraints and clocks. By ensuring that timing constraints are valid throughout the entire design process, and by pinpointing real design issues early, quickly, and accurately, Conformal Constraint Designer helps designers achieve rapid timing convergence with fewer iterations, leading to more predictable schedules.

Encounter Conformal Technology

To shorten overall design cycle times and minimize silicon re-spins, designers need production-proven validation tools. Encounter Conformal verification technologies offer the most comprehensive and trusted solutions for equivalency checks, timing constraints management, clock-domain-crossing synchronization checks, analysis and generation of functional engineering change orders (ECOs), and low-power design optimization and verification.

Encounter Conformal Constraint Designer

Validating, modifying, and creating the SDC timing constraints required for design implementation and static timing analysis (STA) signoff have conventionally involved manual and inefficient processes. IP reuse and hierarchical design abstraction often result in complex timing constraints and asynchronous clock domain crossings.

Encounter Conformal Constraint Designer enables efficient development and management of timing constraint intent, ensuring they are functionally correct—from RTL to layout. By delivering higher quality timing constraints early and throughout the flow, Conformal Constraint Designer helps designers reduce overall design cycle times and achieve the highest quality of silicon for even the most challenging SoC designs. By analyzing clocks and clock domain crossing, it catches errors that could cause a functional failure of the SoC design. Conformal Constraint Designer is available in L and XL configurations, plus an XL Multi-Mode Compare Option.

Benefits

- Shortens design cycles by checking the creation and integration of block-level and top-level constraints
- Improves quality and provides early predictability of silicon in terms of area, timing, and power by using higher quality constraints
- Reduces risk of re-spins through formal validation of exception constraints
- Speeds convergence on timing closure by quickly validating failing timing paths as functionally false
- Validates SDC constraints against the original intent, as the design constraints transform during implementation
- Helps users create initial timing constraints effortlessly, directly from RTL, with the SDC Template Generator capability
- Offers the most trusted and independent equivalence checking solution

Features

Conformal Constraint Designer automates SDC validation by first checking SDC for structural, syntactical, and implementation issues and then by functionally verifying the exception constraints. It validates the constraints that have been propagated at different hierarchical levels

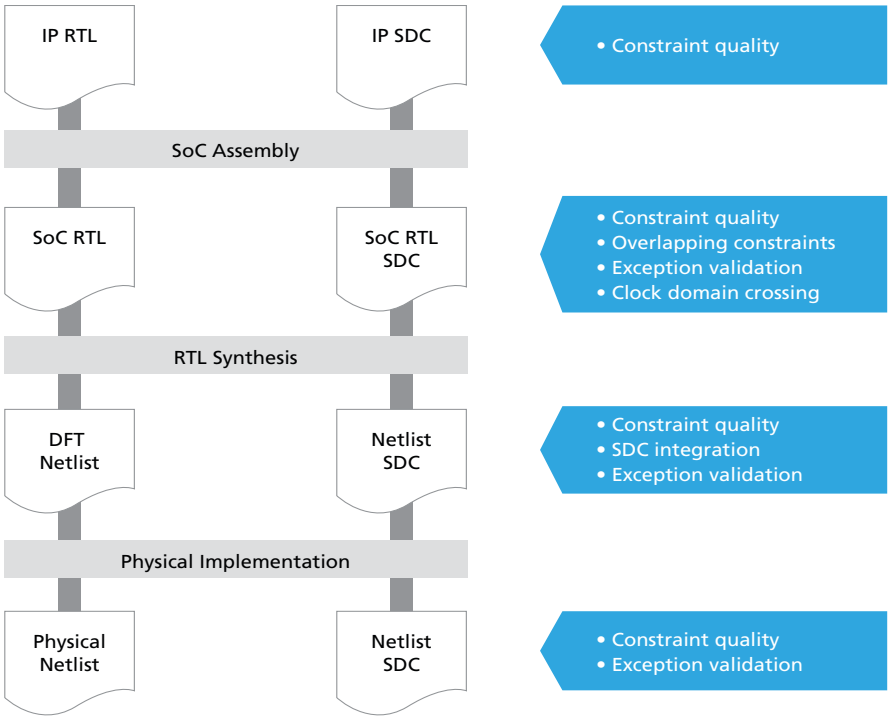

Figure 1: Encounter Conformal Constraint Designer offers a complete solution for designing and refining constraints—from RTL to layout

using hierarchical constraint checking, while also checking for the overlaps among constraints. In addition, Conformal Constraint Designer derives clocks from SDC and validates clock domain crossings to highlight problems with synchronizers. It provides an extensive debugging and analysis environment to pinpoint the errors in SDC and arrive at correct constraints quickly.

SDC quality checks

Conformal Constraint Designer ensures functionally correct SDC specifications in a design context by checking different aspects of specification and design:

- Checks with design elements; for example, reference points are not connected in a multi-chip package
- Enforces SDC syntax and additional requirements
- Flags syntactically legal but problematic constructs, such as incorrect mode set-up
- Categorizes SDC errors related to clocks, I/Os, exceptions, or others; annotates SDC errors to the SDC source and provides rich analysis via an intuitive GUI
- SDC Exception Manager window displays constraints annotated with error summaries and analysis
- Performs cross-probing between constraint errors, RTL, netlist, waveforms, and schematics

Hierarchical constraint checks

Block designers typically write SDC independently from top-level constraints. When chip integrators or physical designers assemble the chip, they may find that the constraints have conflicts in terms of clock definition, set I/O delay settings, and exceptions. Conformal Constraint Designer can quickly and easily detect these errors early in the design cycle with hierarchical constraint checks. It checks the SDC of the design at different hierarchical levels—chip-level SDC vs. block-level SDC—and pinpoints conflicts, overlap, or other issues related to clocks, I /O delays, and exceptions. Additionally, it annotates the errors onto the SDC file, design source, or schematics.

Overlap checks

Overwritten, overlapping, or conflicting exceptions within the same SDC can cause delays in timing closure. Implementation and STA tools may have inconsistent precedence rules or select pessimistic constraints, which result in poor quality of silicon. Designers must have an opportunity to review the conflicts and decide on the proper course of action. Conformal Constraint Designer reports duplicated or overwritten constraints and overlapping exceptions, so designers can accomplish this task efficiently and formally.

Exception validation

Using industry-proven formal verification technology, Conformal Constraint Designer functionally validates false-path and multi-cycle-path exceptions specified in SDC. A true path incorrectly set as false, or a multi-cycle path exception with an incorrect number of cycles, could easily result in a re-spin if they fail timing. Inadvertent wild-carding of exceptions

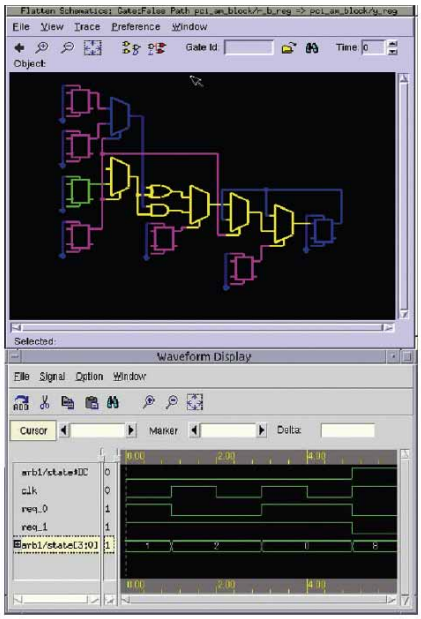

Figure 2: For an invalid false-path exception, Encounter Conformal Constraint Designer can show the path of concern and the waveform that triggers it

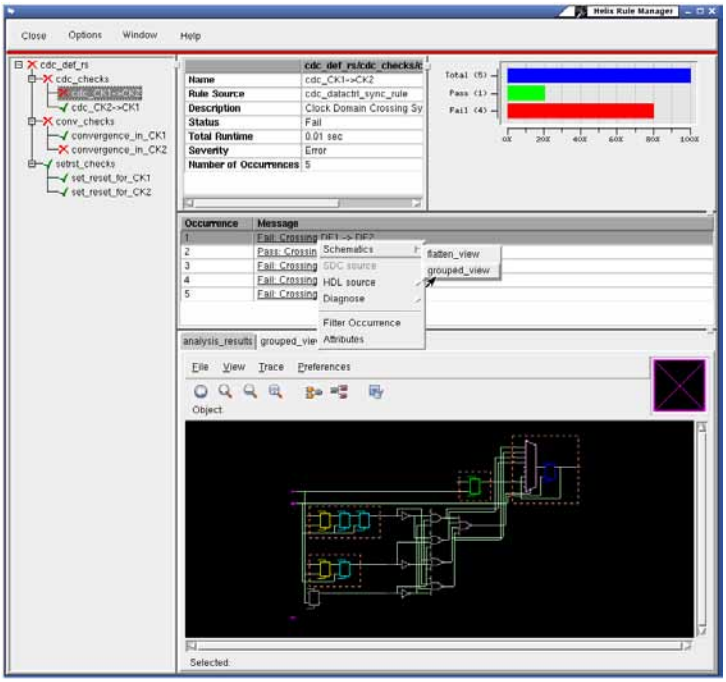

Figure 3: Clock domain crossing checks as viewed in a helix extensible platform

only increases this risk. The Exception Manager in Conformal Constraint Designer expands all defined paths and validates each of them formally.

The false paths can also be found in asynchronous behavior of designs, and analysis and validation of these paths are performed accordingly. Statements that simply cover too many paths can also be flagged. A counter-example is generated when validation fails, quickly pinpointing the active path and the waveform that enables it.

Timing report validation

Designers can spend enormous amounts of time debugging timing reports to separate functional false paths from true ones. Conformal Constraint Designer automates and accelerates this validation process by identifying false paths from critical timing reports and generating new SDC exceptions. These results can be used to improve synthesis, place-and-route, or STA results. By focusing only on paths that violate timing, the generation is quick, relevant, and accurate (as it is done through formal validation).

SDC Advisor and template generator

The SDC Advisor enables directed constraint creation through a GUI environment. Included in the output are clock definitions, set_case_analysis settings, and input/output constraints. The SDC Advisor reveals the structures of any undefined clocks, allowing the user to constrain them quickly and completely. All that is needed is to fill in the blanks, such as clock frequencies. Alternatively, an SDC template can be easily created from scratch for any given design through the use of the SDC Template Generator. More extensive output capabilities are available through a text-based utility, ideal for the user starting with more knowledge of the specifics of the design.

SDC integration

Given a set of block-level constraints, Conformal Constraint Designer can generate the top-level constraints through the use of default or user-defined precedence rules, easing the process of assembling the design for place-and-route.

SDC Compare

During the design process, optimization tools may transform reference objects in the design. Also, as a design progresses, users may add to or change SDC files. The impact of adding or deleting timing constraints can be observed; for example, the impact of adding a timing exception upon the rest of the design. SDC Compare can check before-and-after, or can be used to manage revisions of SDC files. It helps verify final output versus the original intent of timing constraints.

Multi-mode constraints

All designs are multi-mode, with a test mode and basic functional mode, and usually more. SDC quality checks are done on a mode-by-mode basis. Then, using multi-mode checks, Conformal Constraint Designer identifies inconsistent, conflicting, or missing constraints across the modes. This prepares a design for faster, smoother multi-mode implementation and optimization.

Clock domain crossings

Clocks are defined within SDC constraint files. After Conformal Constraint Designer performs fundamental quality and consistency checks on timing constraints, it can check structural and functional issues with clock domain crossings (CDC). Conformal Constraint Designer also offers FIFO checks. A FIFO manager graphical interface pinpoints issues with CDC synchronizers.

Helix extensible platform

Conformal Constraint Designer has been updated with an extensible design platform that speeds debug across

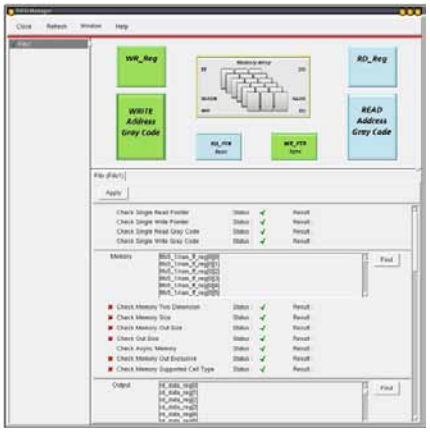

Figure 4: FIFO manager GUI pin-points issues with CDC synchronizer logic

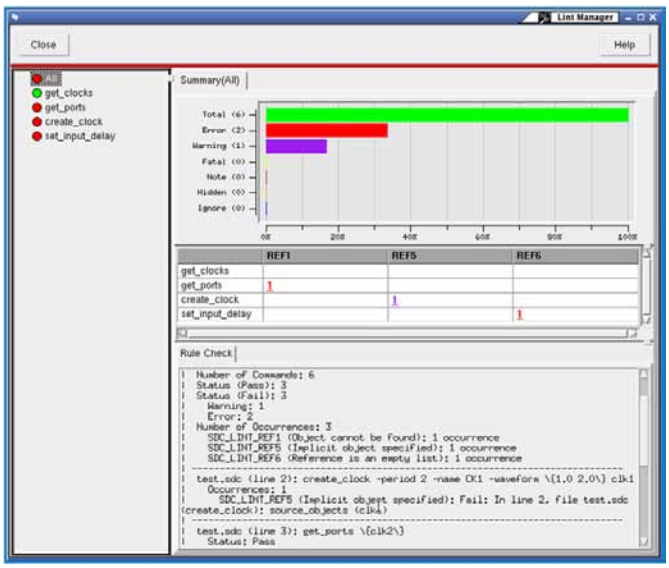

Figure 5: Encounter Conformal Constraint Designer detects and categorizes incorrect and problematic constraints

multiple dimensions. It is ready-to-go yet customizable, allowing users to write or configure rules, assign warning thresholds, and utilize visualization widgets like charts, histograms, tables, schematics, and design source to illuminate the root cause of problems.

Intuitive GUI

Conformal Constraint Designer provides an intuitive and interactive GUI for set-up and debugging, allowing the user to quickly operate the product and investigate issues with the constraints. The GUI includes:

- Rule manager with documentation inset, quickly showing the root cause of warnings and why they are important
- Constraint and source-code viewers
- Automatic counter-example creation with waveform and annotated schematics, demonstrating the sequence of events leading to a dangerous condition

This integrated GUI allows a seamless transition from SDC quality checks to more advanced ones such as exception validation.

Encounter platform integration

Conformal Constraint Designer can be run standalone or as part of Encounter Digital Implementation System, Encounter RTL Compiler, and Encounter Timing System. SDC quality and hierarchical checks can be invoked from the synthesis (quality only), place-and-route, and STA environments, displaying any constraint conflicts or inconsistencies. These issues are often revealed only during integration of the different blocks.

Furthermore, timing report validation (TRV) can be run by Conformal Constraint Designer from within all three Encounter implementation technologies. This helps to quickly filter out paths that can never be exercised (and therefore do not need to be constrained), thus helping accelerate timing closure.

PSL and SVA generation

Conformal Constraint Designer can generate PSL and SVA assertions to bridge formal validation and simulation, thereby increasing confidence and easing adoption. These assertions can be created for false-path and multi-cycle path statements in the user's current SDC as well as the exceptions produced by Conformal Constraint Designer.

Parallel processing

For large and complex designs or exceptions, Conformal Constraint Designer reduces overall verification time by automatically dividing the checks and running validation on as many machines for which users have licenses. LSF is supported.

Configurations

The L configuration offers capabilities focused on fundamental checks of SDC and clocks:

- Validation
  - SDC checks
  - Hierarchical checks
  - CDC structural checks
- SDC Template Generator
- Basic equivalence checking

The XL configuration offers all the capabilities of Conformal Constraint Designer L plus more advanced features, which require knowledge of the design under validation and knowledge of sequential validation techniques:

- Validation
  - FP validation
  - MCP validation
  - Timing report validation
- Generation
  - SDC Advisor
  - SDC integration
- PSL and SVA generation
- Parallel processing
- Advanced equivalence checking

The XL Multi-Mode Compare Option offers:

- SDC Compare
- Multi-mode SDC checks

Platforms

- Sun Solaris (64-bit)
- Linux (32-bit, 64-bit)
- IBM AIX (32-bit)

Languages

- Verilog® (1995, 2001)
- SystemVerilog
- VHDL (87, 93)
- Mixed languages
- SDC timing constraints up to and including v. 1.8

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- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
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