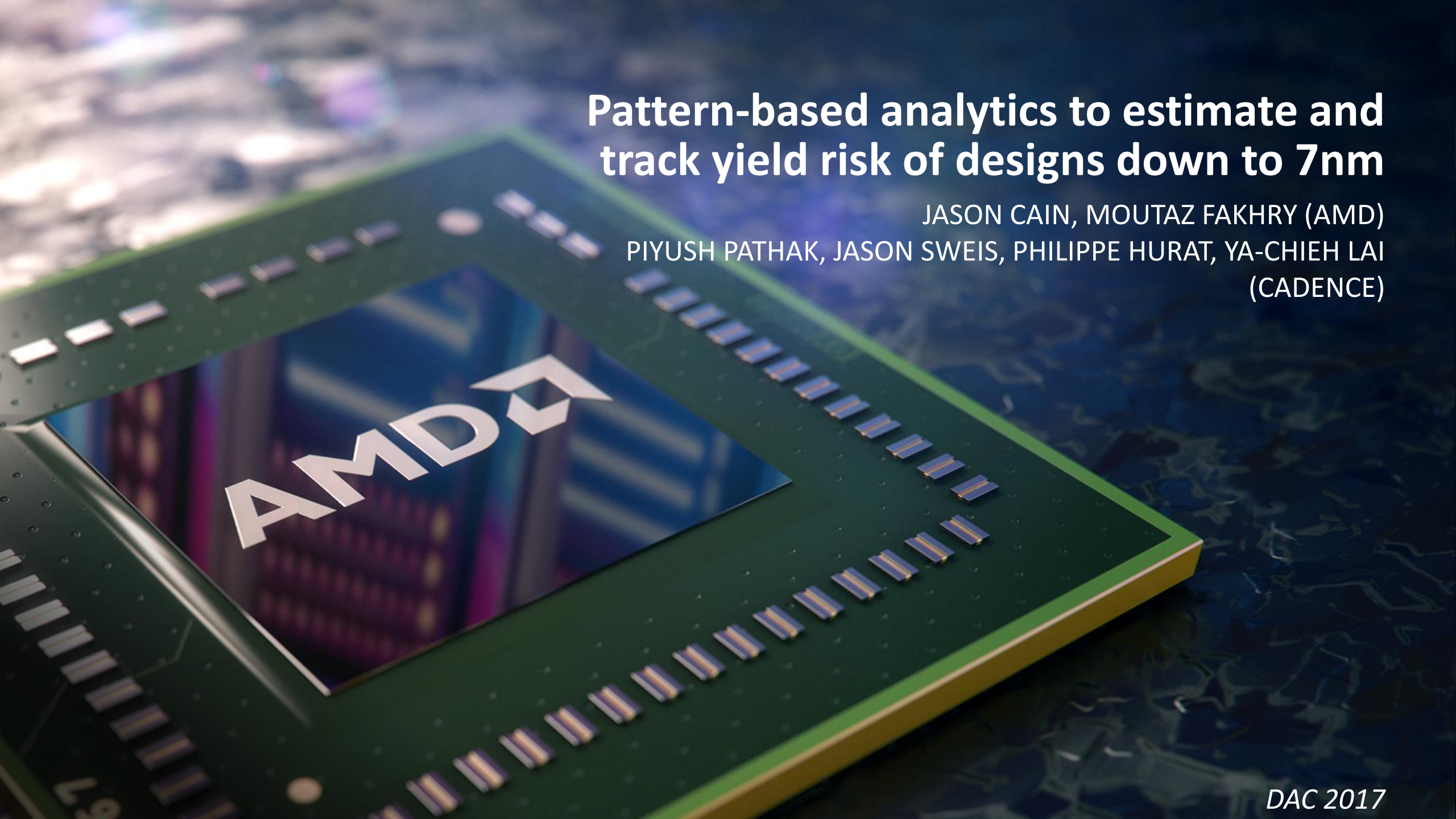

Pattern-based analytics to estimate and track yield risk of designs down to 7nm

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DAC 2017

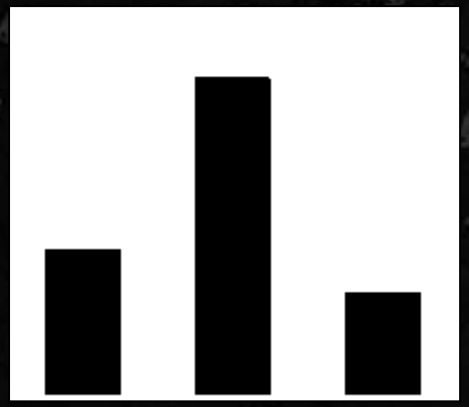
INTRODUCTION

AMD

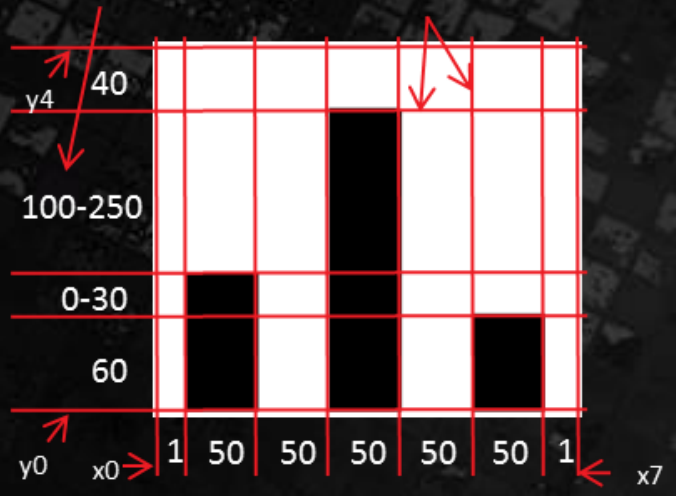
- Layout pattern matching engines have been available in the IC physical design ecosystem for over a decade.
- The use of pattern matching to augment design-rule checking (DRC) in the physical verification flow has been widely adopted since the 32/28nm generation.
- The more recent introduction of topological-based pattern matching engines has opened a range of new applications for layout analysis.
  - Pattern cataloging can be used to identify all unique pattern topologies (with or without specific dimensions) in a layout.
  - Catalogued pattern topologies can be compared between layouts to identify differences and commonalities and to identify potential risks.

TOPOLOGICAL PATTERN DESCRIPTION

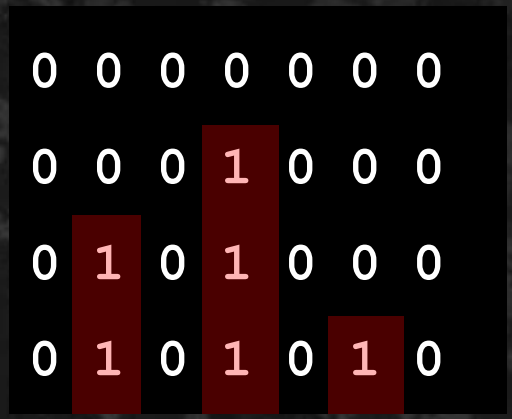
The “3-finger” Pattern



Deltas and Scanlines



Bit Pattern

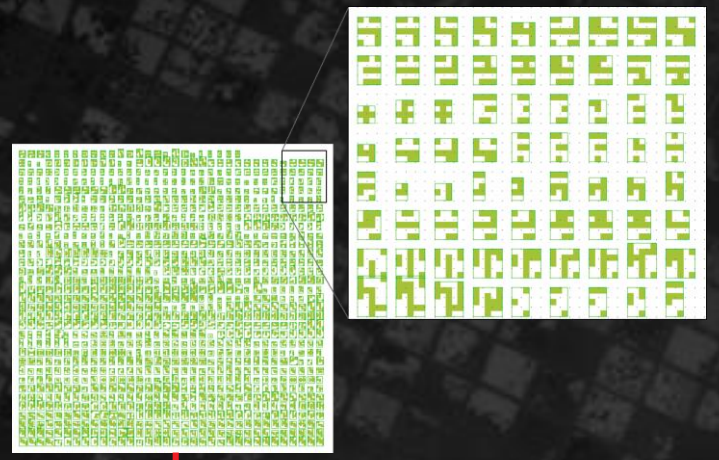


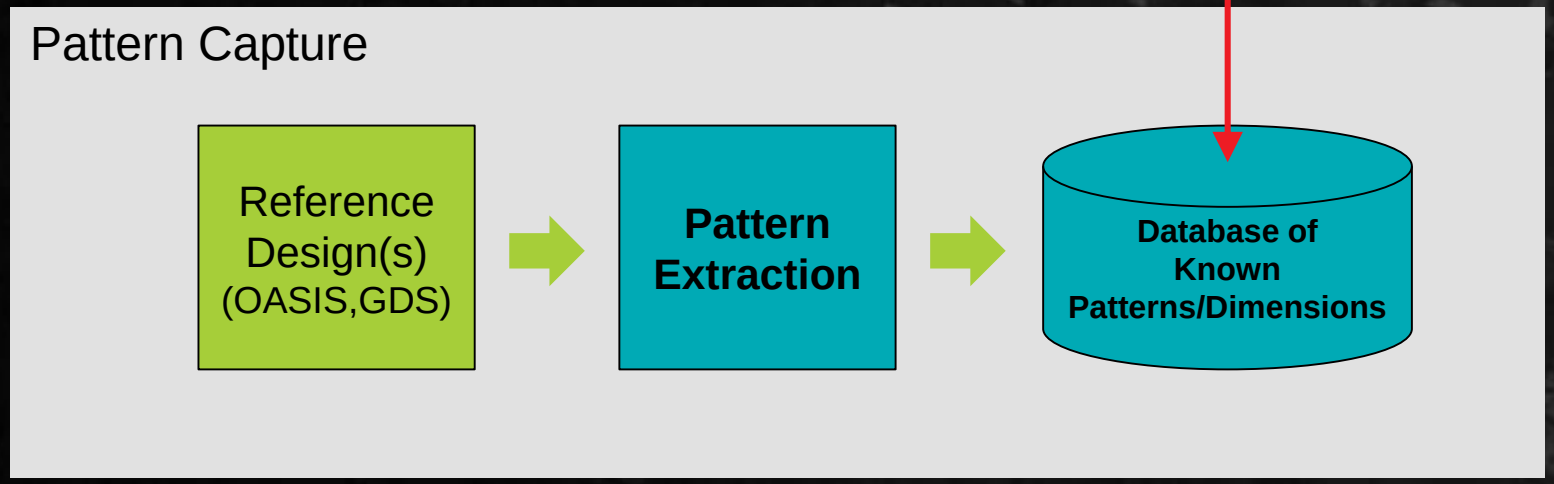
4×7 bitmap

- A powerful tool for characterizing and comparing physical designs
- Compact form for describing patterns
- Can be independent of physical dimensions

LAYOUT PATTERN CATALOGING

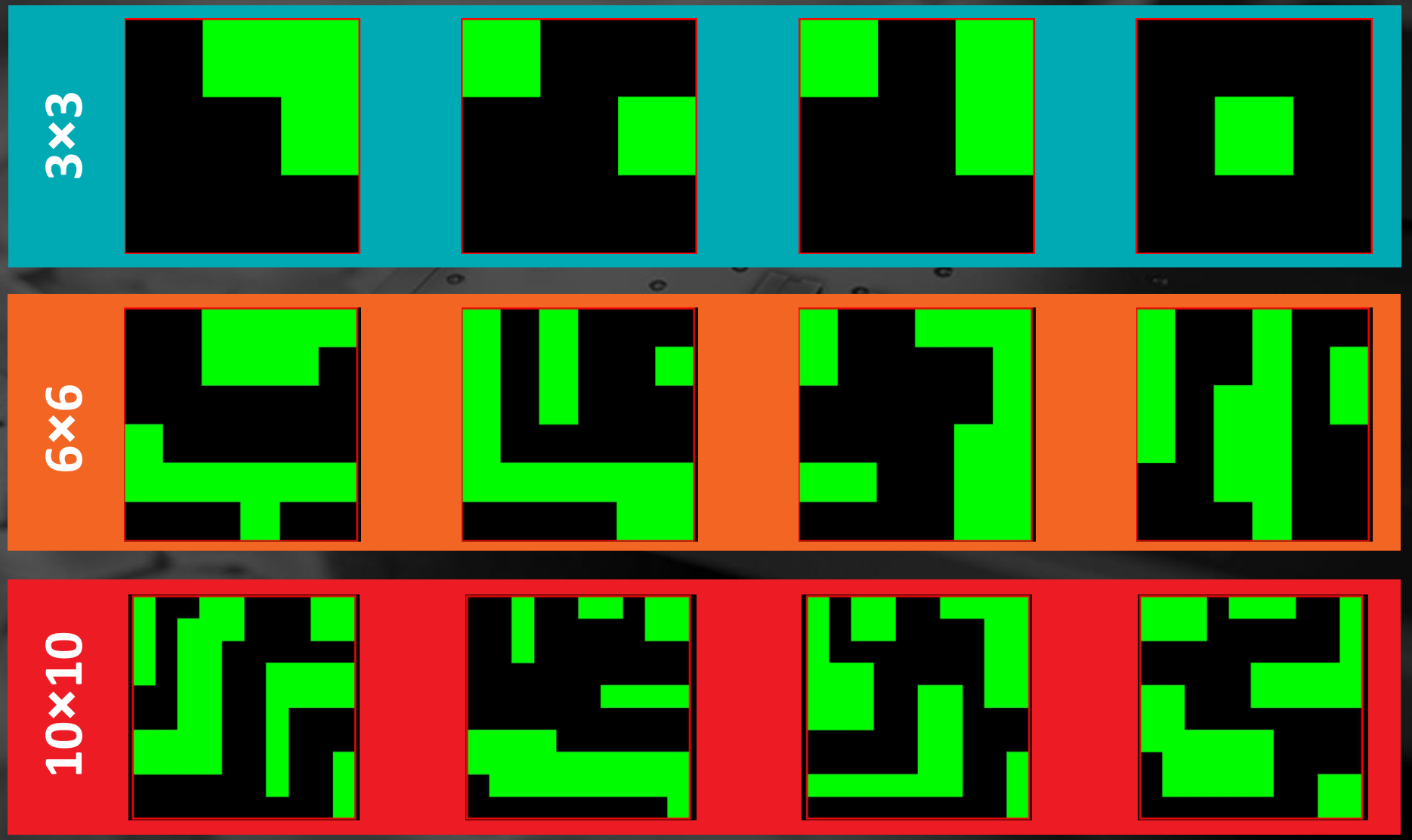
1. Systematically scan a window across entire design (choice of window size is important!)
2. In every window, break-down and identify every pattern and sub-pattern that exists in that design (with dimensions)
3. Store a full catalog of all patterns with dimensions





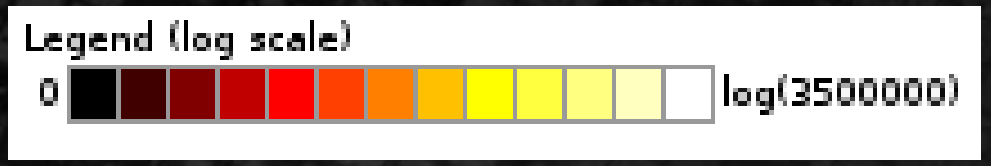
TOPOLOGICAL PATTERN EXAMPLES FOR MX LAYERS

14NM DIGITAL LOGIC – WINDOW SIZE = 3 METAL PITCHES

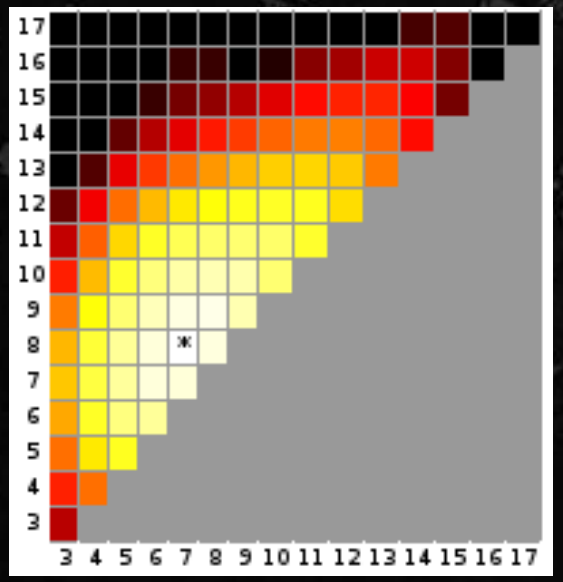


EVOLUTION OF DESIGN TOPOLOGICAL COMPLEXITY

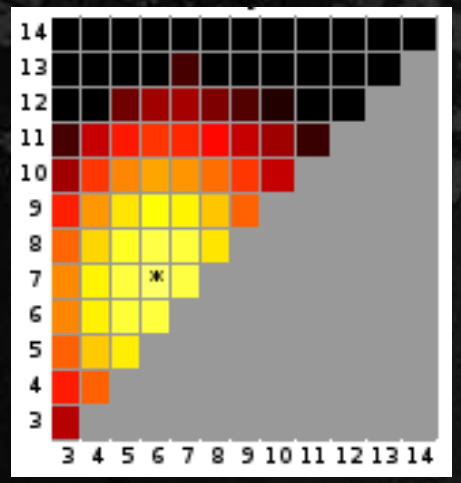
1X METAL LAYERS, WINDOW = 3 METAL PITCHES, INEXACT MATCHES



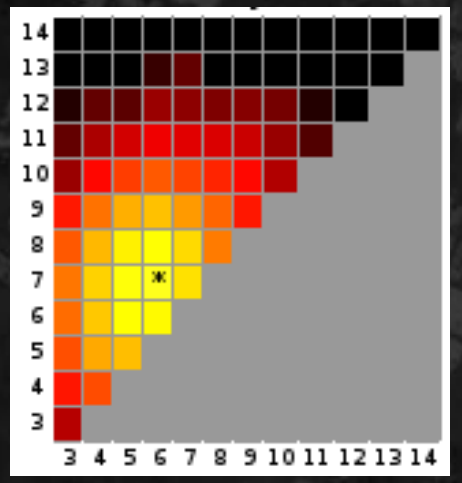
28 nm



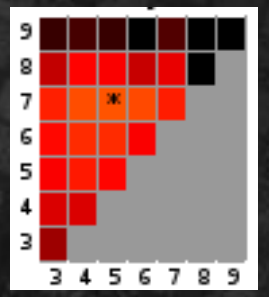
20 nm



14 nm



7 nm

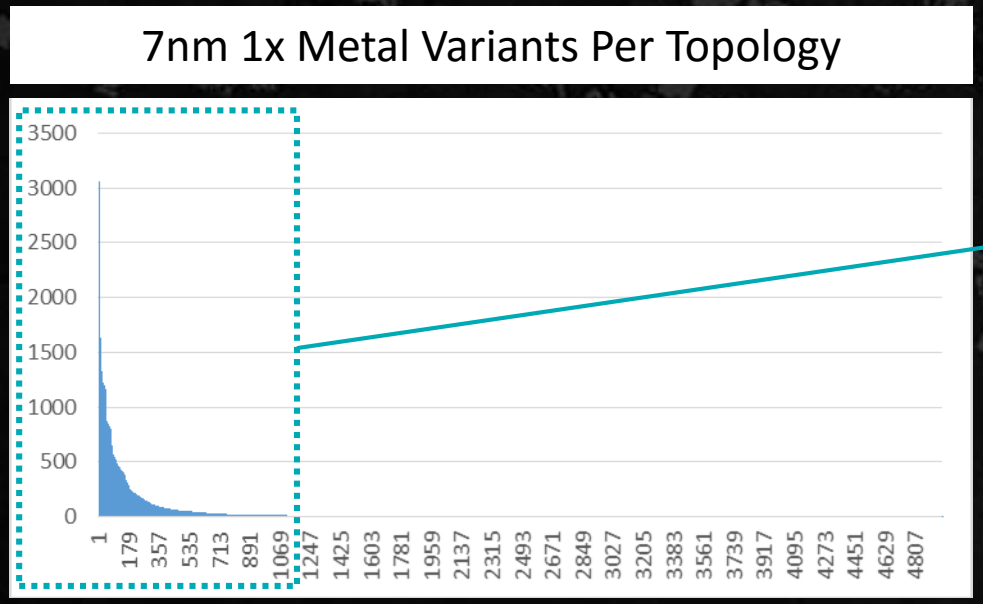


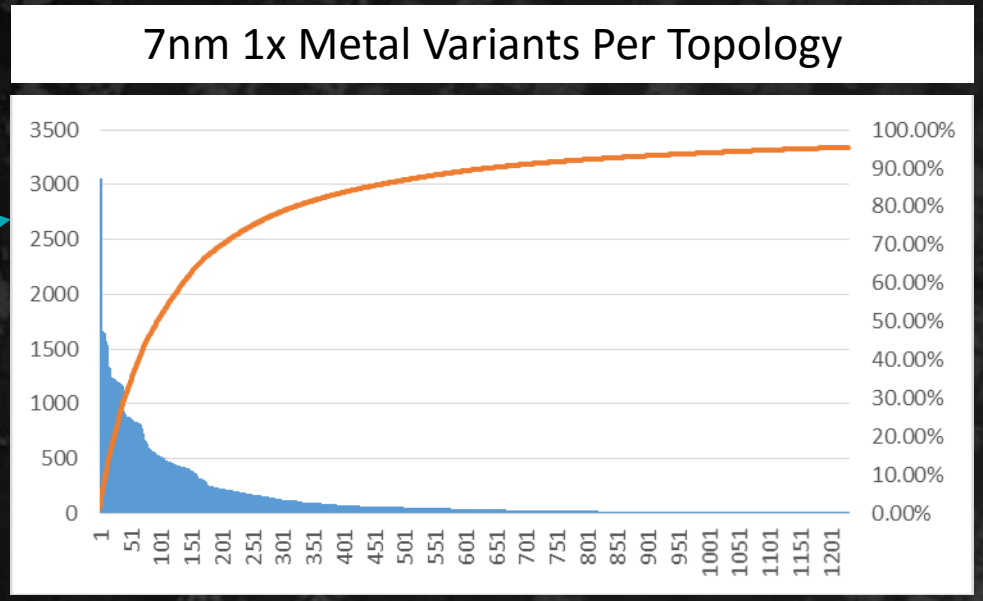
- The same circuit was implemented in 28, 20, 14, and 7 nm technologies.
- Pattern extraction was run on each and the number of unique topologies was counted.
- Note the use of a log scale.

Technology Node	Total Unique Topologies	Total Exact Patterns
28 nm	20,763,677	286,593,810
20 nm	835,025	39,977,934
14 nm	242,633	17,634,752
7 nm	4,964	197,257

LET'S TAKE A CLOSER LOOK AT THOSE 7NM PATTERNS

Technology Node	Capture Layer	Capture Max Window	Total Unique Topologies	Total Exact Patterns
7 nm	1x metal	3 pitch (7nm 1x metal rules)	4,964	197,257

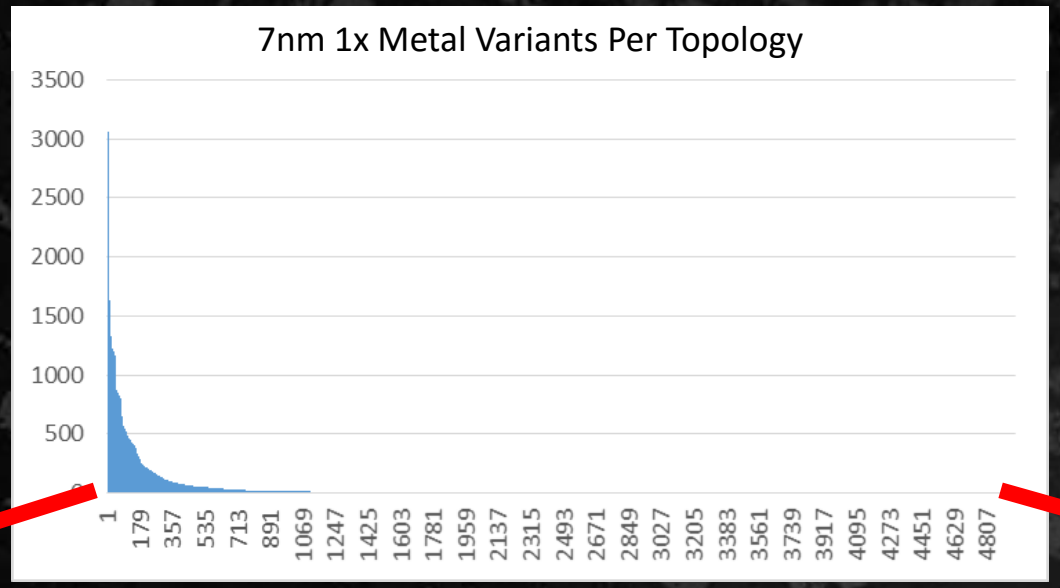


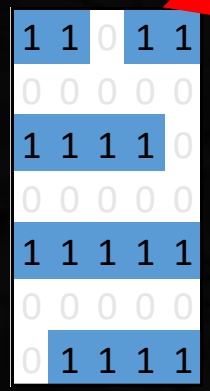


- Only a small number of topologies contribute to the vast majority of patterns
- There is still a long tail of topologies with small number of pattern variants (though much better than at older nodes)

- Looking more closely at the top 1231 topologies that contribute 95.45% of all exact patterns
- For comparison at 14nm, 23,056 topologies (out of 242,633) contribute 95.45% of all exact patterns

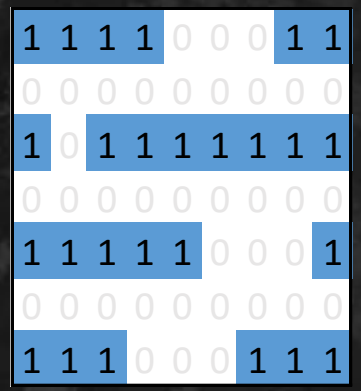
WHAT DOES IT MEAN FOR A TOPOLOGY TO HAVE MULTIPLE EXACT PATTERNS?





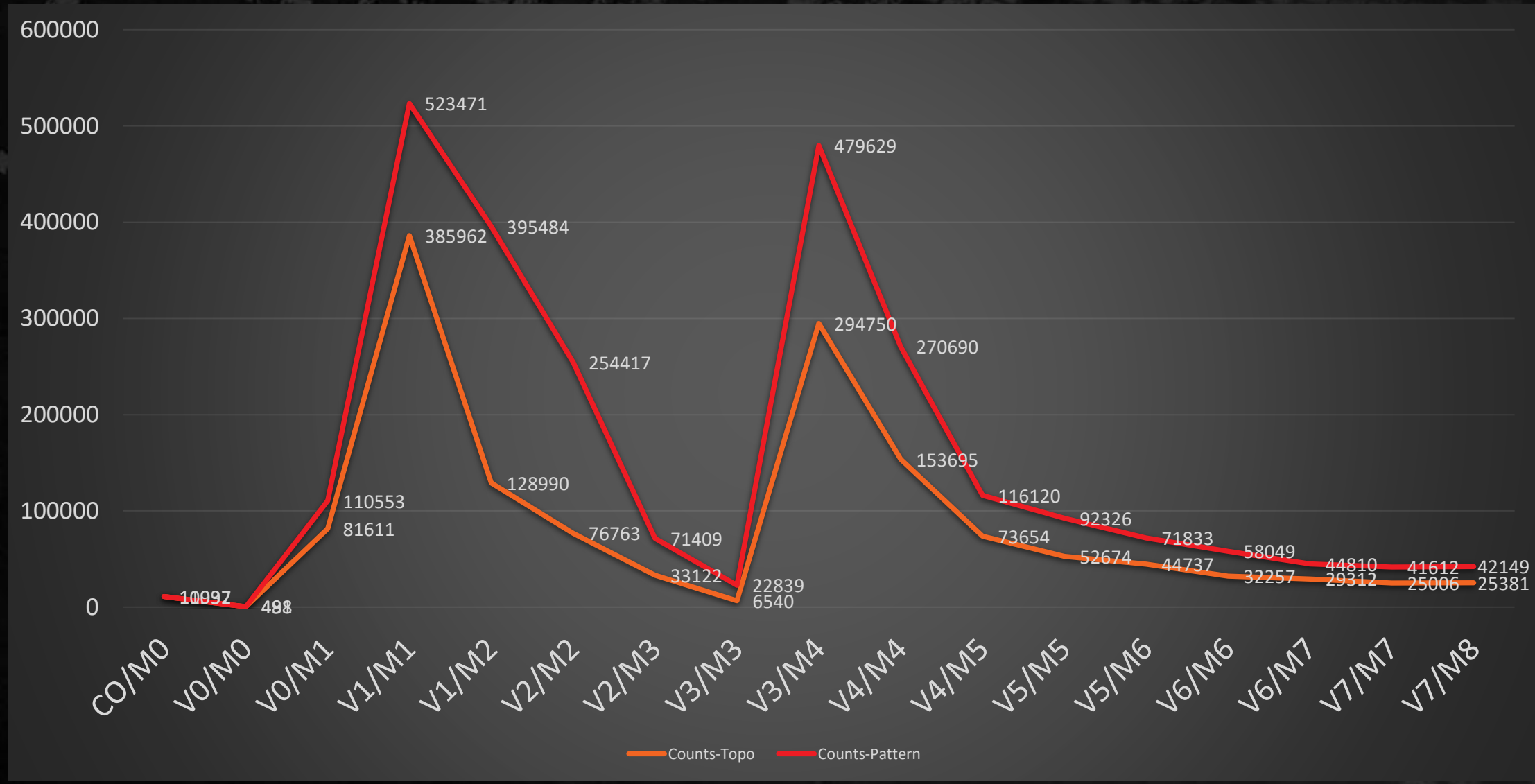
- This is our most common topology
- There are 3061 exact pattern variants of this topology
- All the variation is along the x dimension of this pattern!

- This is an example of a topology with only a single corresponding exact pattern
- Design rules only yielded a single exact variant in design!



TOPOLOGY AND PATTERN COUNT STATISTICS

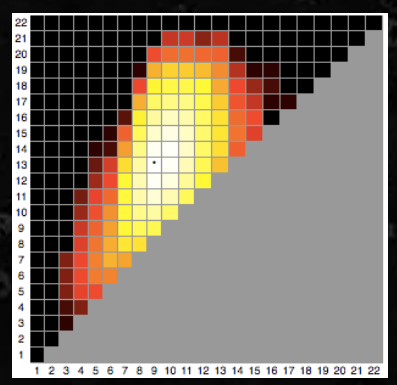
7NM MOL/BEOL LAYERS



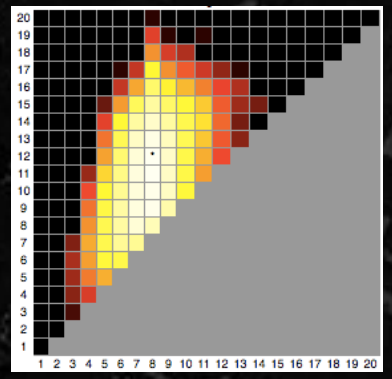
VIA ANCHORED PATTERNS

EVOLUTION OF COMPLEXITY ACROSS 14/20NM STACK

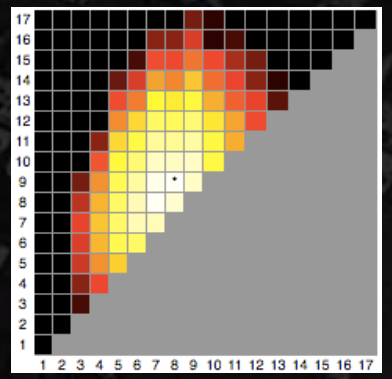
14NM



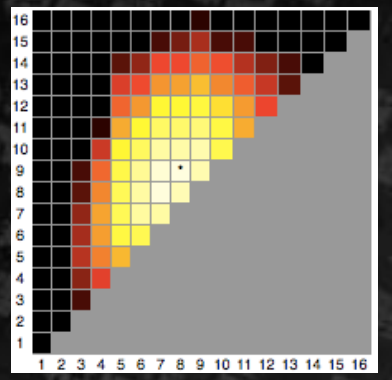
V1/M1



V1/M2

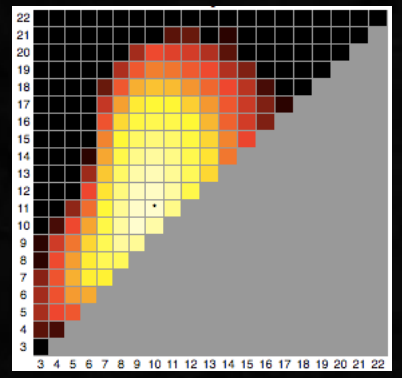


V2/M2

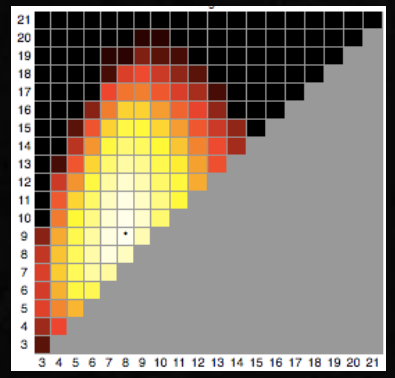


V2/M3

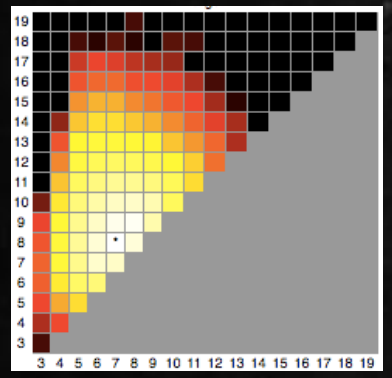
20NM



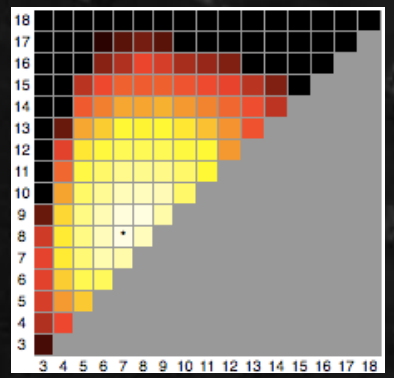
V1/M1



V1/M2



V2/M2

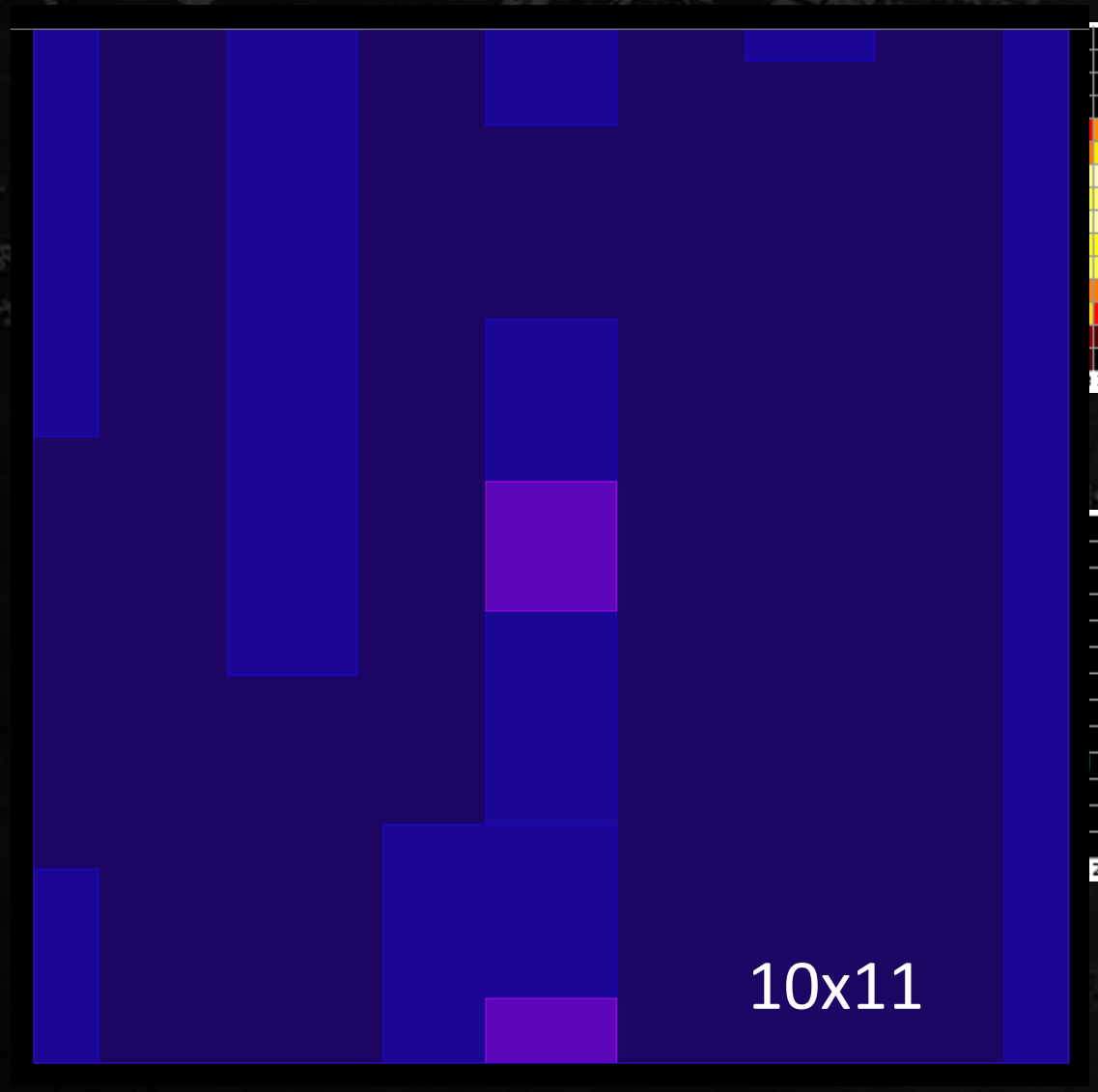


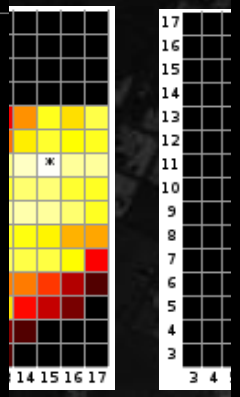
V2/M3

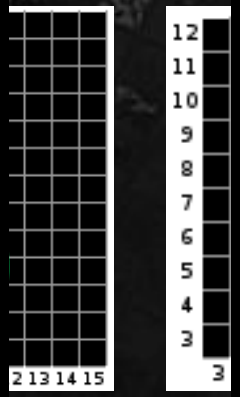
- Compared to 14nm, 20nm Vx/Mx patterns have a longer range towards the low complexity bins.
- Compared to 20nm, 14nm complexity bin coverage shows minor reduction in max scanlines.

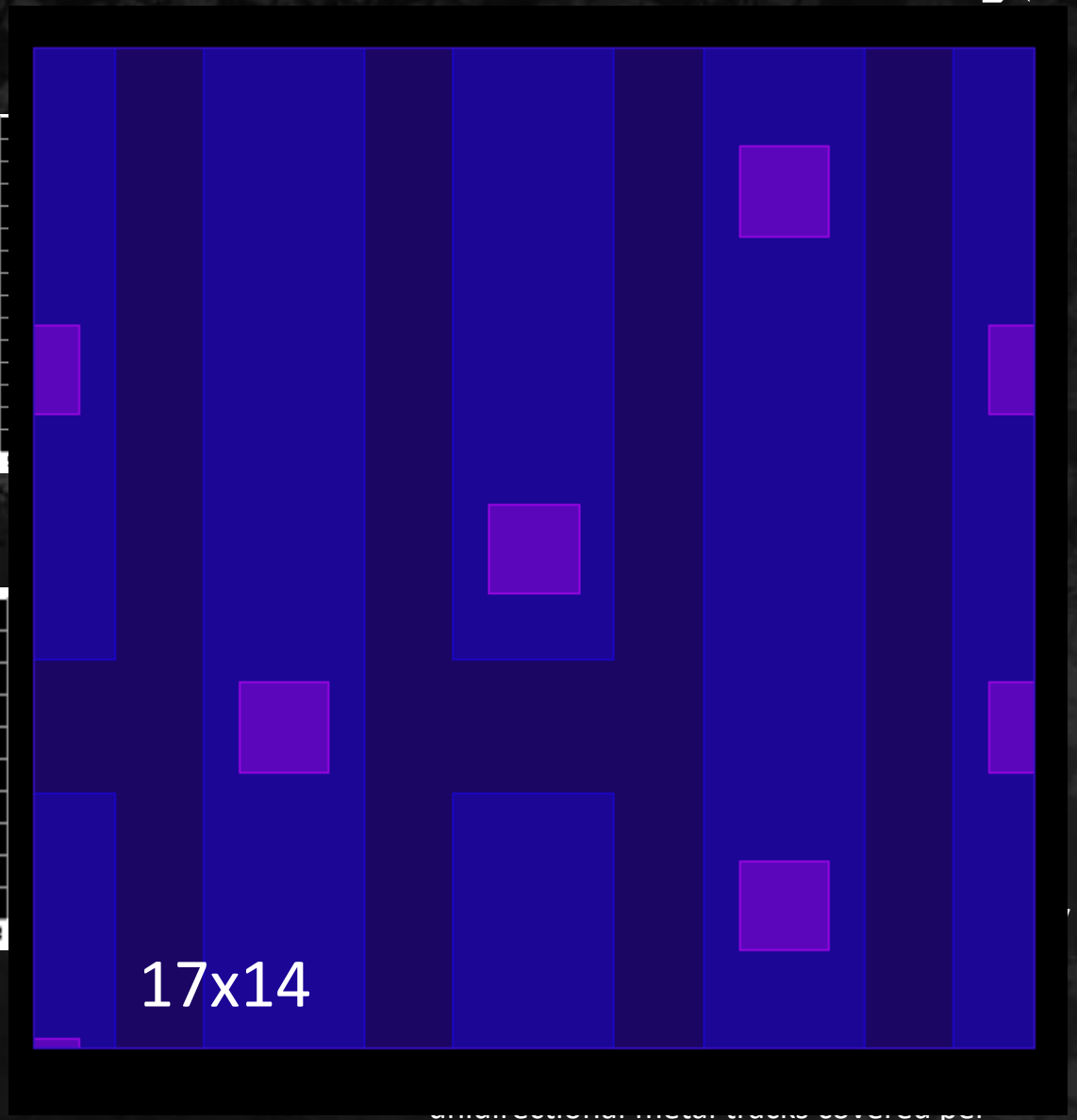
VIA ANCHORED PATTERNS

EVOLUTION OF COMPLEXITY ACROSS 7NM STACK





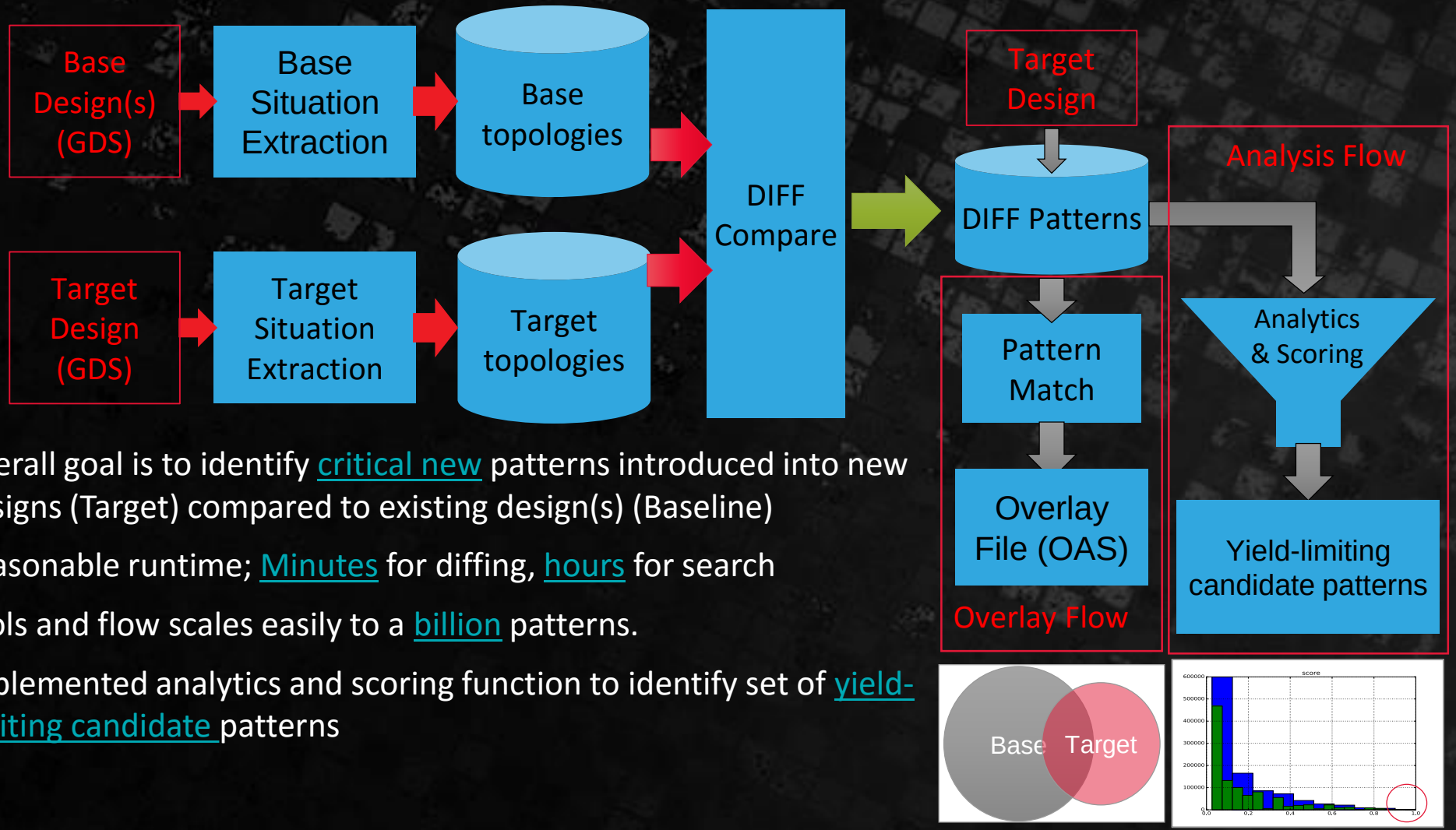




pattern.

LAYOUT DIFF AND ANALYTICS (DNA) FLOW

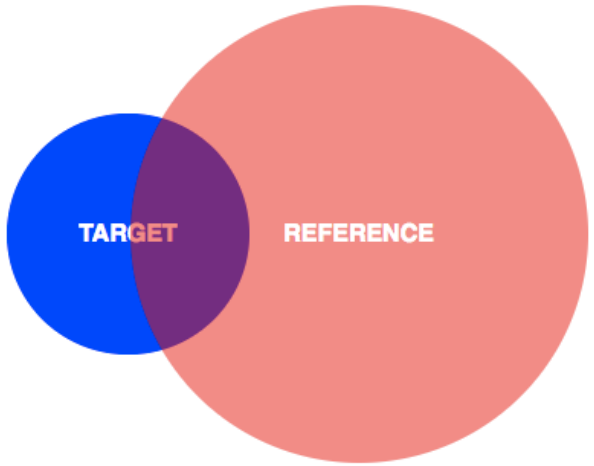
OVERVIEW



- Overall goal is to identify critical new patterns introduced into new designs (Target) compared to existing design(s) (Baseline)
- Reasonable runtime; Minutes for diffing, hours for search
- Tools and flow scales easily to a billion patterns.
- Implemented analytics and scoring function to identify set of yield-limiting candidate patterns

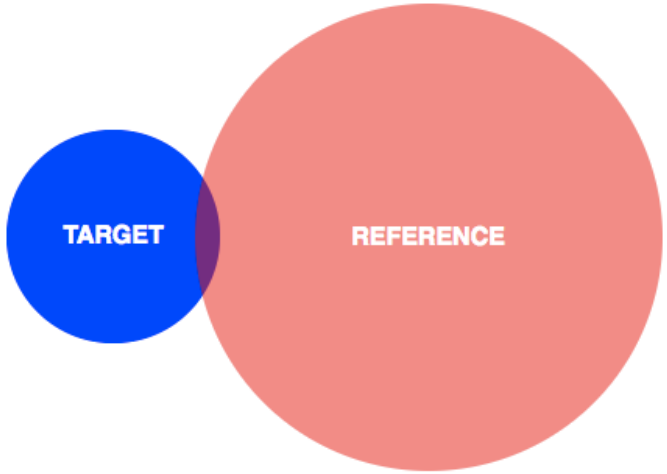
7NM VS. 14NM/20NM – COMMON METAL LAYERS

TOPOLOGIES AND PATTERNS



	Target (Not in Reference)	Intersecting	Reference (Not in Target)
All Target Signatures	451,276		
Signature Counts	255,443	195,833	1,418,550
All Reference Signatures		1,614,383	

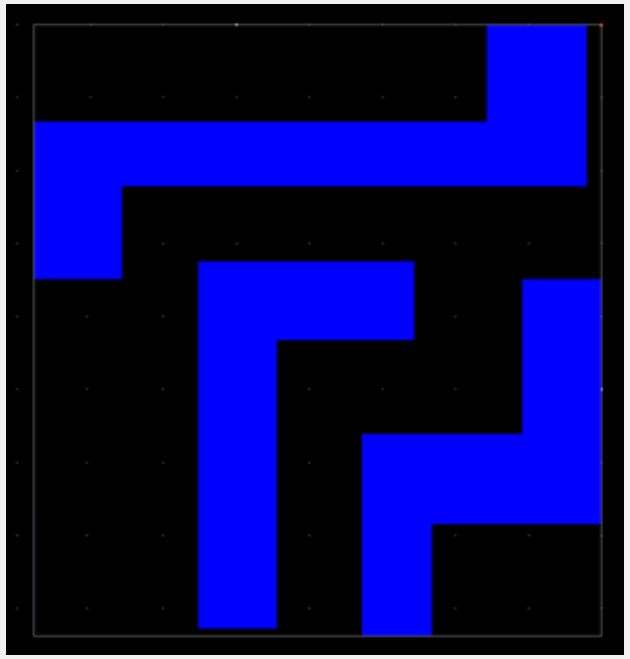
- ~55% signatures (for 7nm block) are new.



	Target (Not in Reference)	Intersecting	Reference (Not in Target)
All Target Patterns	8,506,983		
Pattern Counts	8,021,110	485,873	40,357,476
All Reference Patterns		40,843,349	

- ~92% patterns (for 7nm block) are new!

PATTERN ANALYTICS AND SCORING:
COMPLEXITY



Signature

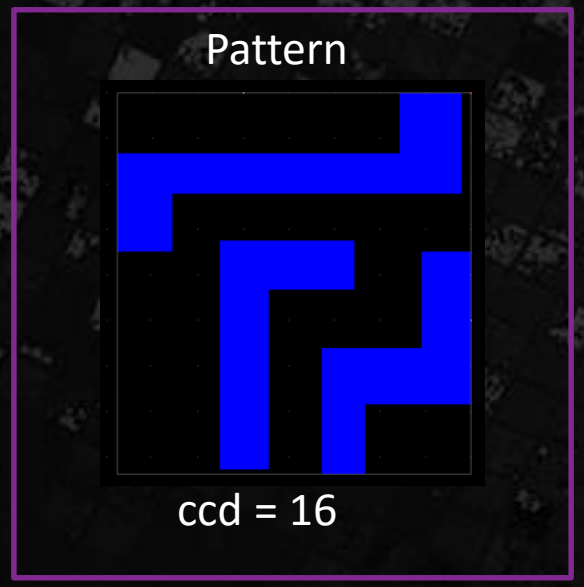
0	0	0	0	0	0	0	1	1	0
1	1	1	1	1	1	1	1	1	0
1	0	0	0	0	0	0	0	0	0
1	0	1	1	1	0	0	0	0	0
0	0	1	1	1	0	0	0	1	1
0	0	1	0	0	0	0	0	1	1
0	0	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	0	0	0
0	0	0	0	1	1	0	0	0	0

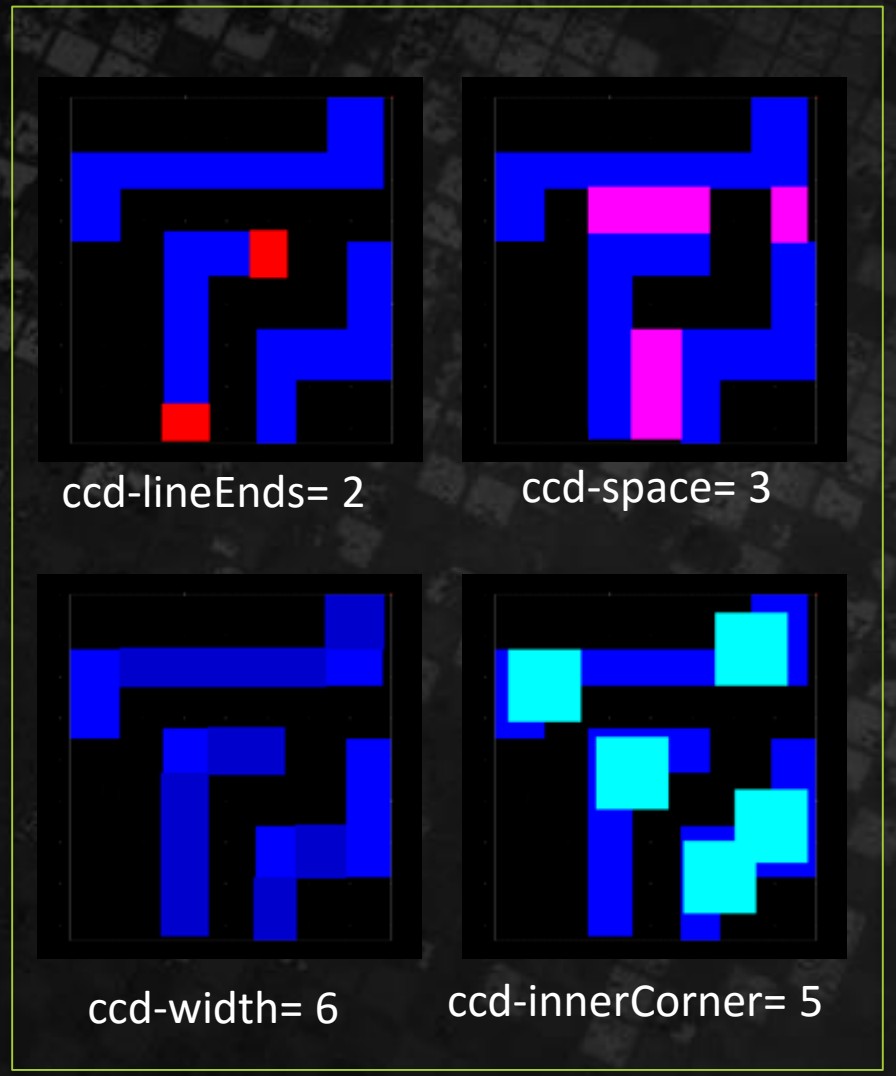
Cy =9

Cx = 10

Complexity: Cxy = Cx*Cy = 9*10 = 90

PATTERN ANALYTICS AND SCORING:
COUNT OF CRITICAL DIMENSIONS (CCD)



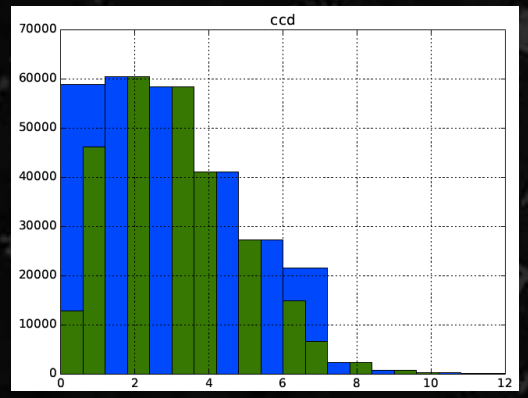


- Count of critical dimensions
  - Line-ends
  - Inner corners
  - Space/Width
  - Island shapes: includes –
    - Rect., U, L, Z, T with min-area

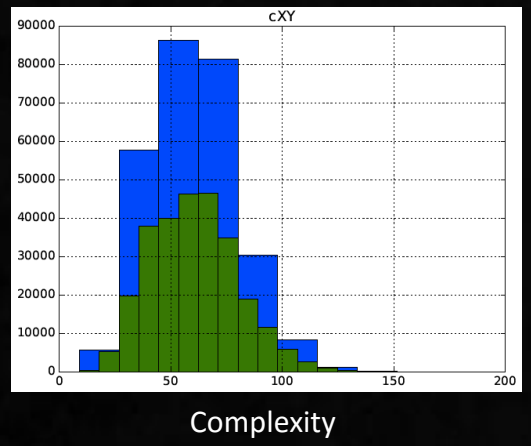
PATTERN ANALYTICS

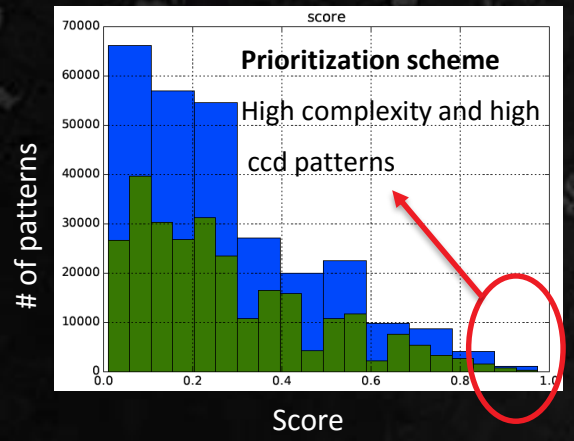
VIA ANCHORED PATTERNS

Pattern Analyses



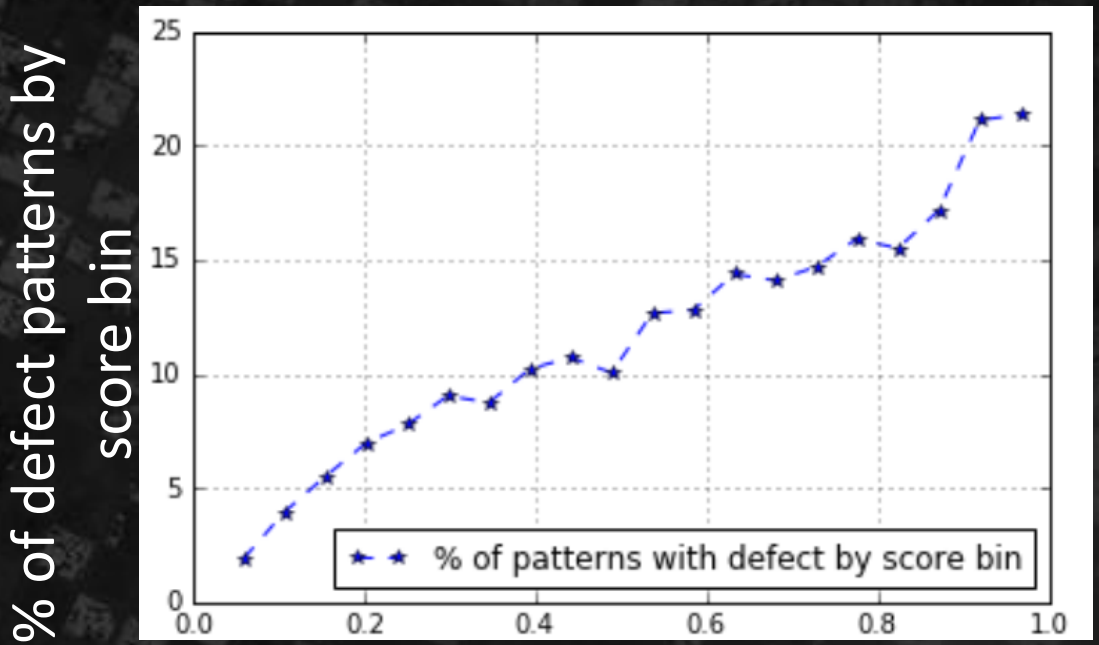
$f(ccd,Cxy) = Score \rightarrow$





Validation: Simulation Hotspot Coverage

Hotspot coverage by scored bin



EXAMPLES OF WEAK LITHO HOTSPOTS ON 2X METAL LEVELS

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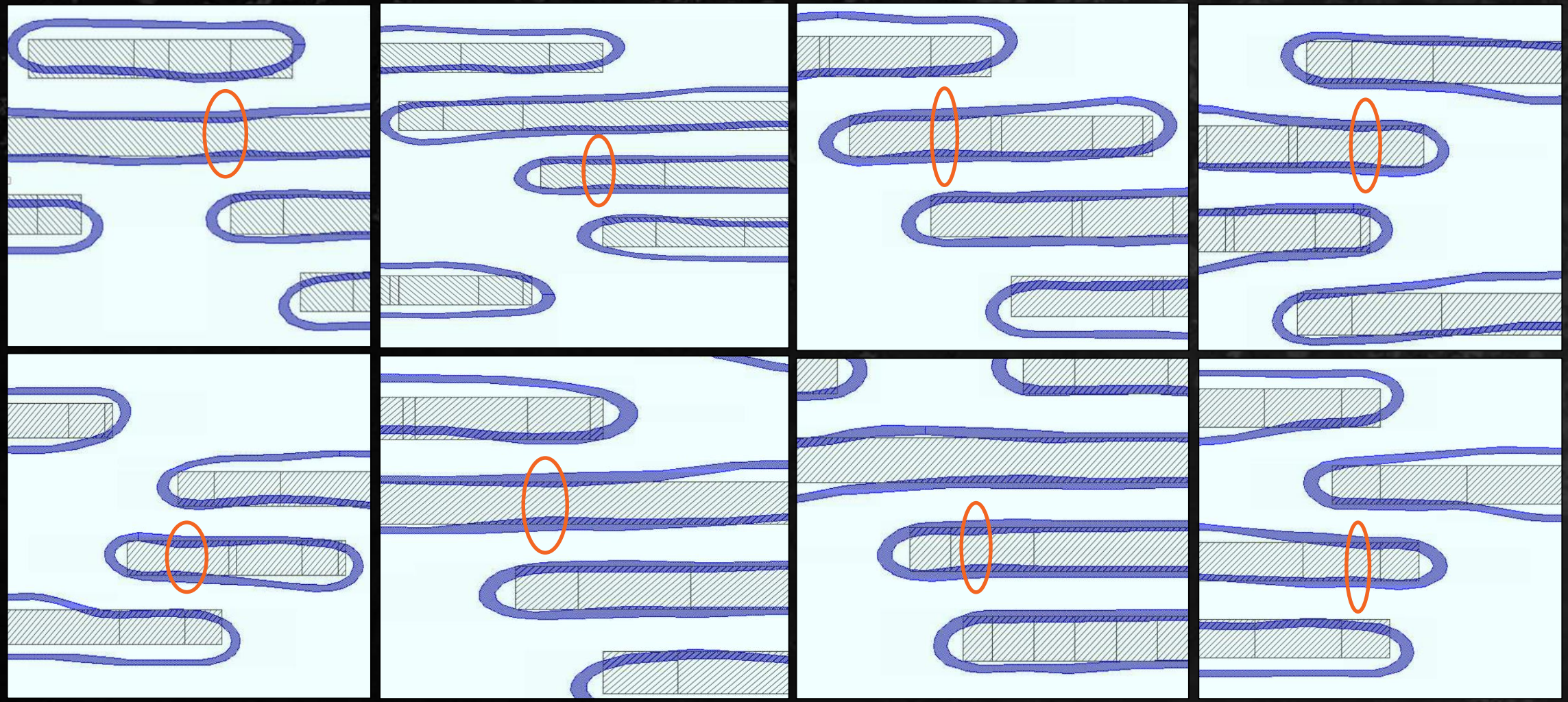
2X Metal PW necking at Dense-ISO transition



TRACKING TOPOLOGIES AND PATTERNS ACROSS PRODUCTS AND TECHNOLOGIES

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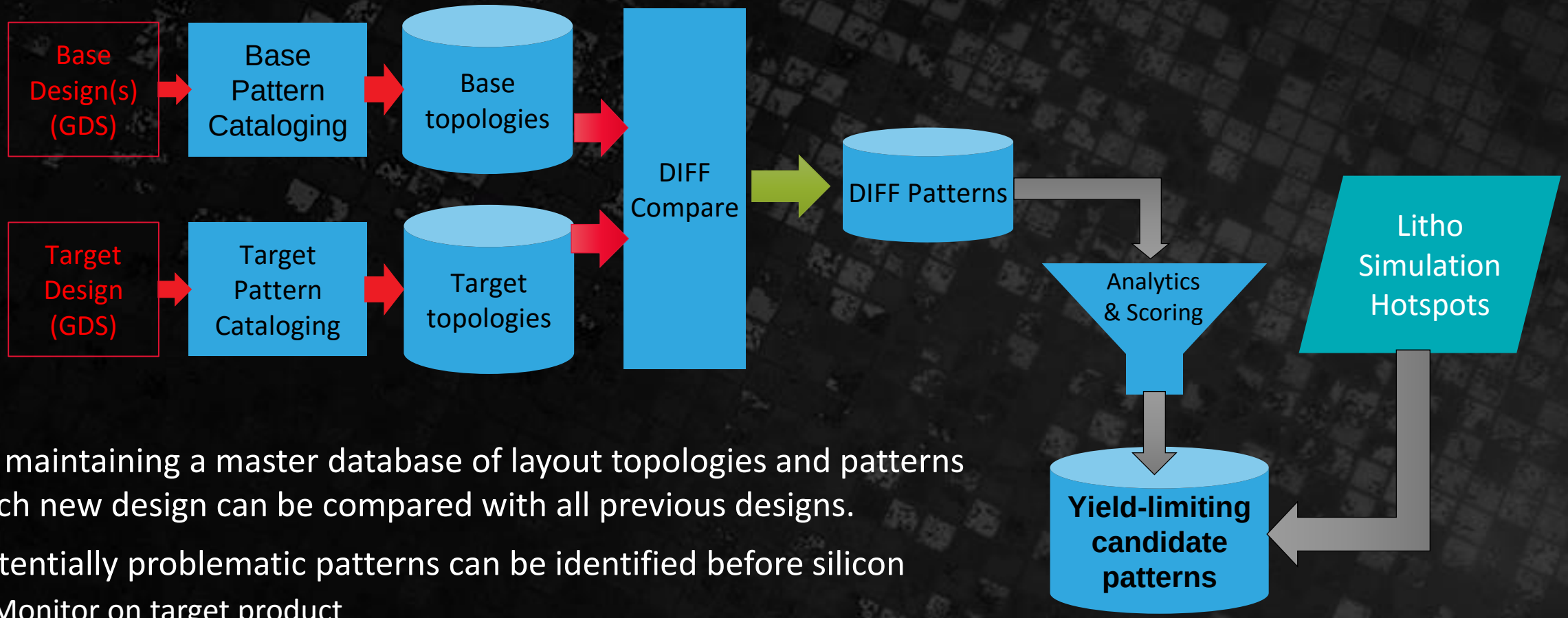
OVERVIEW

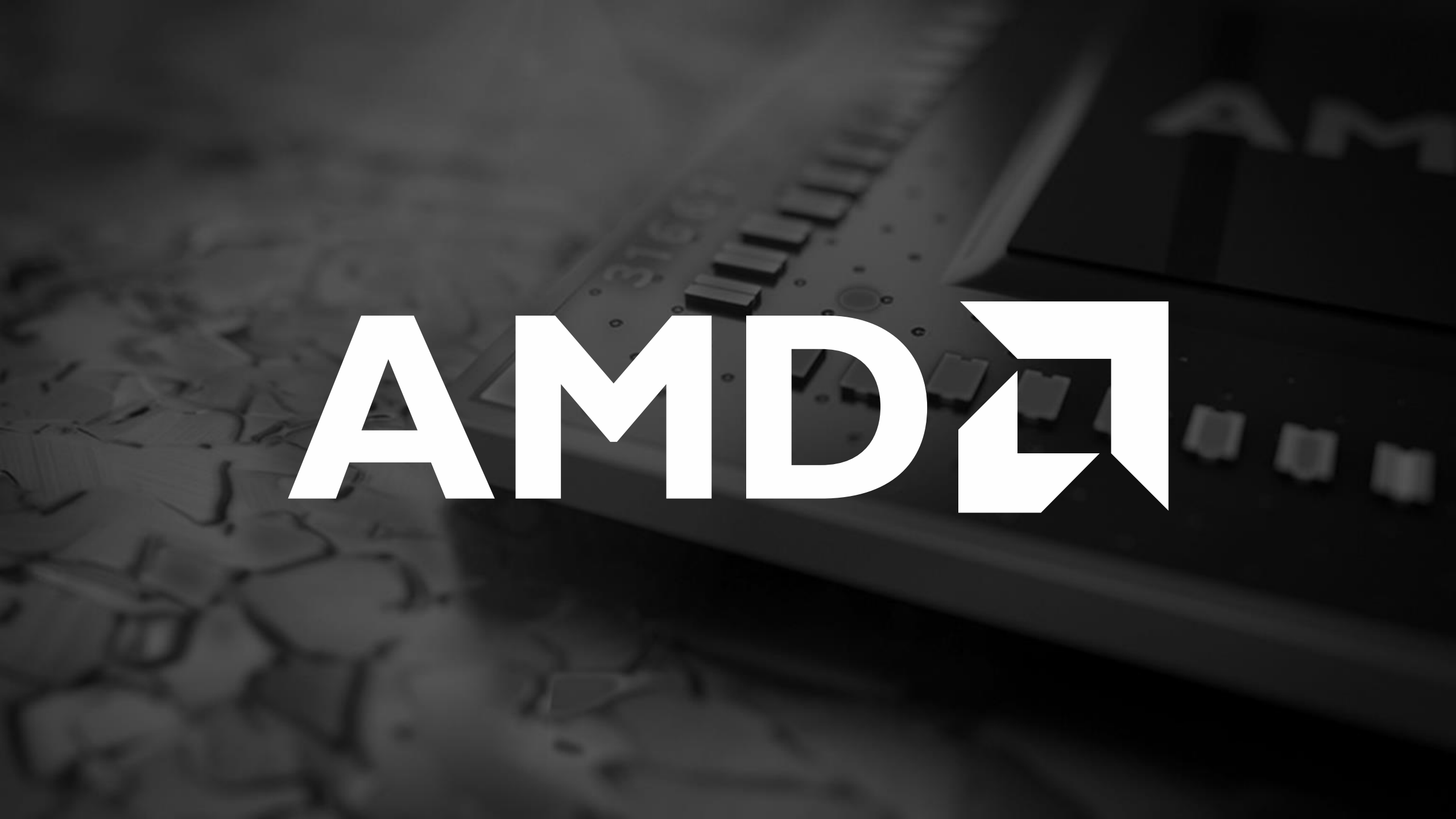


- By maintaining a master database of layout topologies and patterns each new design can be compared with all previous designs.
- Potentially problematic patterns can be identified before silicon
  - Monitor on target product
  - Consider removing from future designs

SUMMARY

AMD

- Previous pattern cataloging work was extended to 7nm and the trend toward lower layout complexity continues.
- Pattern-based analysis of 7nm metal stack was completed
- Analysis at 7nm suggested that there is some signal to identify risky patterns based on pattern features
- Preliminary analysis of pattern features shows some correlation with simulated process risk
- Future work includes evaluating tradeoffs in DFM layout optimization and layout complexity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