DATASHEET

cadence®

Conformal Equivalence Checker

Formal verification technology for fast and accurate bug detection and correction

Cadence® Conformal® Equivalence Checker (EC) pioneers a solution to verify and debug multimillion–gate designs without using test vectors. It is the only equivalence checking tool in the industry that can verify the complete full design context from RTL to final LVS netlist (SPICE) while delivering truly independent verification. With Conformal Equivalence Checker, designers can verify the widest variety of circuits, including complex arithmetic logic, datapaths, memories, and custom logic.

Conformal EC

Conformal EC is the most widely supported independent equivalence checking product in the industry. Compared to the competition, it works on more products at various stages, including physical design closure products, advanced synthesis engines, ASIC libraries, and IPs.

Conformal EC is available in three configurations: L offers core equivalence checking technology; XL adds automated checking of complex datapaths and equivalence checking of the final place-and-route netlist; GXL further adds transistor circuit analysis for custom designs and embedded memories.

Engineers can use the GXL offering with custom embedded memories, arithmetic blocks, datapaths, standard and extended libraries, and all other custom and semi-custom digital circuit functions. Circuit styles include standard and complex Boolean functions, latches and registers, pass-gate, transmission-gate, tri-state switch logic, pre-charged logic cells, domino logic blocks, and dual-rail.

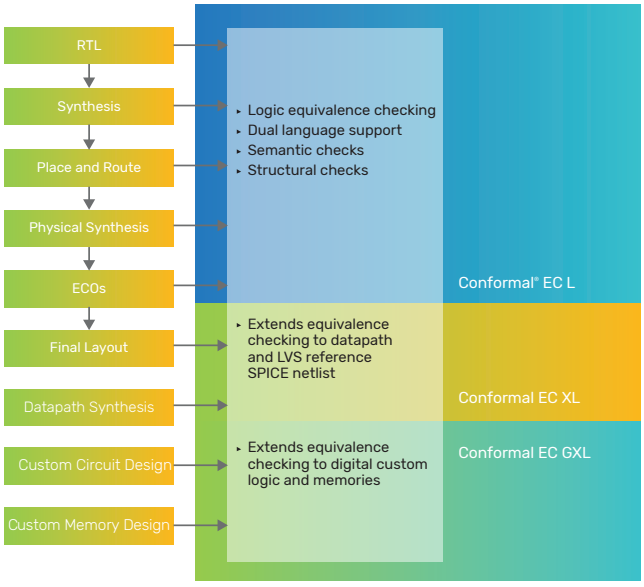

Figure 1: Conformal EC offers a complete solution, from RTL to final layout, to drive convergence on design goals

Benefits

- Exhaustively verify multimillion-gate ASICs several orders of magnitude faster than traditional gate-level simulations
- Reduce the risk of missing critical bugs with independent verification technology
- Detect and correct bugs more accurately throughout the entire design flow
- Extend equivalence checking to complex datapaths and close the RTL-to-layout verification gap (XL configuration)
- Ensure that RTL models perform the same functions as the corresponding transistor circuits implemented on silicon (GXL configuration)

Features

Conformal EC L

Equivalence checking

During development, a design will undergo numerous iterations, and each step might introduce logical bugs. Conformal EC L helps designers to identify and correct the violations immediately by checking the functional equivalence of different versions of a design at various stages, thereby, maintaining the initial design intent. Conformal EC L is best suited for basic designs with less complex synthesis optimizations or gate-to-gate equivalence runs.

Design flow independence

Conformal EC L checks the design process independently to avoid discrepancy between design implementation and verification products. The tool includes technologies developed independently from the design flow, such as production proven HDL parsing, synthesis, mapping, optimization, and datapath algorithms. With Conformal EC L, you will catch the maximum number of design bugs.

Integrated environment

Conformal EC L offers an intuitive GUI for setup and debugging. It identifies the root causes of mismatches with the following features:

- Graphical debugging via an integrated schematic viewer that shows logic values for each error vector
- Full cross-highlighting between the RTL model and circuit
- Automatic error candidate identification with assigned and weighted percentages
- Logic-cone pruning to focus debugging on relevant information

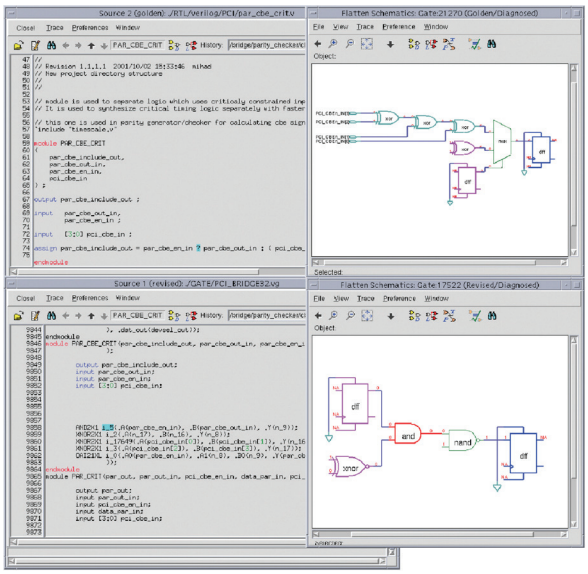

Figure 2: Conformal EC has an easy-to-use GUI with extensive diagnosis and debugging capabilities

Conformal EC XL

Datapath synthesis verification

Many modern designs are more difficult to formally verify since they are optimized with complex arithmetic operations. In the past, designers relied on simulation to verify datapath blocks, but simulation runtimes are exceedingly long, and the results can be incomplete.

Conformal EC XL pioneers a formal solution that exhaustively verifies complex datapath blocks without using test vectors. It can handle a wide variety of datapath structures required for high-performance designs:

- Automatic flat datapath module verification: enable easy verification without manually specifying boundaries or architectures in the flattened netlist, automatically verify merged operators, compare circuitry that has gone through expression optimization, and automatically verify multipliers with standard architectures and dynamic structures
- Advanced pipelining check and diagnosis: verify proper implementation of pipelined designs
- Carry-save verification capability: allow verification of circuits containing carry-save transformations introduced during optimization for a sequences of adders, multipliers, and registers

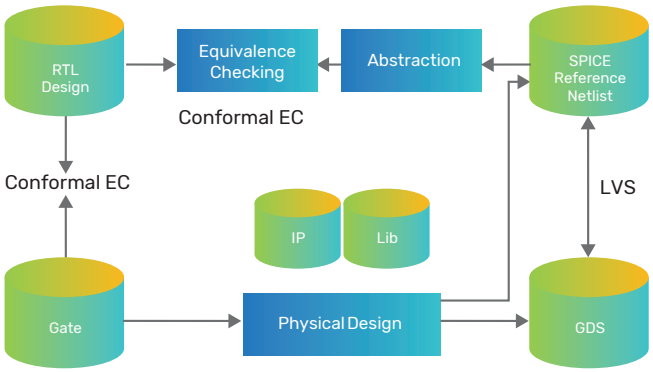

Figure 3: Conformal EC provides complete verification from RTL to SPICE

Final circuit verification

Conformal EC XL is the only verification product that provides a complete verification solution from RTL to final layout, driving convergence on original design goals. Its functionally compares a SPICE netlist created for LVS or extracted from GDS to the RTL or gate model. This process ensures that the circuit on silicon has the same intent as the initial design that was verified.

Smart setup and diagnosis

Conformal EC XL includes a set of intelligent analysis commands to ease setup and diagnosis. For example, Smart setup investigates the current environment and automatically fixes common setup issues for new users. In tandem, non-equivalent analysis can be invoked if non-equivalences are encountered and can present concise root cause information for quicker debug.

Parallel processing

For larger and more complex designs, running comparison and datapath analysis on many cores simultaneously can reduce overall verification time. LSF is also supported.

Conformal EC GXL

Custom logic abstraction

Conformal EC GXL analyzes digital transistor circuits and abstracts an equivalent logical Verilog model. The underlying abstraction algorithms are more powerful than pattern based solutions. A Verilog gate logic model of the abstracted circuit can be used for the following:

- Equivalence checking
- Fault grading: preserve the circuit hierarchy and structure for maximum debugging efficiency
- Emulation: provide accurate emulation models for actual transistor-level circuits
- Simulation acceleration: run many times faster than SPICE circuit simulation

Memory verification

Traditional and symbolic simulation tools do not scale for verifying today's memory functions and their ever increasing complexity. Conformal EC GXL provides fast exhaustive logic verification without the need for a dedicated testbench. Conformal EC GXL generates memory-primitive models for Verilog system simulation and complete logic function verification of the transistor circuit design using abstraction and equivalence checking. Conformal EC GXL has the following features:

- Intuitive graphical interface to generate specific primitives
- Generated primitives are address, word, and column MUX-configurable
- All read-write, read-only, and write-only combinations can be generated
- Generated simulation models have the highest performance and contain built-in assertions for trapping illegal memory use, such as address collision and simultaneous read-write

Platforms

- Linux (64-bit)

Language Support

- Verilog (1995, 2001, 2005, 2009, 2012)
- SystemVerilog
- VHDL (1987, 1993, 2008)
- SPICE (traditional, LVS)
- EDIF
- Liberty
- Mixed languages

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