DATASHEET

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Conformal ECO Designer

ECO automation for greater predictability and design convergence

Cadence® Conformal® ECO Designer enables designers to implement RTL engineering change orders (ECOs) for pre-and post-mask layout, and offers early ECO prototyping capabilities for driving critical Yes/No project decisions. Cadence ECO solutions combine automatic ECO analysis, logic optimization, and design netlist modification with world-class equivalence checking to provide superior performance, productivity, and predictability, helping you achieve convergence on your design goals.

Cadence ECO Solutions

After transistors and layout are finalized, designers must use Engineering Change Orders (ECOs) to implement surgical-changes to designs without requiring the schedule cost of re-running a full implementation flow. All ECOs focus on delivering products to market as soon as possible with minimum violations. ECOs can span a variety of scenarios from adding or removing logic in a design, to more subtle changes such as cleaning up routing; Cadence offers the only truly automated ECO solution from RTL to GDSII.

Regardless of design flow stage, Cadence offers comprehensive and automatic ECO solutions. Conformal ECO Designer handles ECO automation for RTL-level functional changes; Genus™ Synthesis Solution manages logic synthesis and ECO logic optimization; and Innovus™ Implementation System manages the physical implementation of the ECO changes. The combination brings automation and predictability to the ECO process.

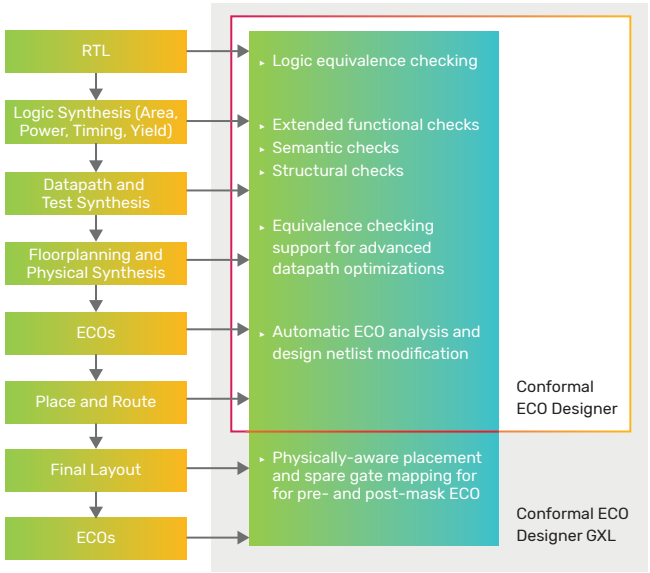

Figure 1: Conformal ECO Designer offers automatic ECO analysis and design netlist modification

Conformal ECO Designer

Conformal ECO Designer is a unique technology that offers-functional ECO analysis, optimization, and generation capability. It combines proven equivalence checking and functional checks, and uses formal techniques to analyze, abstract, and implement the functional ECO.

Conformal ECO Designer is available in two configurations: an XL offering, which targets primarily the pre-mask ECO flow, and a GXL offering, which targets the pre-mask and post-mask ECO flow with metal layers and spare gates. The GXL configuration leverages physical database knowledge to generate ECO placement guidance for downstream place-and-route tools.

Benefits

- Provide faster turnaround time by minimizing manual intervention and eliminating time-consuming implementation iterations
- Estimate ECO feasibility at an early stage by quantifying design intent
- Implement complex ECOs that are typically not manually attempted
- Enable front-end designers to deliver netlists to ASIC vendors earlier
- Allow for metal-only ECOs to reduce manufacturing costs and drive design convergence faster
- Reduce verification time significantly using abstraction techniques to verify multi-million gate designs vs. traditional gate-level simulation
- Reduce the risk of missing critical bugs through independent verification technology

Features

Conformal ECO Designer combines logic equivalence-checking for the most complex SoC and datapath-intensive designs with functional ECO analysis, design netlist modification, and logic optimization.

Equivalence checking for ECOs

During development, a design will undergo numerous iterations, and each step might introduce logical bugs. Conformal ECO helps designers to identify and correct violations immediately by checking the functional equivalence of different versions of a design at various stages.

In an ECO implementation process, equivalence checking-plays an important role. It identifies the incompatible-modules and logic cones during ECO analysis. For instance, in Figure 2, the original netlist is compared against the new netlist to determine what has changed. In addition, equivalence checking is used at the end of the process to ensure the ECO implementation was successful in both front-end and back-end signoff.

Functional ECO analysis

Conformal ECO Designer provides an ECO analysis engine to identify the discrepancy between the original design netlist and the new one. With this engine, rather than analyzing ECOs on the entire design, users can more efficiently inspect specific modules within the design hierarchy. Once the ECO analysis is completed and the logic changes optimized, Conformal ECO Designer will modify the original netlist to add new functions and output an ECO netlist. In addition, Conformal ECO Designer can create an ECO script that can be used to directly change the place-and-route database.

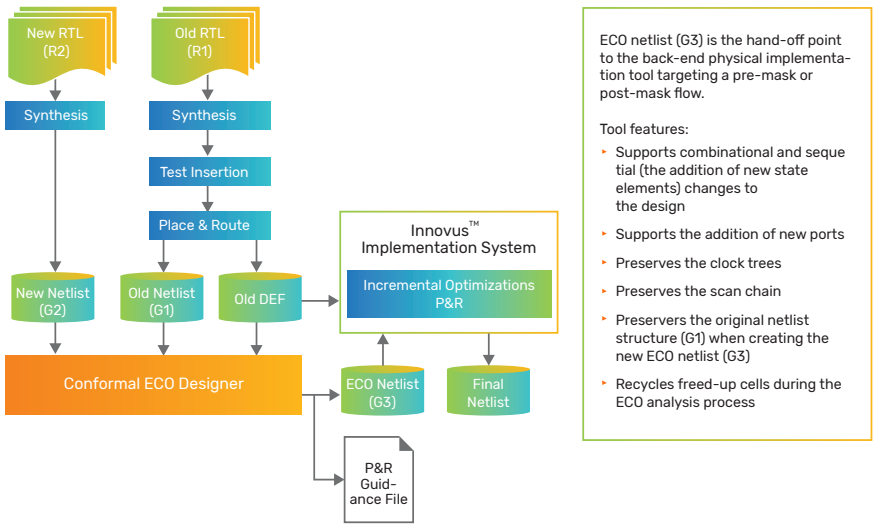

Figure 2: The Conformal ECO Designer implementation flow

Spare gate mapping for post-mask ECOs

Conformal ECO Designer (GXL) can also read the DEF layout database corresponding to the original design netlist, LEF, Liberty synthesis libraries, and SDC to optimally map ECO logic to standard cell and gate-array spare gates. The mapping engine will be influenced by timing and spare cell location. With this function, designers can estimate ECO feasibility at an early stage and drive convergence in the back-end implementation flow.

Conformal ECO Designer (GXL) can also recycle freed-up-cells in the ECO mapping process. The output is the ECO netlist and a spare gate mapping file, which instructs the place-and-route tool on how to map the newly added ECO logic to specific spare logic resources in the layout.

Integrated environment

Conformal ECO Designer offers an intuitive GUI for setup and debugging. It identifies the root causes of mismatches with the following features:

- Graphical debugging via an integrated schematic viewer that shows logic values for each error vector
- Full cross-highlighting between RTL model and circuit
- Automatic error candidate identification with assigned and weighted percentages
- Logic-cone pruning to focus debugging on relevant information

Smart setup and diagnosis

Conformal ECO Designer includes a set of intelligent analysis commands to ease setup and diagnosis. For example, Smart setup investigates the current environment and automatically fixes common setup issues for new users. In tandem, non-equivalent analysis can be invoked if non-equivalences are encountered and can present concise root cause information for quicker debug. For hierarchical designs, Conformal ECO Designer includes smart technology for accelerating setup requirements through boundary condition profiling.

Platforms

- Linux (32-bit, 64-bit)

Language Support

- Verilog (1995, 2001, 2005, 2009, 2012)
- SystemVerilog
- VHDL (1987, 1993, 2008)
- SPICE (traditional, LVS)
- EDIF
- Liberty
- Mixed languages

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- Cadence application engineers can answer your technical questions by telephone, email, or internet—they can also provide technical assistance and custom training.
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