INVENTIVE

CMP Model Application in RC and Timing Extraction Flow

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Outline

- Problems Due to Thickness/Topography Variation
  - Physical: Copper Pooling and Yield Issues
  - Electrical: Timing Failures and Performance Loss Due to Excessive Guardband
- Modeling Technology & Product Overviews
  - Model Calibration and Validations
  - Product (CMP Predictor) & Features
- Problem Mitigation Approaches
  - Integration Flow with RC Extraction Tool
  - RC Extraction and Timing Results

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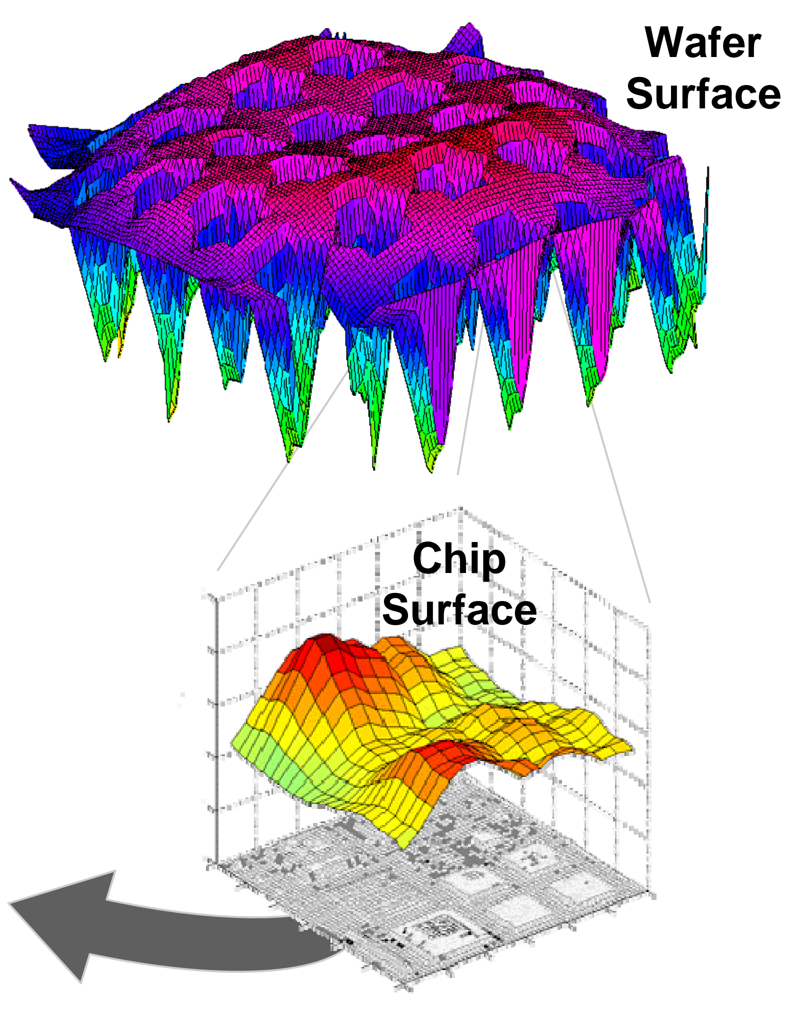
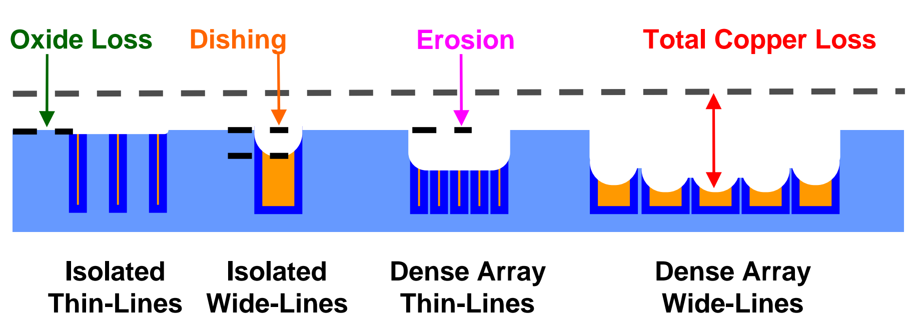
Interconnect Thickness Variation

- Significant Variation
  - Thickness Variation: 10% to 40%
  - Width Variation: 10% to 40%
- Due to Design Layout
  - Varying Feature Density
  - Varying Feature Widths
- Has Impact on Manufacturing
  - Functional Yield Loss
  - Parametric Timing Failures





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Accounting For Variation in Design Process

Actual Thickness

Systematic Thickness Manufacturing Variation Guardband

+20%

-20%

Systematic & Random Thickness Manufacturing Variation Guardband

Current "2D" Methodology is Conservative Full Chip Guardband for Both Systematic and Random Thickness Variation (+- 20%)

Actual Thickness

+10%

-10%

Random Thickness Manufacturing Variation Guardband

Cadence "3D" Methodology Eliminates Systematic Guardband Leaving Only a Relatively Small Random Thickness Variation (+/- 10%)

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Cadence CMP Model Calibration

Calibration Step

Fabricate Test Wafer (ECP/CMP)

Data from ECD & CMP Processing Results

Measurement Data From Test Wafer

Test Wafer Design Layout File

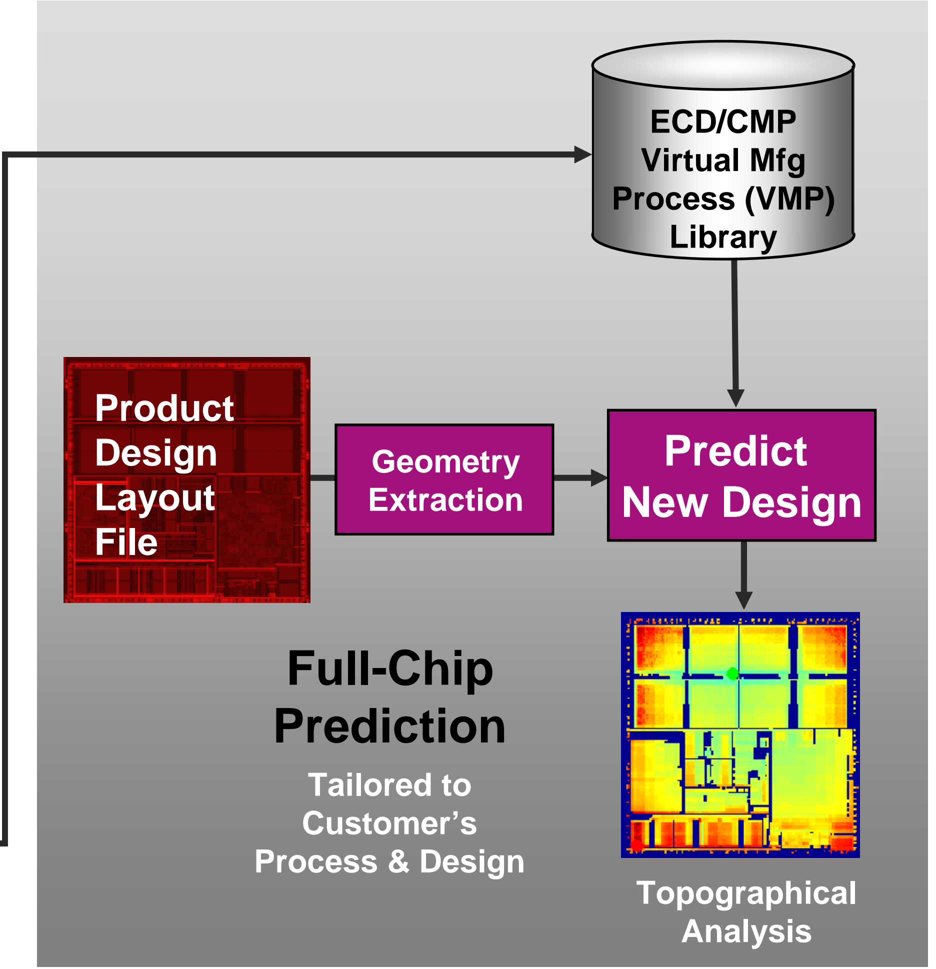
Geometry Extraction

Calibrate Model

Semi-Physical Model Tailored to Specific Process

ECD/CMP Virtual Mfg Process (VMP) Library

Prediction Step



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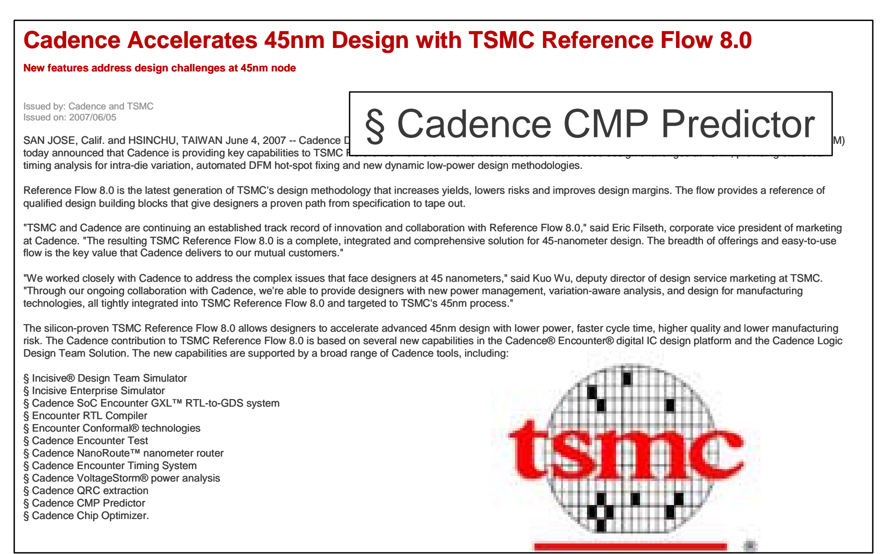
Supported By Leading Edge Foundries and Many Top Tier IDM's

- Virtual Manufacturing Process Libraries created for each Foundry Process Node (65nm, 45nm, …)
- VMP's Calibrated by Foundries/IDM's
- VMP's provided by foundries/IDM's to Design Teams
- Half node support



Cadence Accelerates 45nm Design with TSMC Reference Flow 8.0

New features address design challenges at 45nm node

Issued by: Cadence and TSMC
Issued on: 2007/06/05

§ Cadence CMP Predictor

SAN JOSE, Calif. and HSINCHU, TAIWAN June 4, 2007 -- Cadence D … M)
today announced that Cadence is providing key capabilities to TSMC R …
timing analysis for intra-die variation, automated DFM hot-spot fixing and new dynamic low-power design methodologies.

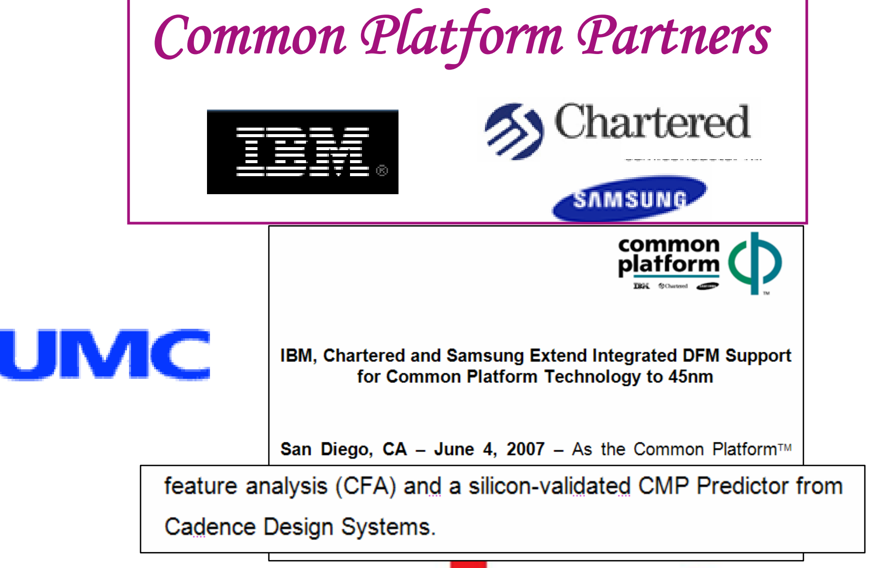
Reference Flow 8.0 is the latest generation of TSMC's design methodology that increases yields, lowers risks and improves design margins. The flow provides a reference of qualified design building blocks that give designers a proven path from specification to tape out.

"TSMC and Cadence are continuing an established track record of innovation and collaboration with Reference Flow 8.0," said Eric Filseth, corporate vice president of marketing at Cadence. "The resulting TSMC Reference Flow 8.0 is a complete, integrated and comprehensive solution for 45-nanometer design. The breadth of offerings and easy-to-use flow is the key value that Cadence delivers to our mutual customers."

"We worked closely with Cadence to address the complex issues that face designers at 45 nanometers," said Kuo Wu, deputy director of design service marketing at TSMC. "Through our ongoing collaboration with Cadence, we're able to provide designers with new power management, variation-aware analysis, and design for manufacturing technologies, all tightly integrated into TSMC Reference Flow 8.0 and targeted to TSMC's 45nm process."

The silicon-proven TSMC Reference Flow 8.0 allows designers to accelerate advanced 45nm design with lower power, faster cycle time, higher quality and lower manufacturing risk. The Cadence contribution to TSMC Reference Flow 8.0 is based on several new capabilities in the Cadence® Encounter® digital IC design platform and the Cadence Logic Design Team Solution. The new capabilities are supported by a broad range of Cadence tools, including:

§ Incisive® Design Team Simulator
§ Incisive Enterprise Simulator
§ Cadence SoC Encounter GXL™ RTL-to-GDS system
§ Encounter RTL Compiler
§ Encounter Conformal® technologies
§ Cadence Encounter Test
§ Cadence NanoRoute™ nanometer router
§ Cadence Encounter Timing System
§ Cadence VoltageStorm® power analysis
§ Cadence QRC extraction
§ Cadence CMP Predictor
§ Cadence Chip Optimizer.



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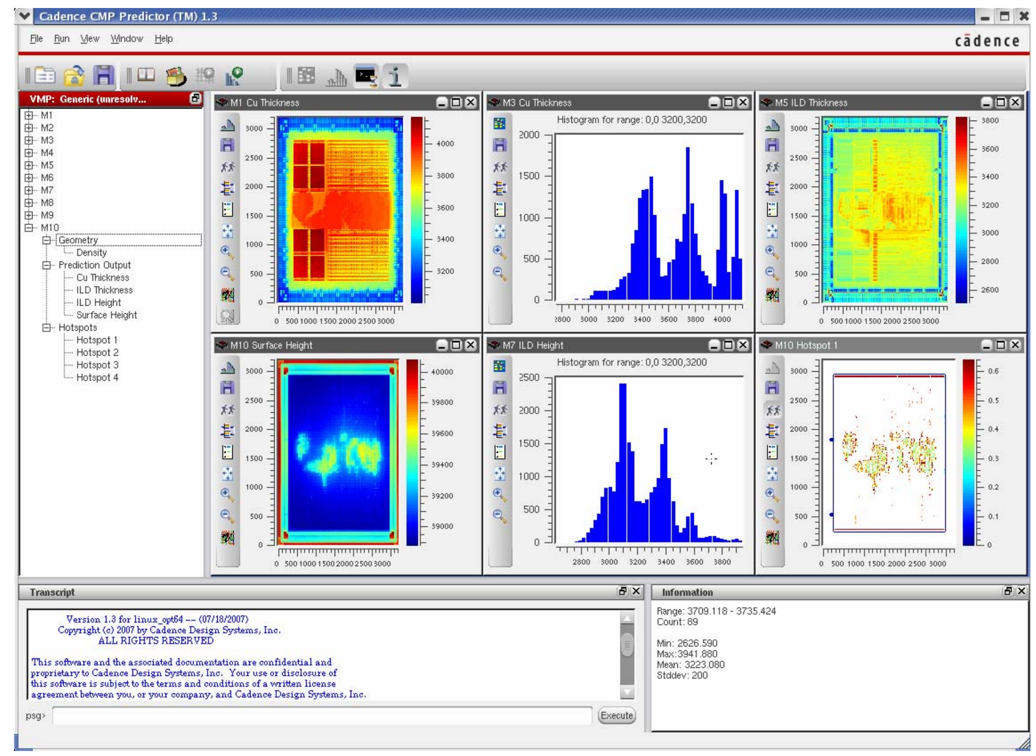
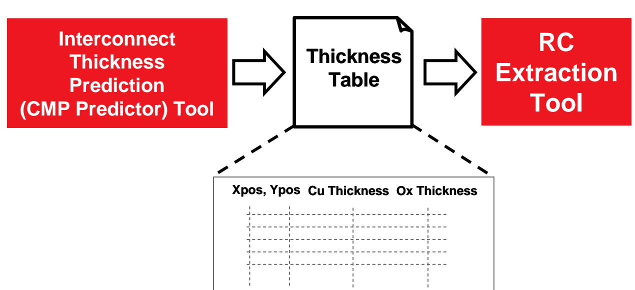
Cadence CMP Predictor

Features/Applications

- Full chip interconnect and dielectric thickness prediction
  - Multi-level
  - Long-range effects – neighboring die and scribe lines
- Robust Viewing and Analysis
  - Command line or point and click UI
  - Surface height, thickness, density,…
  - Topography plot and statistics
- Manufacturing Hotspot Checking
  - Hotspot checking – Foundry defined or customer defined
  - EDA methodology for design/dummy fill modifications
- RC Extraction Interfaces
  - EDA tools (RC extraction)
  - Generic thickness export file





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Cadence CMP Predictor - Applications

VMP Library

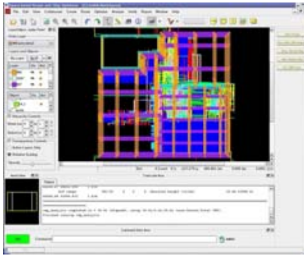
Foundry Process Characterization

Copper Loss [Angs]

Total Copper Loss (Angs)

Total Copper Loss [Angs]

Yield Hot Spots



Hotspot Fix

Dummy Fill Modification

Process Optimization

Virtual Manufacturing Prediction

RC Extraction

Nominal Thickness
Actual Thickness
Time (seconds)

Critical Net Performance

Chip Design

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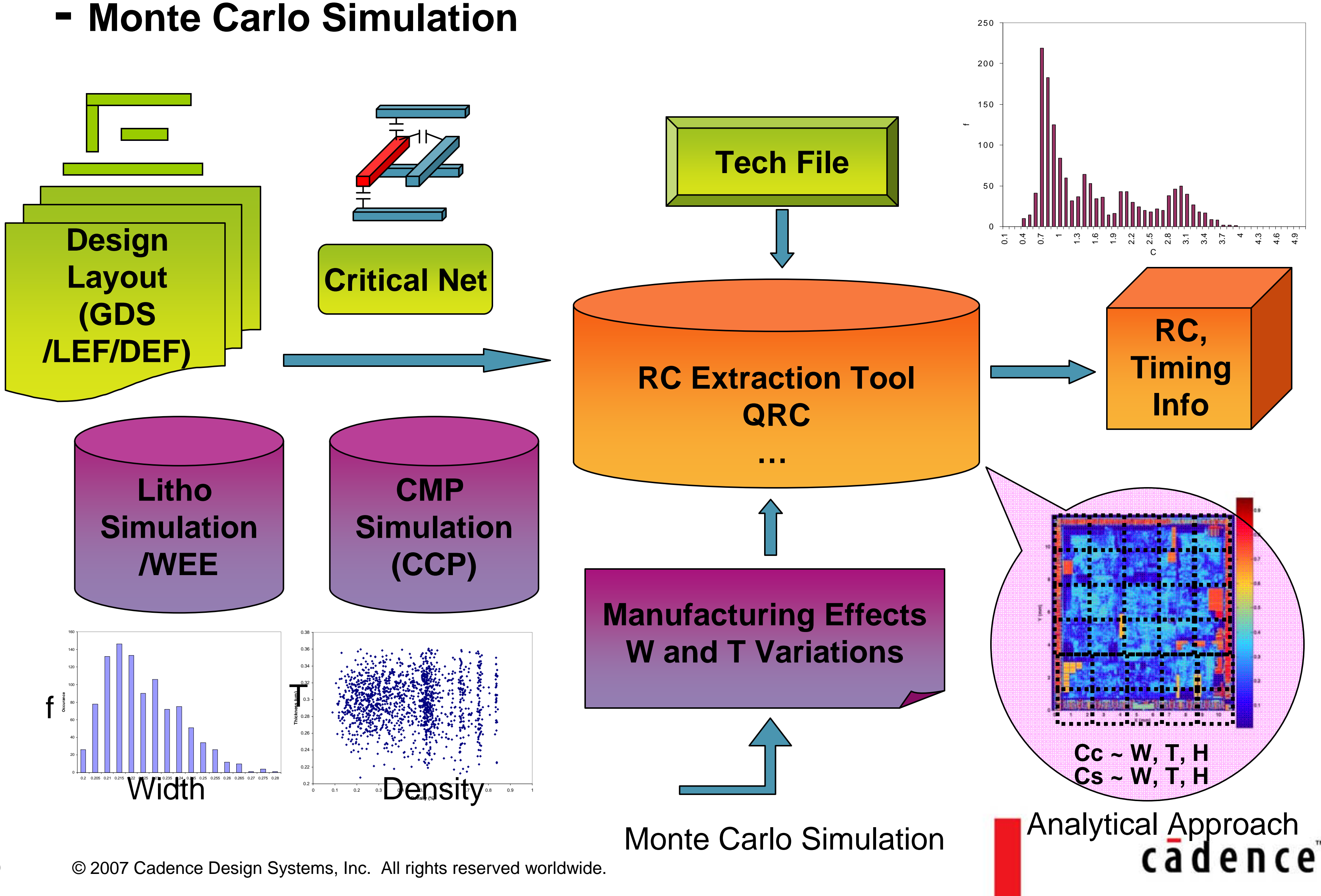
Variation Impact on RC

- Monte Carlo Simulation



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cadence

Thickness Impact on Capacitance

Length (um)

W (um)

0.12 0.22 0.42 1.02

Length (um)

S (um)

f

T (um)

0.15 0.2 0.25

-0.1 -0.08 -0.06 -0.04 -0.02 0 0.02 0.04 0.06 0.08 0.1

The impact of thickness variation (stdev = 5.6%) on C (stdev = 1.9%) is less compared to R (linear). However, variations as large as +/- 7% are observed and it may cause extraction errors for critical nets

Close form calculation. Ref: N.D. Arora, L. Song et al. IEEE Tran. Semiconductor Manufacturing, pp. 262-271, Vol. 18, No.2 May 2005

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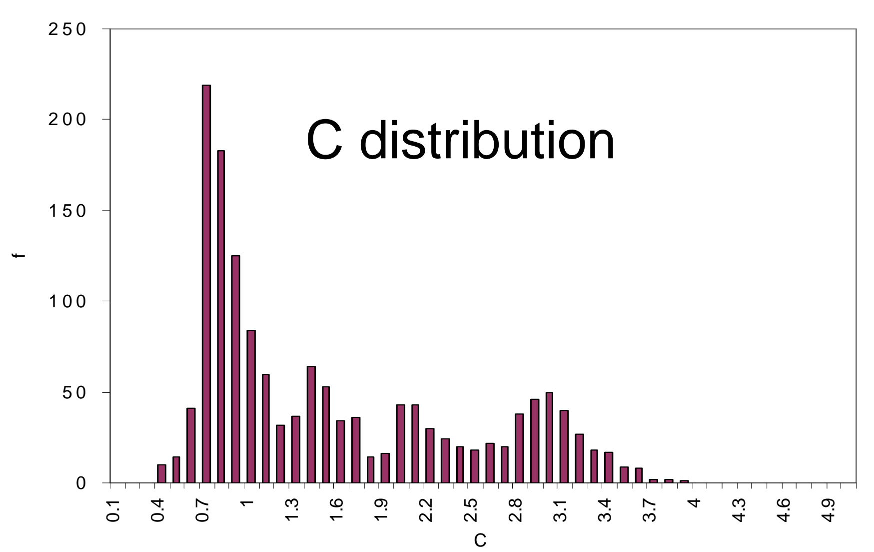
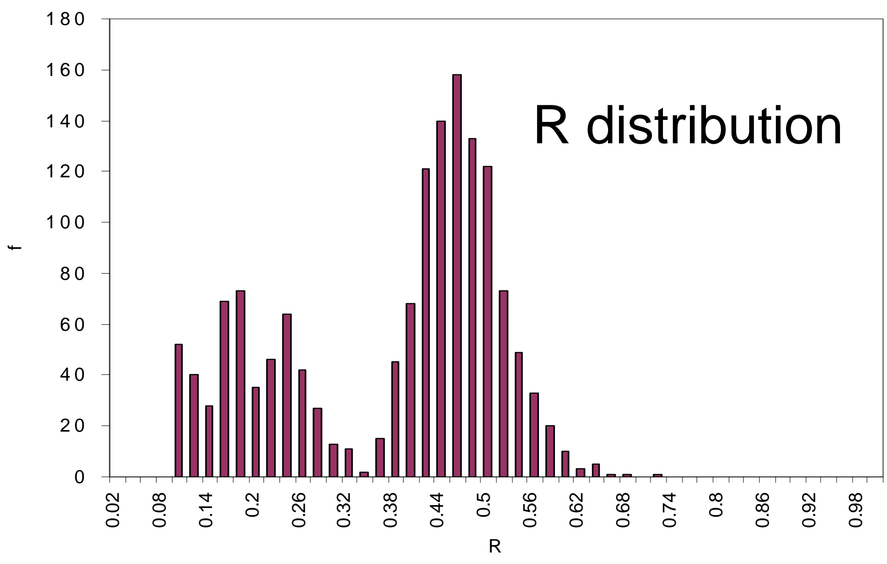
Thickness and Width Variation Impact on Timing





65/90nm	RC delay (ns)	RC Difference (ps)
Nominal	2.7546	0
W Variation[a]	2.6421	-112.5
T Variation[b]	2.8054	50.8
T+W Variation	2.6922	-62.4

a. W = 0.10um, Gaussian, StDev = 10%
b. T = 0.25um, Gaussian, StDev = 12%

Both self and coupling capacitance are included in timing calculation

Close form calculation. Ref: N.D. Arora, L. Song et al. IEEE Tran. Semiconductor Manufacturing, pp. 262-271, Vol. 18, No.2 May 2005

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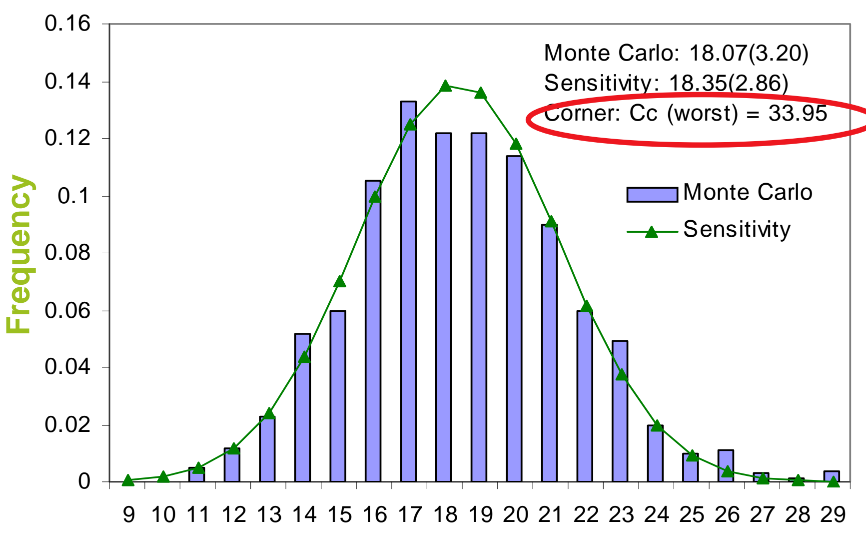
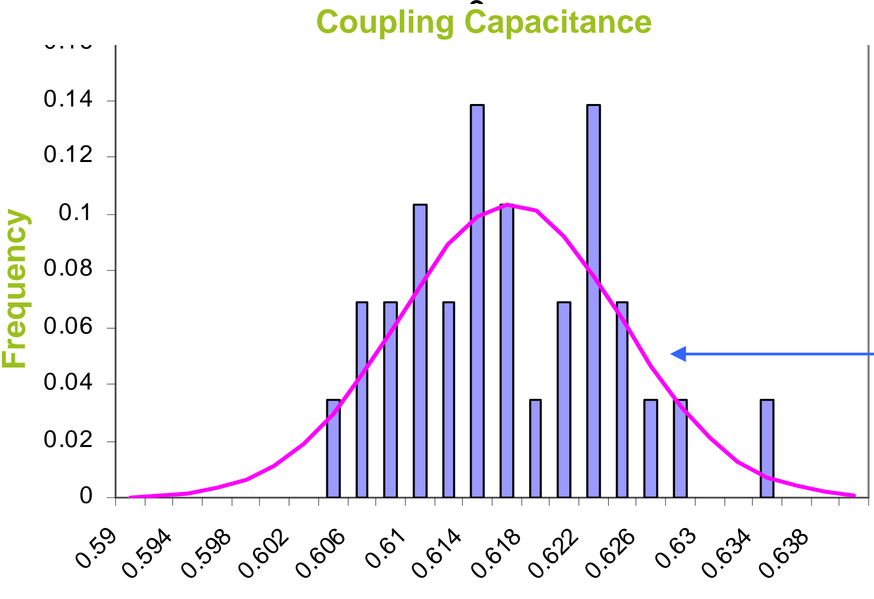
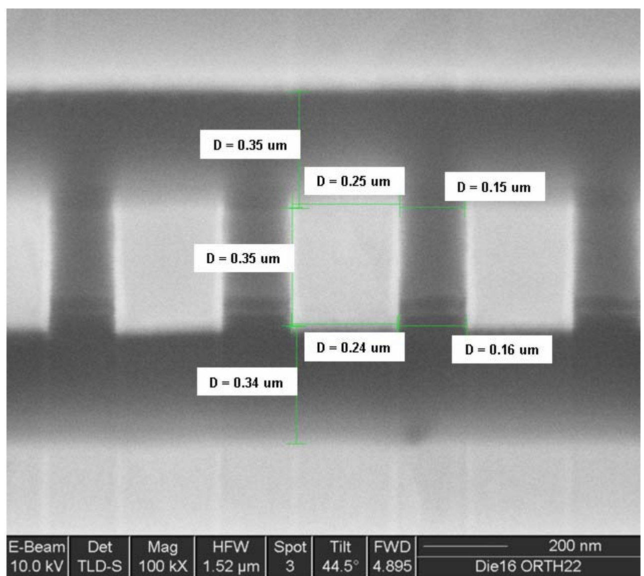
Corner Based Methodology





Worst Case analysis (corner) yields 26% higher worst coupling capacitance estimation



Measurement vs. Analysis

N.D. Arora, L. Song and A. Fujimura
US Patent 7089516

CCP And QRC Integration Flow

VMP

Design (GDS)

Layer map

Cadence CMP Predictor

Design

Erosion Data

Tech File

RC Extraction with Model-based Erosion Data

SPEF/ SSPEF

DSPF

Spice

BEGIN
METAL LEVEL N
X pos, Y pos, Cu Thickness, ,Oxide Thickness etc.
I j A A

No Density Rule Based Erosion Table

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Model-Based versus Rule-Based Approach: Comparison to Golden Data

Validated by TSMC!

nets (%) vs. Errors Compared to Golden Data (%) — legend: Erosion Table, CMP Model

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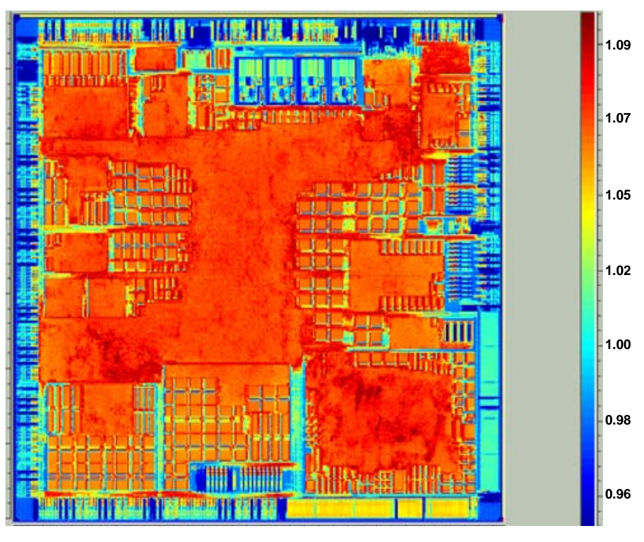
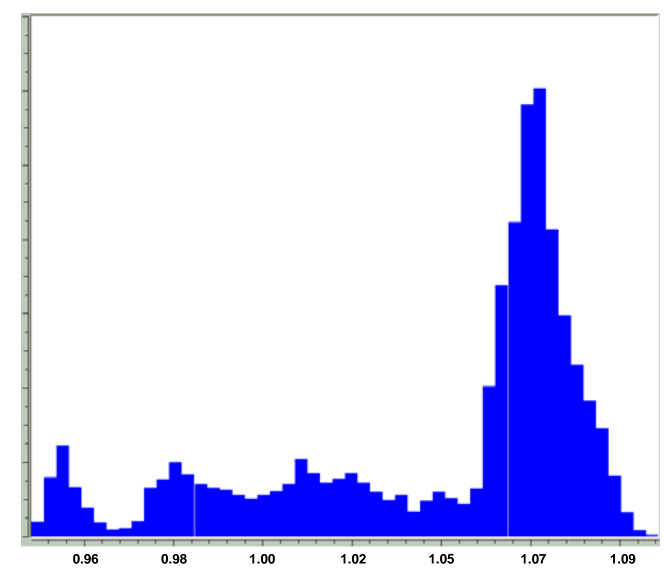
RC Extraction Results – CMP Model vs. Rule

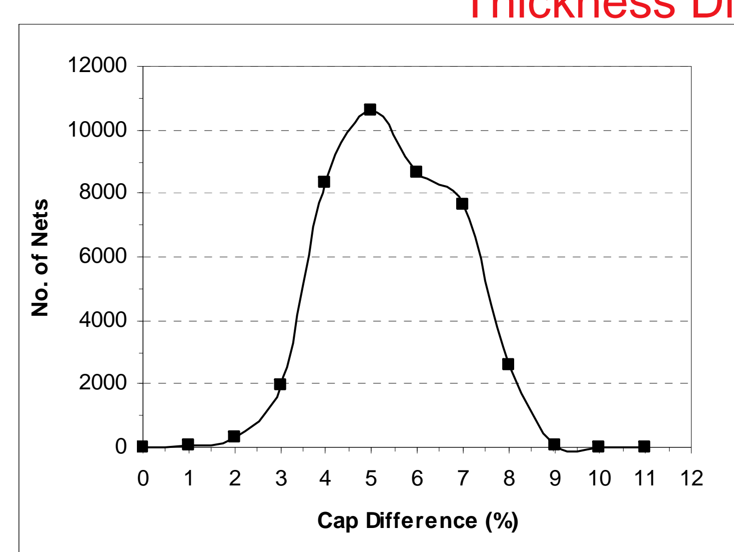


Thickness Variation



Thickness Distribution

Long range and multi-level CMP effects are difficult to capture using rules



Capacitance Variation

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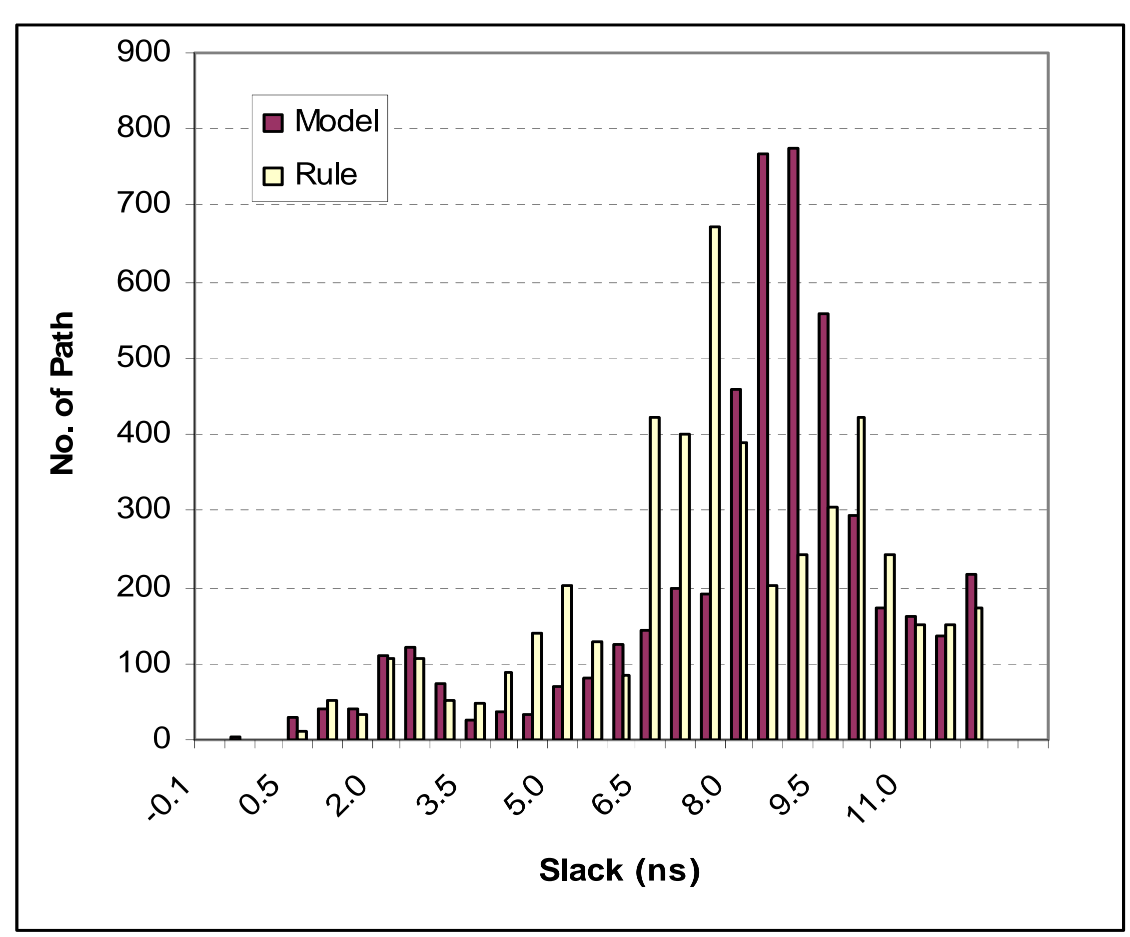
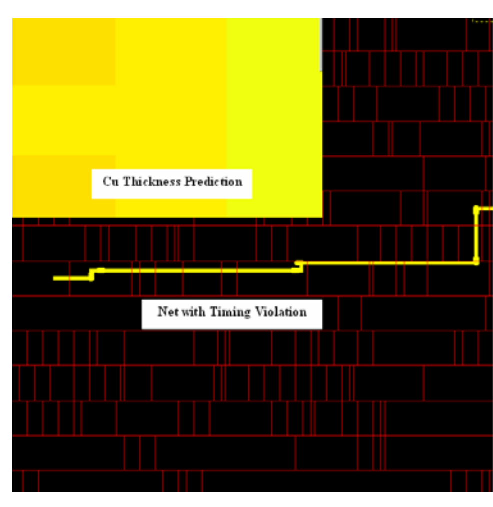
Timing Results – CMP Model vs. Rule





	Setup		Hold	
	Rule	Model	Rule	Model
Path1	OK	46 ps worse		
Path2	OK	56 ps worse		
Path3			OK	OK
Path4			OK	OK

Timing slacks are different using model based approach, possible over/under designs

Timing Difference

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Summary

- The incorporation of CMP model into RC extraction flow of 65nm designs is demonstrated
- Capacitance values extracted using the model based approach is different than those obtained through a rule based approach
- The distribution of timing slacks is also different, in addition, new setup timing violations were observed using the CMP model
- There are potential over or under designs when using rule based approach, model based approach should yield more accurate results

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