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# Cadence Certus Closure Solution

## Delivering overnight concurrent full-chip optimization and signoff

The Cadence® Certus™ Closure Solution is the industry's first fully automated and massively distributed environment for full-chip optimization, fully physical aware, and signoff. It delivers up to 10X concurrent chip-level optimization and signoff with overnight results. It supports the high-capacity requirements of modern designs that consist of multiple subsystems and can handle unlimited-capacity device instances. The Cadence Certus solution employs a massively parallel architecture to support fully automated and distributed hierarchical optimization and signoff closure at a full-chip level. This massively distributed computing ability provides simultaneous full-chip optimization, with implementation in the Innovus™ Implementation System, metal fill in the Pegasus™ Physical Verification System, parasitic extraction in the Quantus™ Extraction Solution, and full static timing analysis in the Tempus™ Timing Signoff Solution. Now, engineering teams can achieve a better design experience starting from block-level to full-chip and subsystem optimization and signoff closure with Tempus ECO, Tempus Timing Solution, and the Cadence Certus solution—all without leaving the Innovus Implementation System environment. This is a unique in-design capability to reduce time-to-market while providing the best-in-class PPA. Furthermore, the Cadence Certus solution is cloud-ready and supports internal cloud and data centers.

## Overview

The Cadence Certus solution eases high capacity design signoff closure bottlenecks and complexities that come with developing today's emerging applications such as hyperscale computing, 5G communications, mobile, automotive, and networking. Prior to the introduction of the Cadence Certus Closure Solution, a full-chip closure flow involved ad-hoc, manual, and tedious processes from full chip assembly, that is, error prone, static timing analysis and ECO optimization and signoff with 100s of views, taking designers months to converge. The new Cadence solution leverages the Concurrent Multi-Mode Multi-Corner (CMMMC) and Parallel Distributed Interactive MMMC (Paradime) technologies of the Tempus Timing Solution to deliver a fully-automated flow and massively distributed for superior optimization and signoff, allowing concurrent, full-chip optimization through shared engines in the Innovus Implementation System and the Tempus Timing Solution, which eliminates iterative loops with block owners and lets designers make quick optimization and signoff decisions. Furthermore, it uses the Tempus Timing Solution SmartMMMC Optimization capability to reduce the increasing number of signoff views, without any limitation, reducing the turnaround time and memory by up to 4X.

Furthermore, using its scalable architecture allows highly distributed and simultaneous signoff closure flow for 3D-IC designs of multi-million-instance dies from the same or different process nodes and inter-die paths in the tightly integrated Integrity™ 3D-IC Solution.

## Key Features and Benefits

- 10X Productivity
  - Overnight concurrent timing optimization and signoff
- Better PPA
  - Delivers fastest path towards maximum power recovery previously untapped due to design closure timeline pressures
  - Delivers 10%-15% inter-partition and up to 5% full chip power recovery
- Empowered Collaboration
  - Eliminates iterative loops with multiple block owners with rapid decision making for optimization and signoff
- Better User Experience
  - Automation enables users to increase their productivity
- Compute resources shared with distribution optimization and signoff closure with smaller machines and the lowest peak memory requirements

## Distributed Processing and Multi-Threading

Every Cadence Certus timing job is naturally multi-threaded for faster execution on minimum CPUs and memory configurations. Furthermore, the Cadence Certus solution has the unique capability to distribute optimization jobs across multiple separate machines that each take advantage of multi-threading in their own minimum memory space. This delivers overnight optimization and signoff design closure while reducing the memory requirements for each machine.

## OS Platform Support

Cadence Certus Closure Solution supports:

- RHEL 6.5+, 7.4+, 8
- CentOS 6.5+, 7.4+, 8

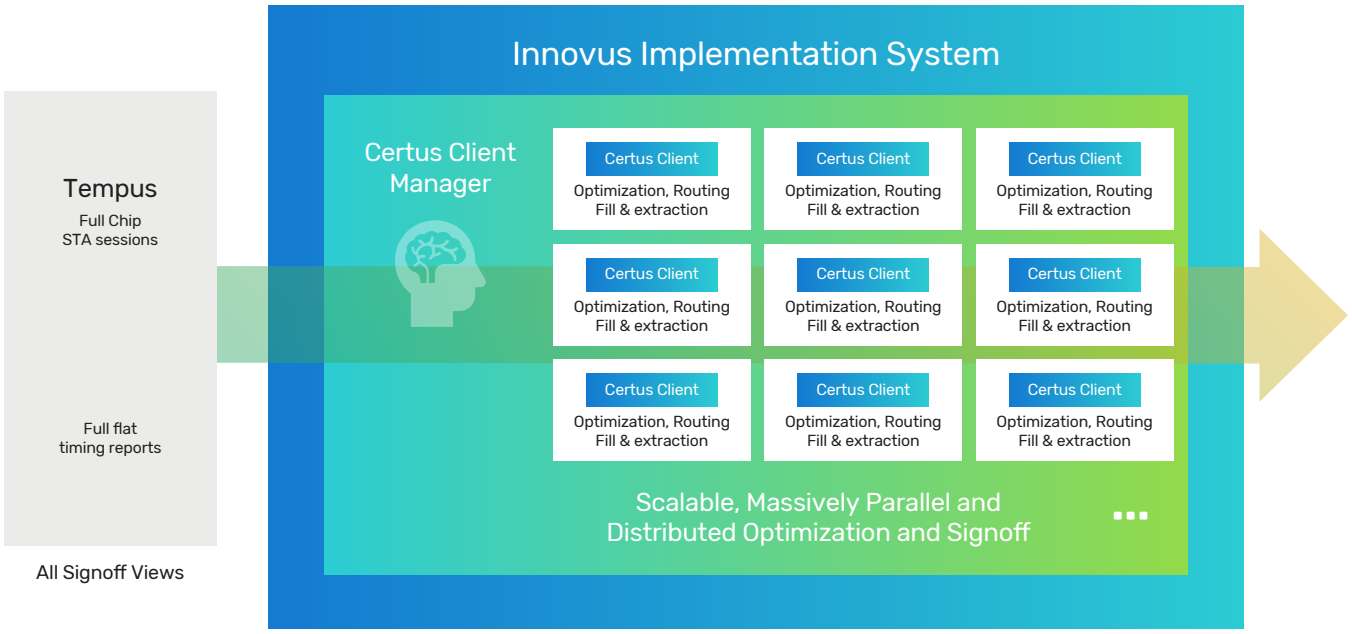


*Figure 1: Fully Automated and Massively Distributed Flow for Signoff Closure*

## Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training.
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- More than 25 Internet Learning Series (ILS) online courses allow you the flexibility of training at your own computer over the Internet.
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more.
- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training.

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