METHODOLOGY FOR ANALYZING AND QUANTIFYING DESIGN STYLE CHANGES AND COMPLEXITY USING TOPOLOGICAL PATTERNS

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OUTLINE

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TOPOLOGICAL PATTERN DESCRIPTION

LAYOUT PATTERN EXTRACTION

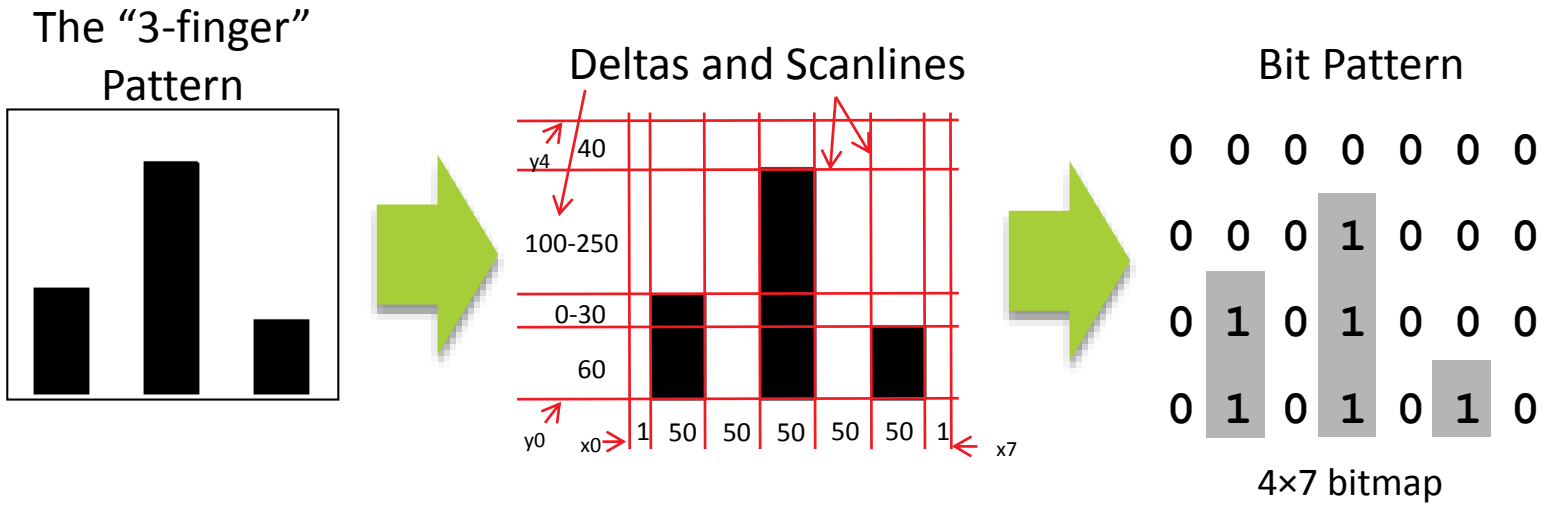
TOPOLOGICAL LAYOUT COMPARISON

SUMMARY

INTRODUCTION

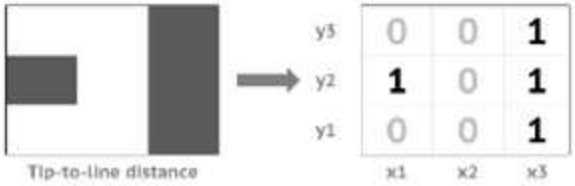
- Pattern matching engines have been available in the IC physical design ecosystem for over a decade.
- The use of pattern matching to augment design-rule checking (DRC) in the physical verification flow has been widely adopted.
- Early pattern matching engines used a three-value logic (TVL) method for describing patterns.
- The more recent introduction of topological-based pattern matching engines has opened a range of new applications for layout analysis.

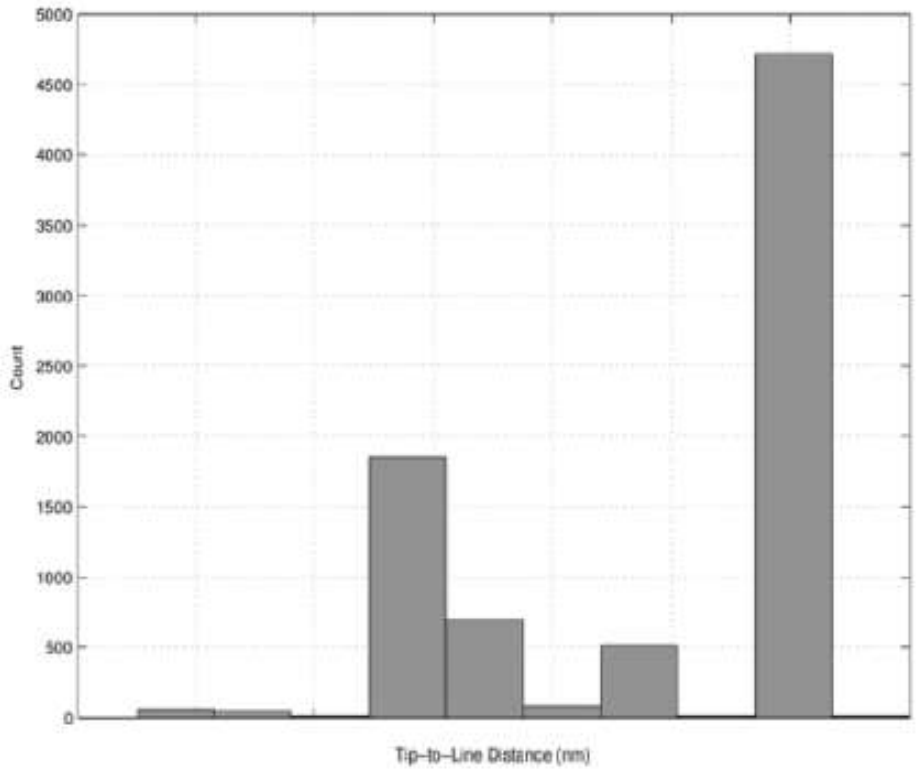
TOPOLOGICAL PATTERN DESCRIPTION



- A powerful tool for characterizing and comparing physical designs
- Compact form for describing patterns
- Can be independent of physical dimensions

TOPOLOGICAL PATTERNS CAN BE USED FOR ANALYSIS





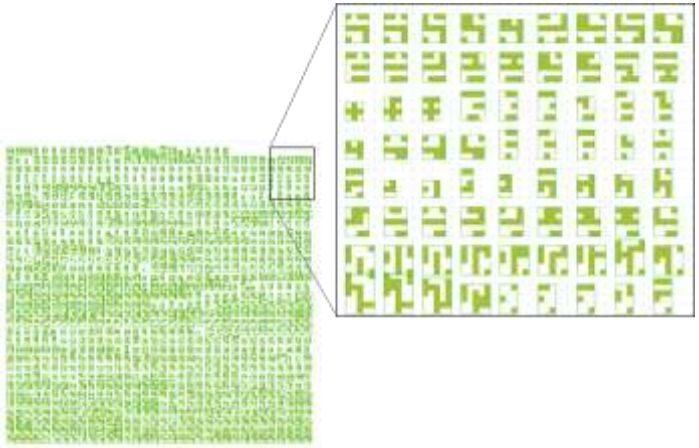
1. Understand usage of patterns in your designs (with locations)
2. Identify common cases (which must yield well) and outliers/edge cases
3. **Identify what is new/different in an incoming design**

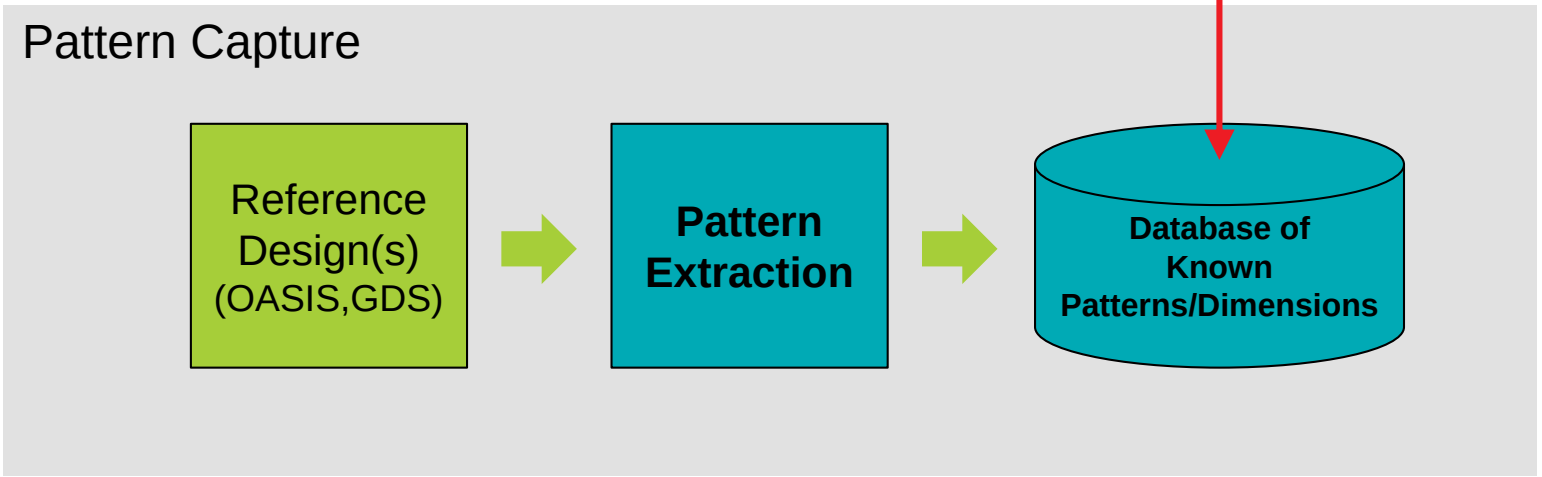
LAYOUT PATTERN EXTRACTION

1. Systematically scan a window across entire design (choice of window size is important!)

2. In every window, break-down and identify every pattern and sub-pattern that exists in that design (with dimensions)

3. Store a full catalog of all patterns with dimensions

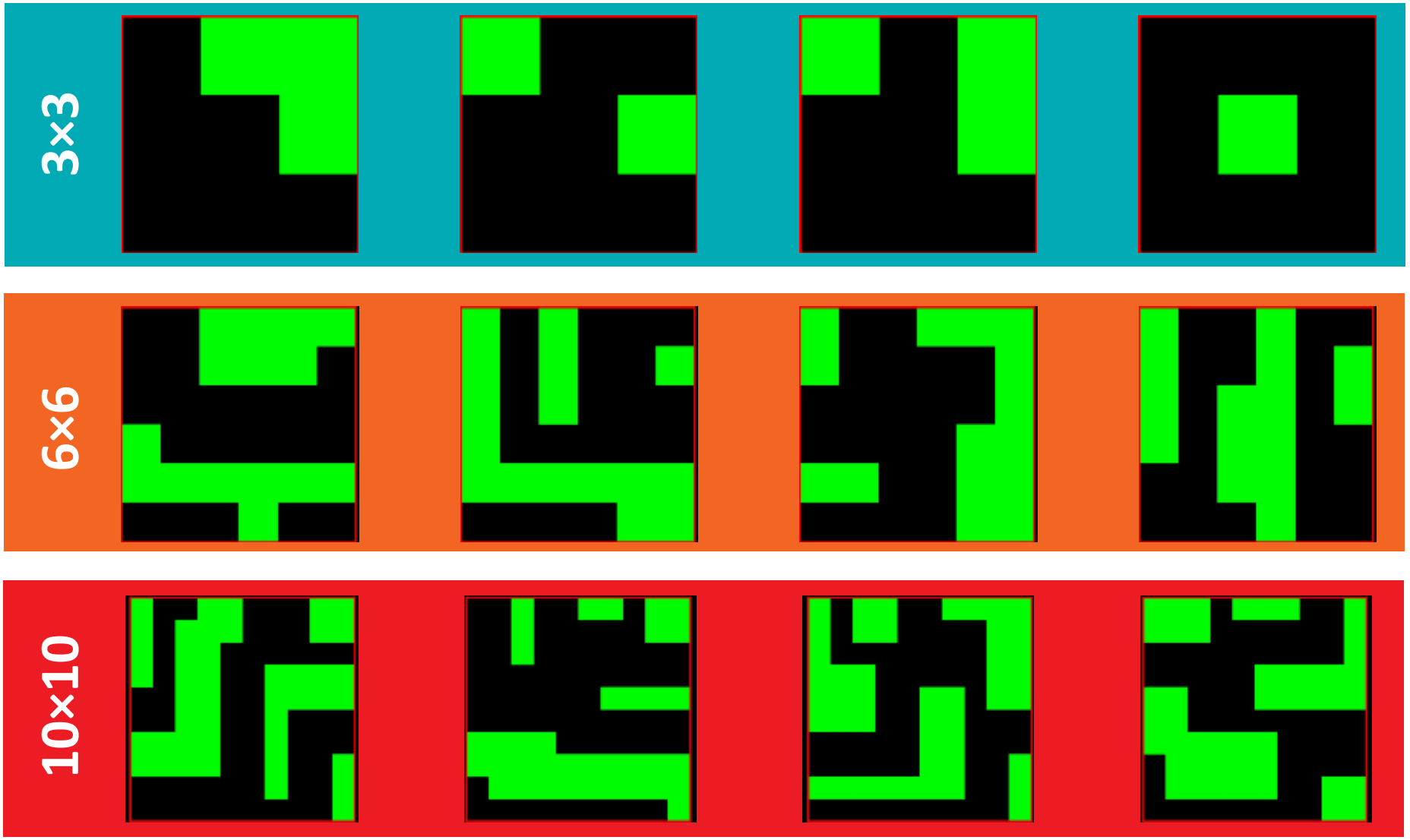




- In our experiments, full chip 1X Metal layers captured in < 8 hours w/ 32 CPUs

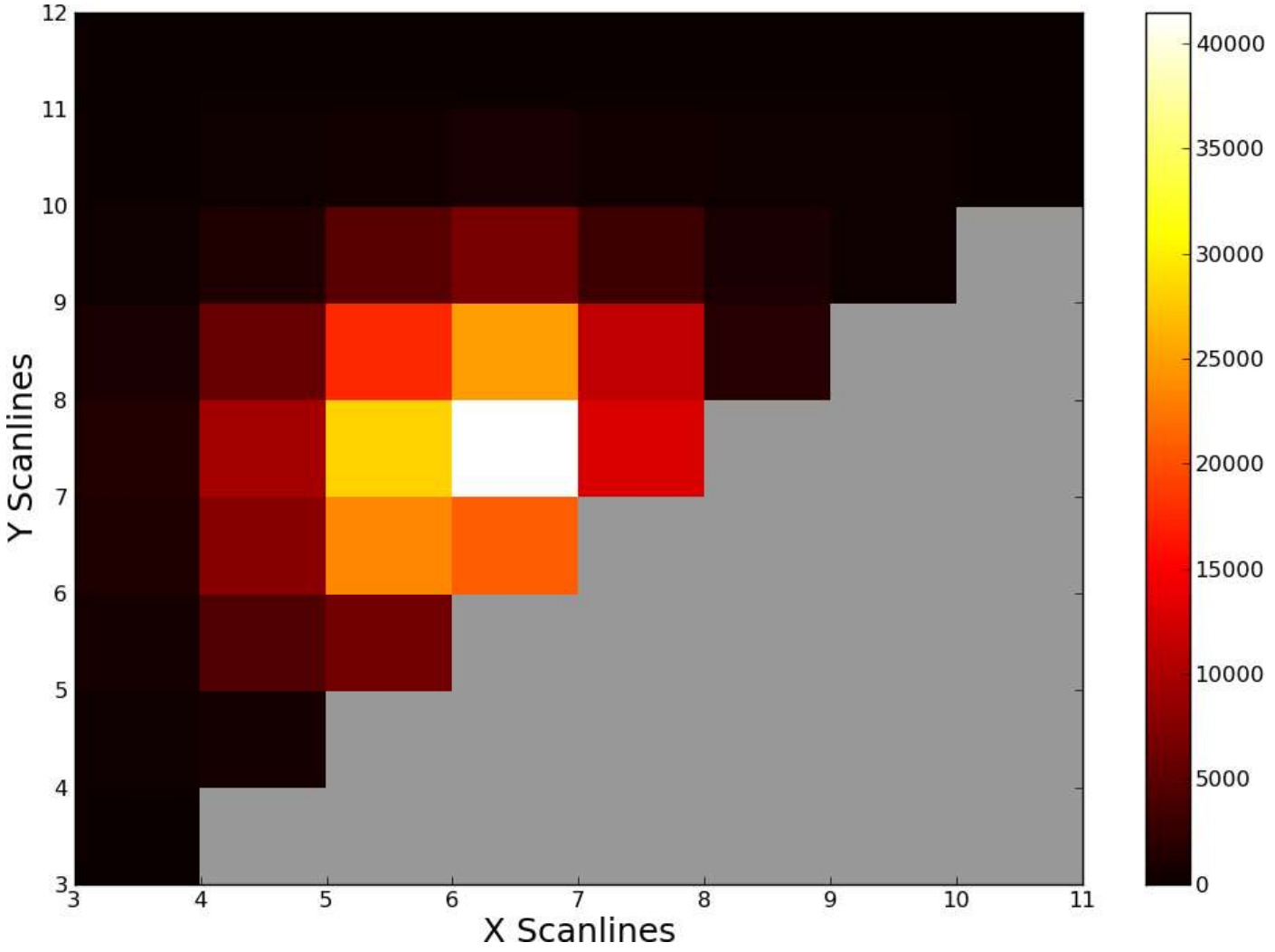
TOPOLOGICAL PATTERN EXAMPLES FOR MX LAYERS

14NM DIGITAL LOGIC – WINDOW SIZE = 3 METAL PITCHES



PATTERN EXTRACTION FOR 14NM DIGITAL LOGIC

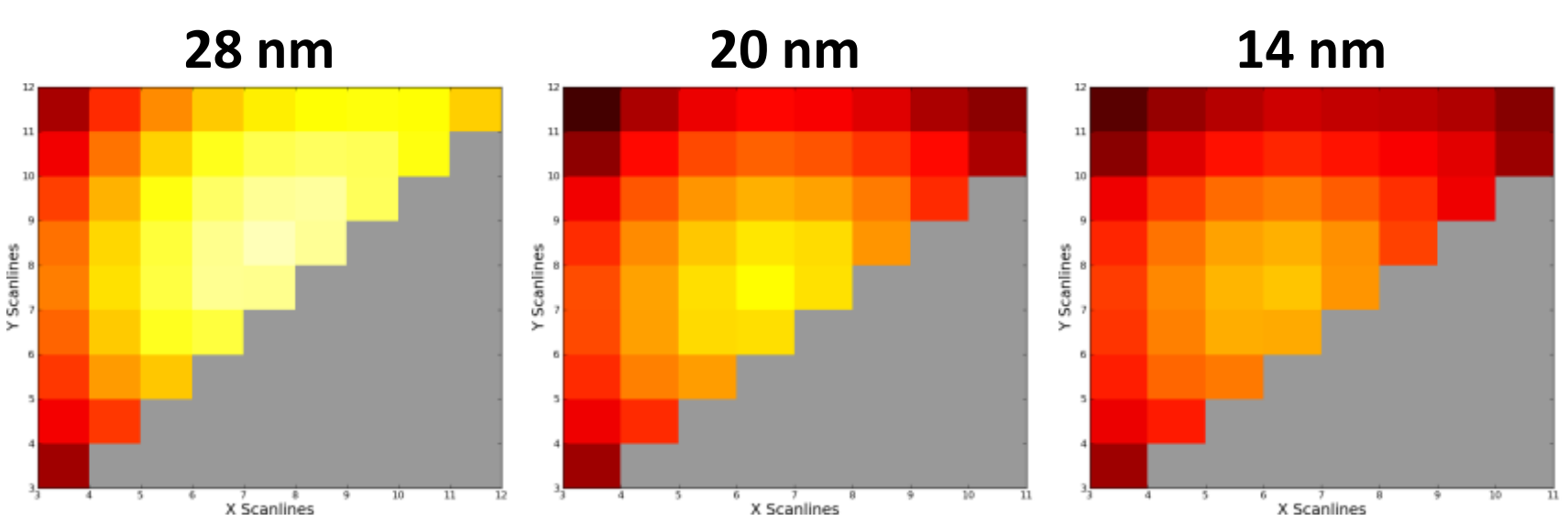
1X METAL LAYERS, WINDOW SIZE = 3 METAL PITCHES, INEXACT MATCHES



EVOLUTION OF DESIGN TOPOLOGICAL COMPLEXITY

1X METAL LAYERS, WINDOW = 3 METAL PITCHES, INEXACT MATCHES

28 nm **20 nm** **14 nm**

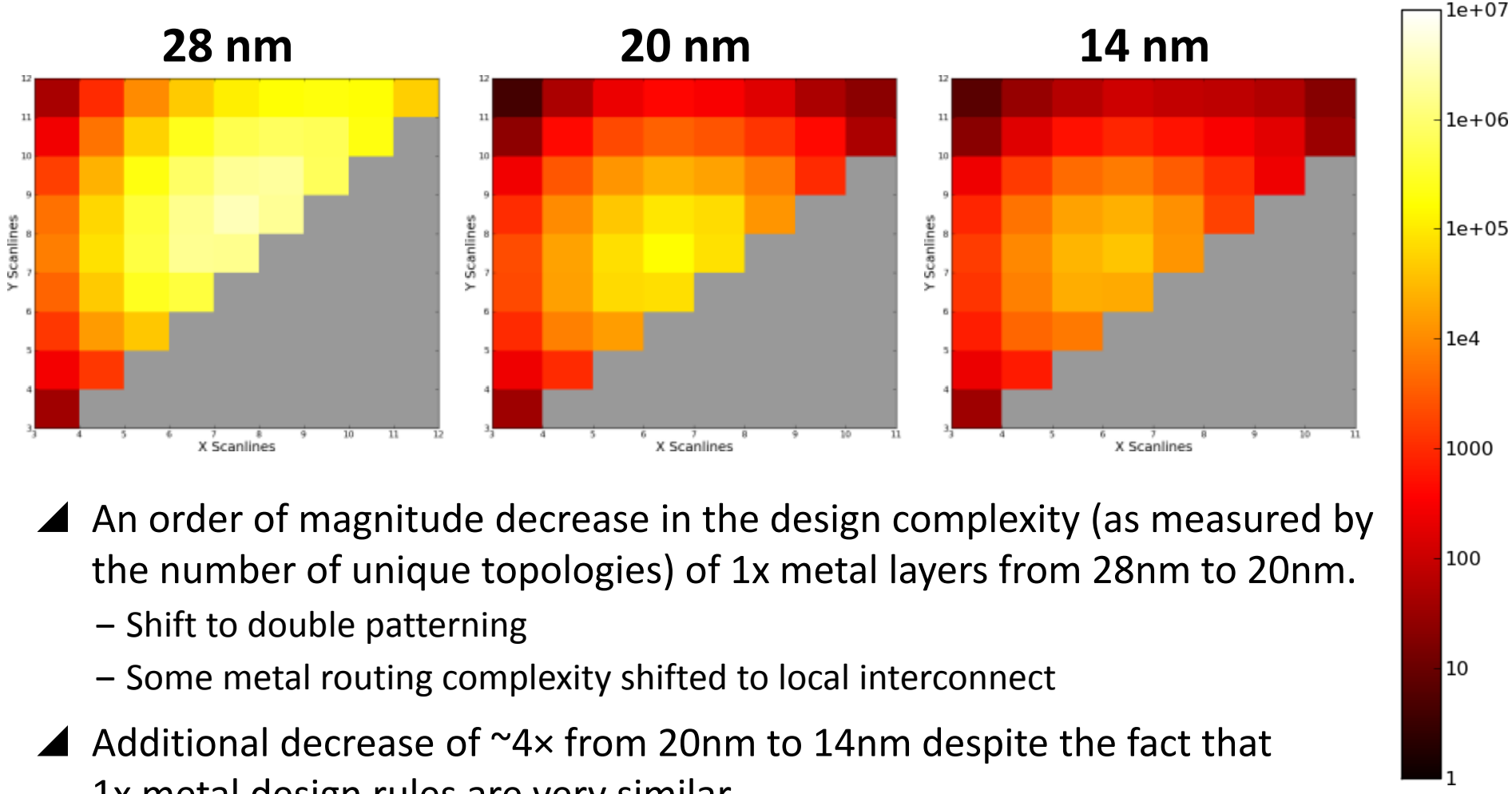


- The same circuit was implemented in 28, 20, and 14 nm technologies.
- Pattern extraction was run on each and the number of unique topologies was counted.
- Note the use of a log scale.

Technology Node	Total Unique Patterns
28 nm	20,718,038
20 nm	835,017
14 nm	242,617

EVOLUTION OF DESIGN TOPOLOGICAL COMPLEXITY

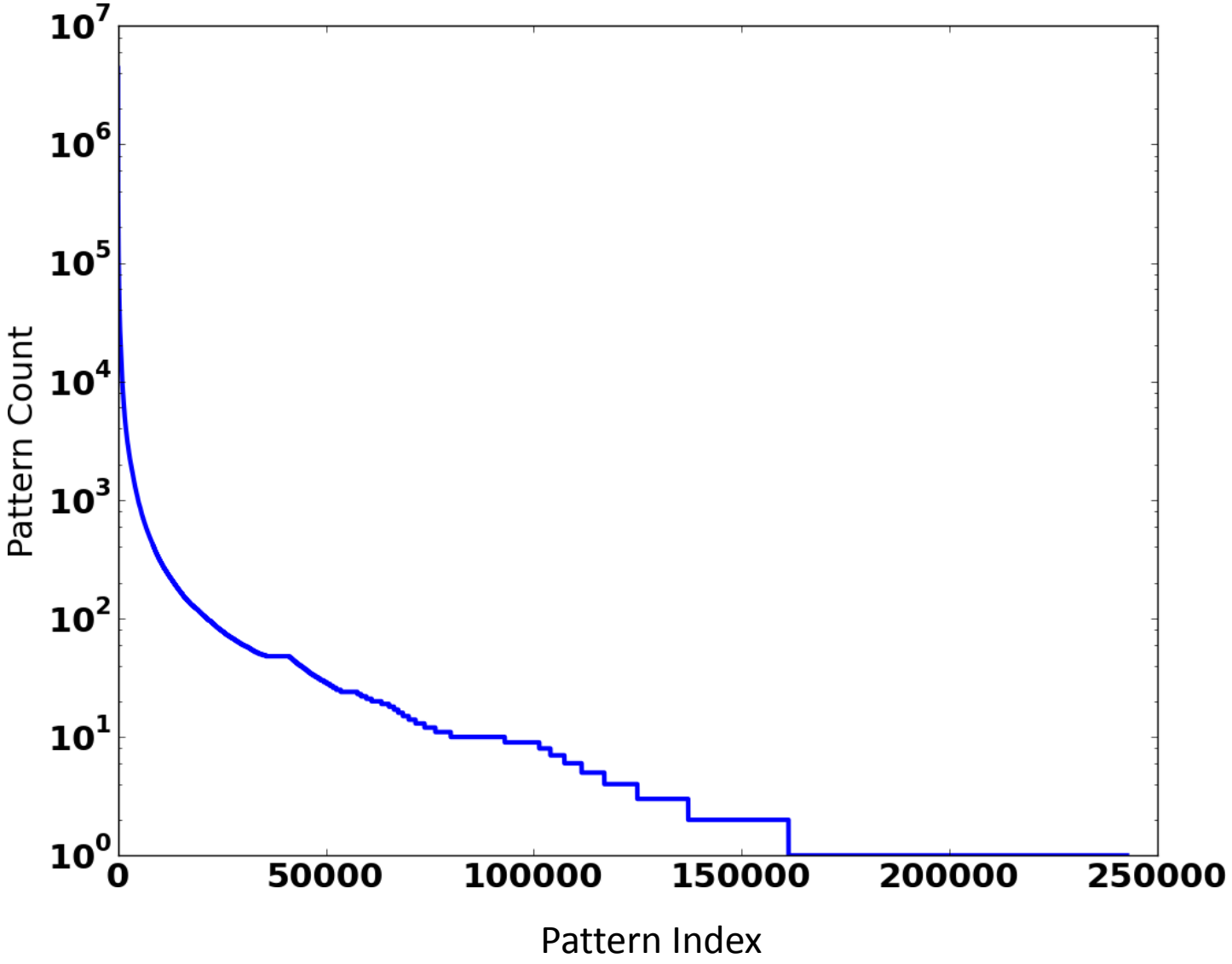
1X METAL LAYERS, WINDOW = 3 METAL PITCHES, INEXACT MATCHES



- An order of magnitude decrease in the design complexity (as measured by the number of unique topologies) of 1x metal layers from 28nm to 20nm.
  - Shift to double patterning
  - Some metal routing complexity shifted to local interconnect
- Additional decrease of ~4× from 20nm to 14nm despite the fact that 1x metal design rules are very similar.
  - Shift to FinFET devices and impact of increased regularity of front end

DISTRIBUTION OF TOPOLOGY COUNTS

14NM DIGITAL BLOCK, 1X METAL LAYERS



PATTERN SPACE SIZE

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X	Y	Total Possible	Reduced Space*
3	3	512	38 (7%)
3	4	4,096	299 (7%)
3	5	32,768	1,716 (5%)
3	6	262,144	9,044 (3%)
3	7	2,097,152	49,610 (2%)
3	8	16,777,216	267,390 (2%)
3	9	134,217,728	1,452,652 (1%)
3	10	1,073,741,824	7,864,304 (1%)
4	4	65,536	1,900 (3%)
4	5	1,048,576	43,428 (4%)
4	6	16,777,216	479,491 (3%)
4	7	268,435,456	5,202,792 (2%)
5	5	33,554,432	500,948 (1%)

- The number of possible patterns in each topological family grows very rapidly with topological complexity.

*Reduced space removes duplicates due to rotation or mirroring and non-physical patterns.

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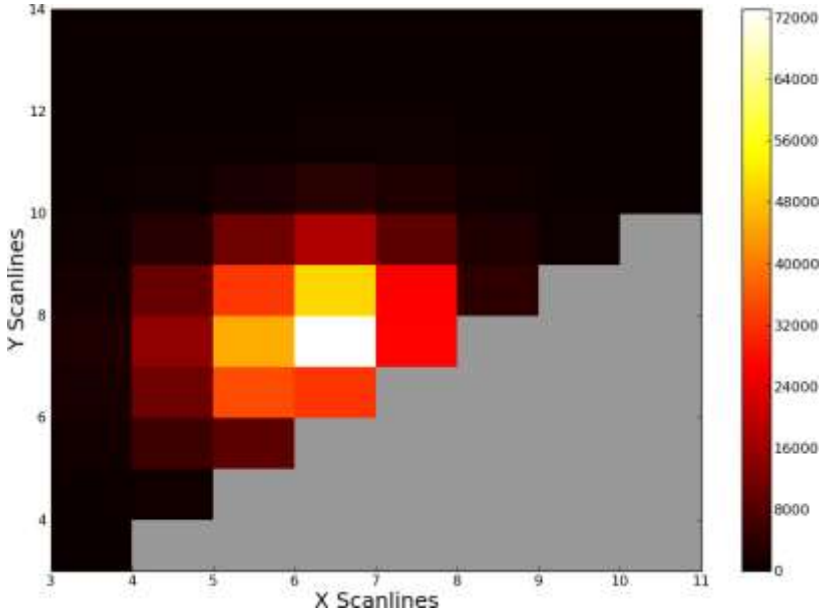
PATTERN SPACE COVERAGE

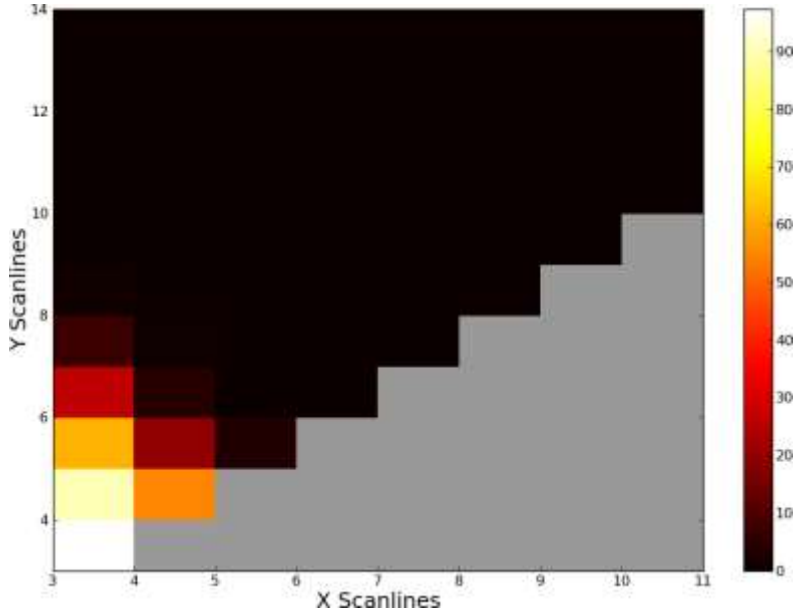
1X METAL LAYERS, WINDOW = 3 METAL PITCHES, EXACT MATCHES

14nm APU (CPU + GPU + Northbridge etc.) product design

Pattern Counts

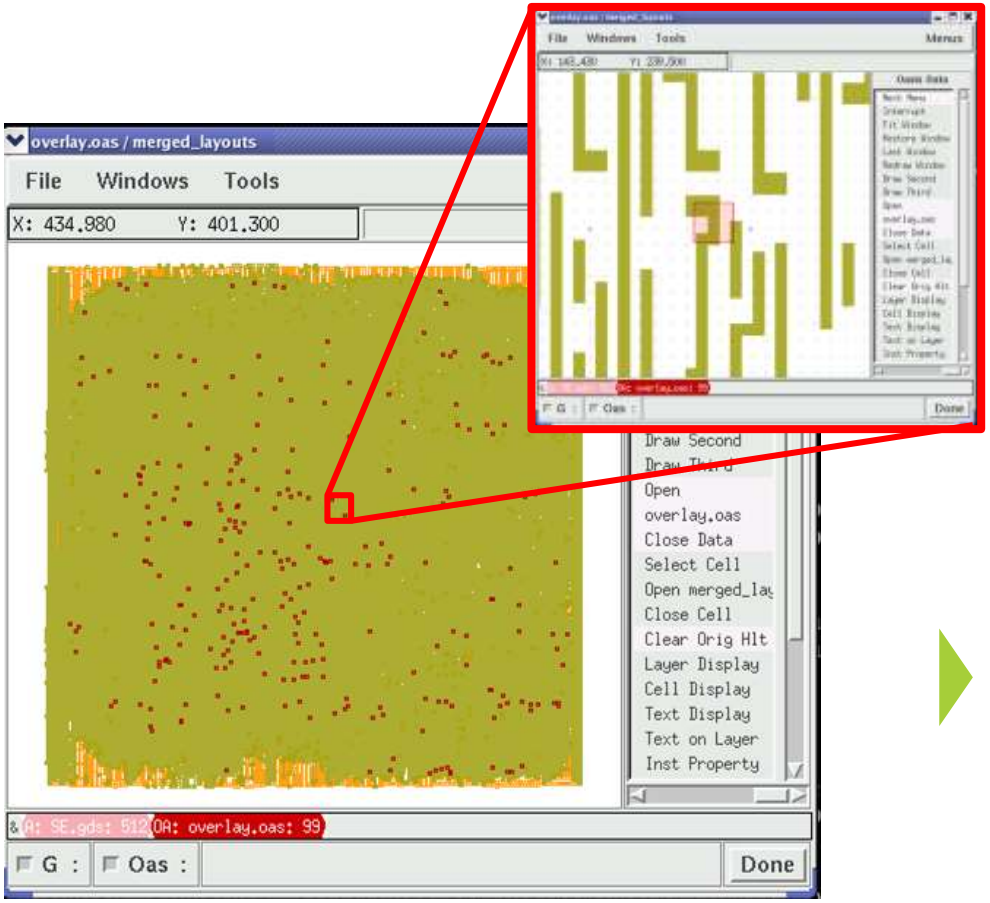


Pattern Space Coverage [%]



- Despite the highest raw count of unique patterns occurring for pattern topologies in the 6×7 family the coverage of the total pattern space is quite low in that region.
- Pattern coverage near 100% for basic topologies (3×3) but drops off quickly.

IDENTIFICATION OF LAYOUT DIFFERENCES



Use cases

1. Identify regions where customer has modified sensitive IP
2. Give OPC engineers regions that need more analysis
3. Feed forward monitoring points to process teams and FA
4. Give entire team an indication of how difficult a new tape-out will be, especially ramping up a new process

How do we define what is "new"?

1. **Topologically Different:** Patterns that have never been seen before
2. **Dimensionally Different:** Patterns whose dimensions are outside the range of what has been seen before

HOW CAN WE IDENTIFY WHAT IS "NEW" IN AN INCOMING DESIGN THAT WE HAVE NEVER SEEN BEFORE?

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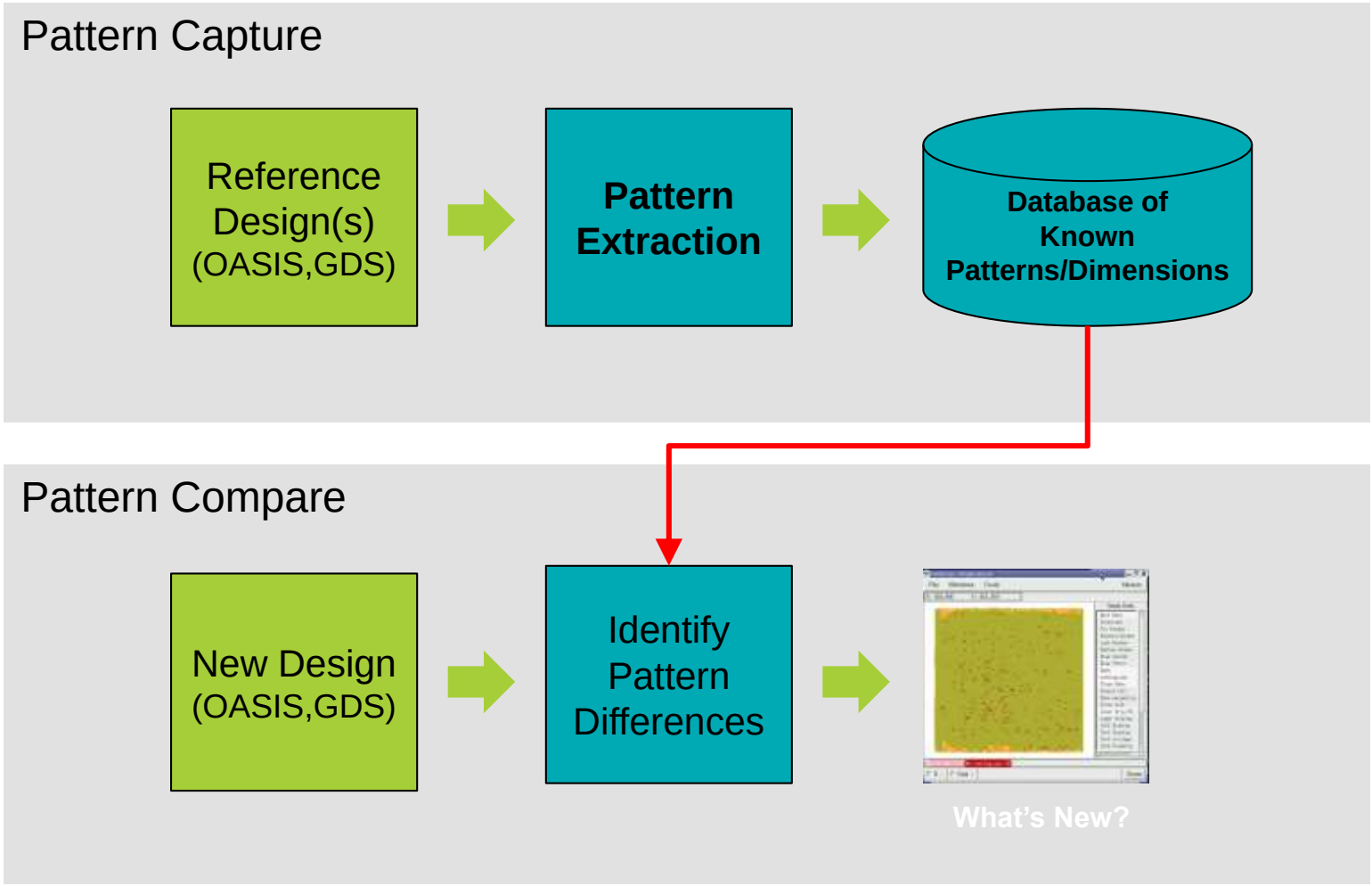

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AUTOMATIC IDENTIFICATION OF REPRESENTATIVE LAYOUT DIFFERENCES

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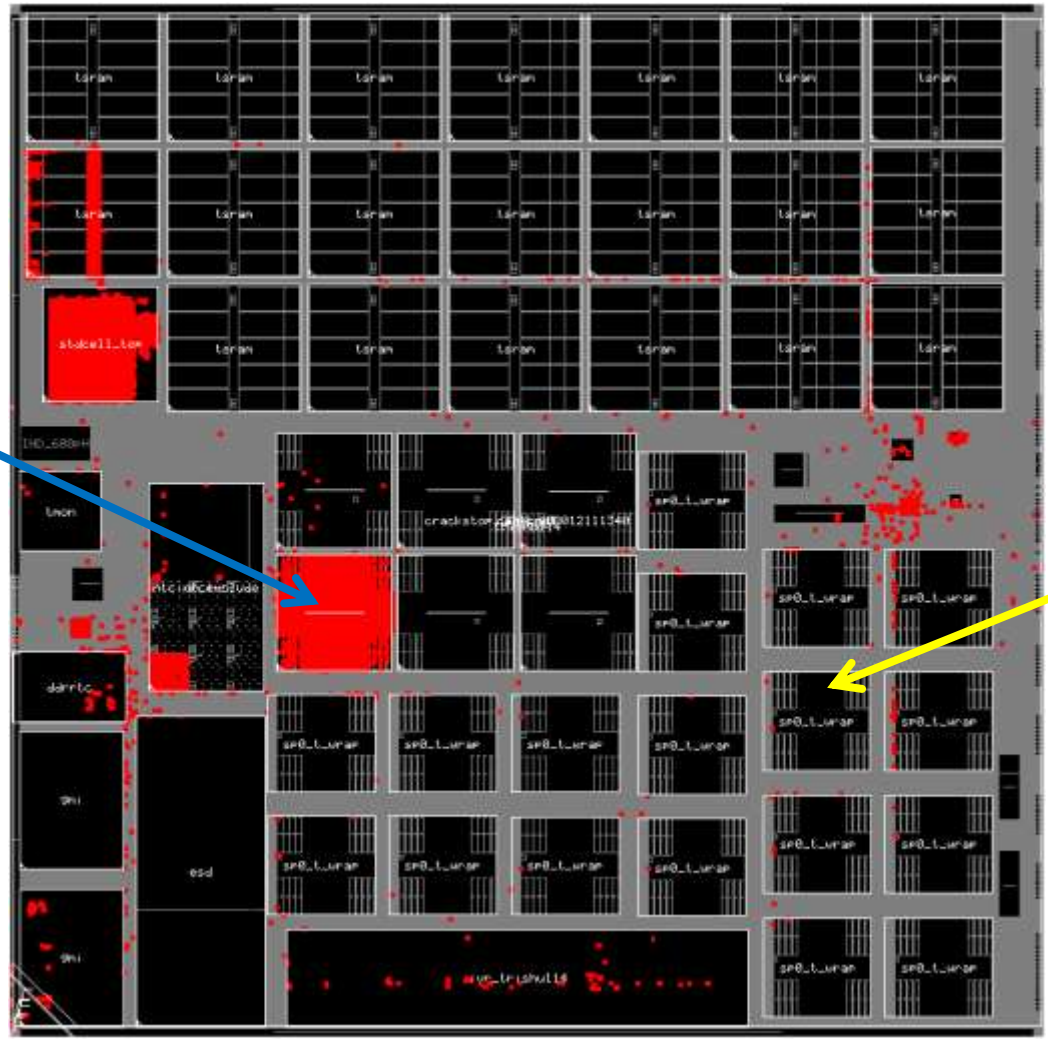
Each red point is a representative pattern present only in new design



Pattern extraction target (digital block)

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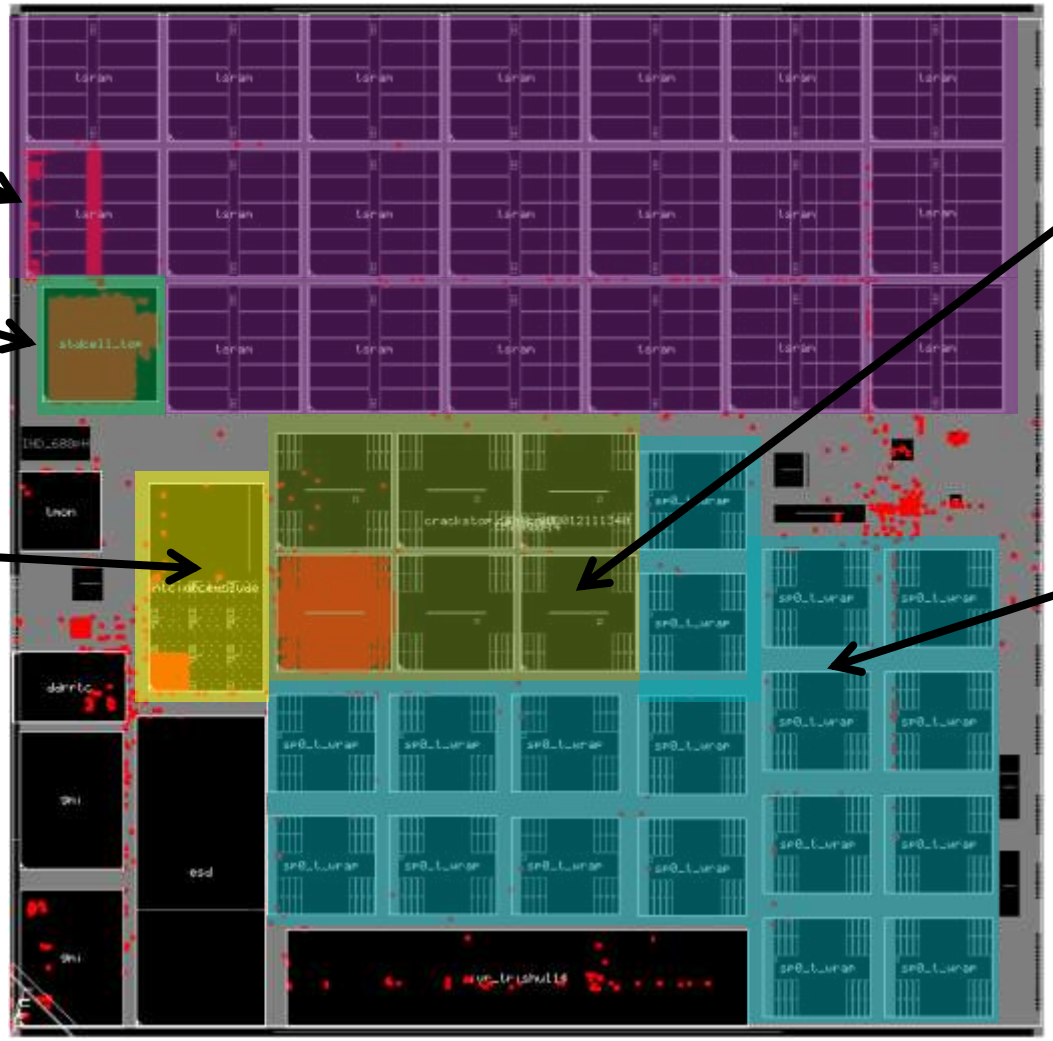
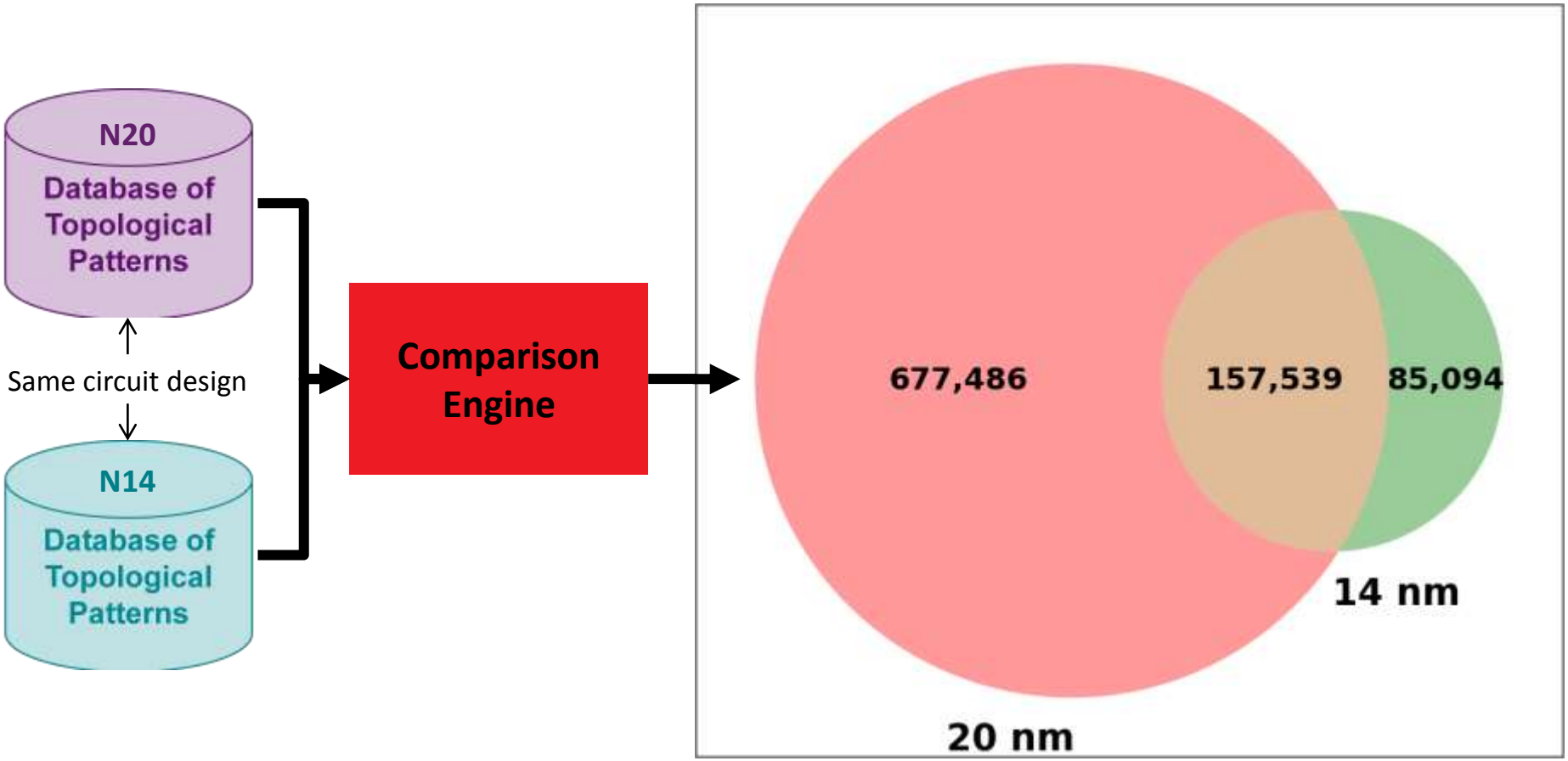
AUTOMATIC IDENTIFICATION OF REPRESENTATIVE LAYOUT DIFFERENCES



TOPOLOGICAL DESIGN COMPARISON

1X METAL LAYERS, WINDOW SIZE = 3 METAL PITCHES, INEXACT MATCHES



COMPARISON OF TEST CHIP TO PRODUCT TOPOLOGIES

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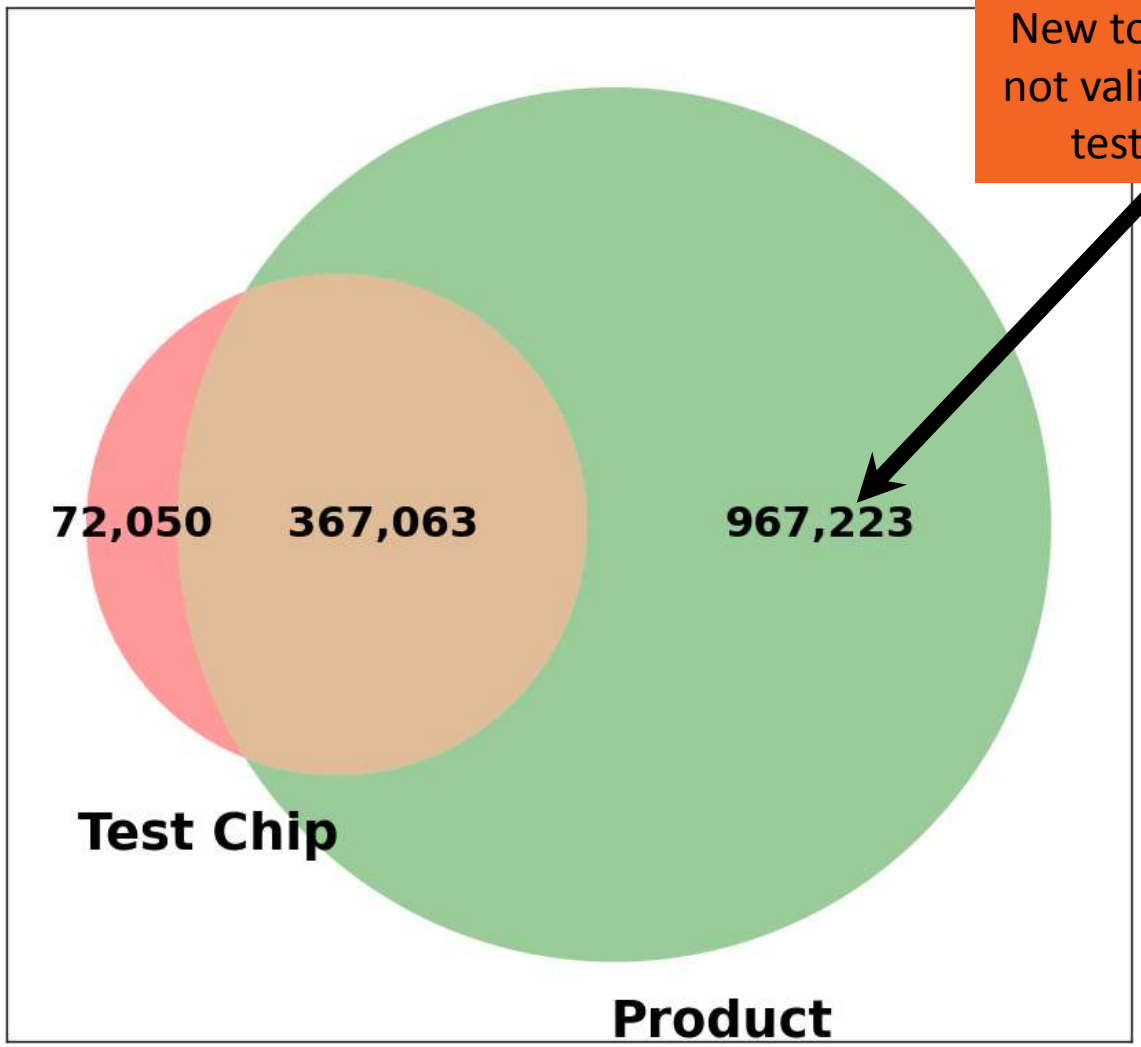
1X METAL LAYERS, WINDOW SIZE = 3 METAL PITCHES, INEXACT MATCHES



Pattern matching results can drive actions to mitigate risk

- For patterns used frequently, notify the fab for monitoring and/or process optimization.
- For infrequent patterns, consider removing from the design.

- Once patterns captured, comparisons performed in < 1 hour

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COMPARISON OF PRODUCT DESIGN STYLES

1X METAL LAYERS, WINDOW SIZE = 3 METAL PITCHES

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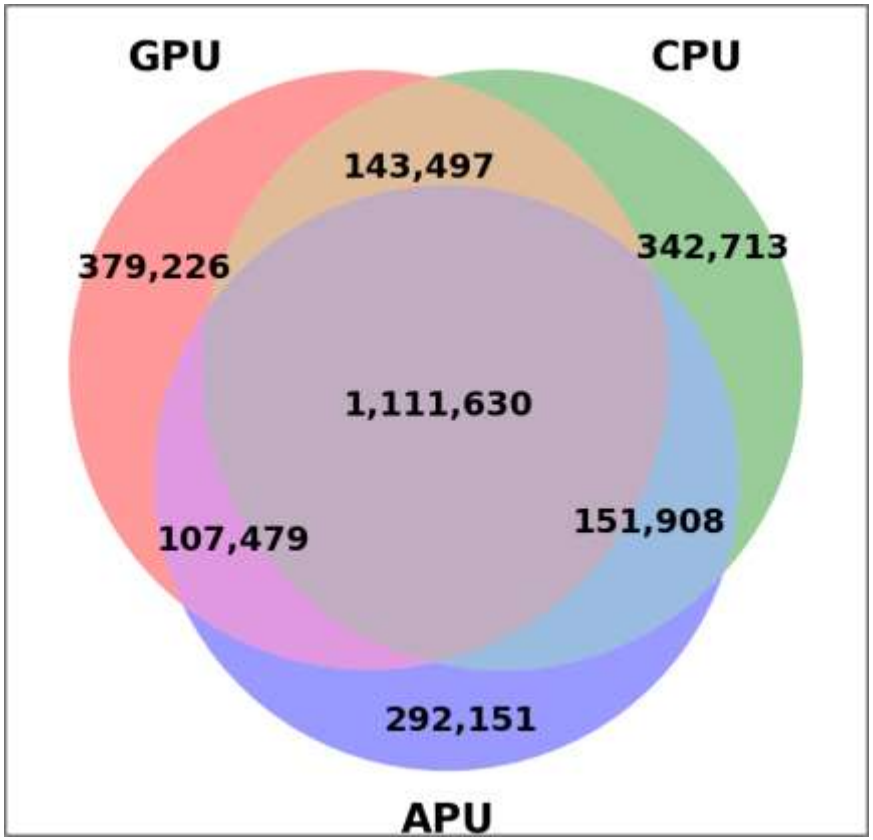
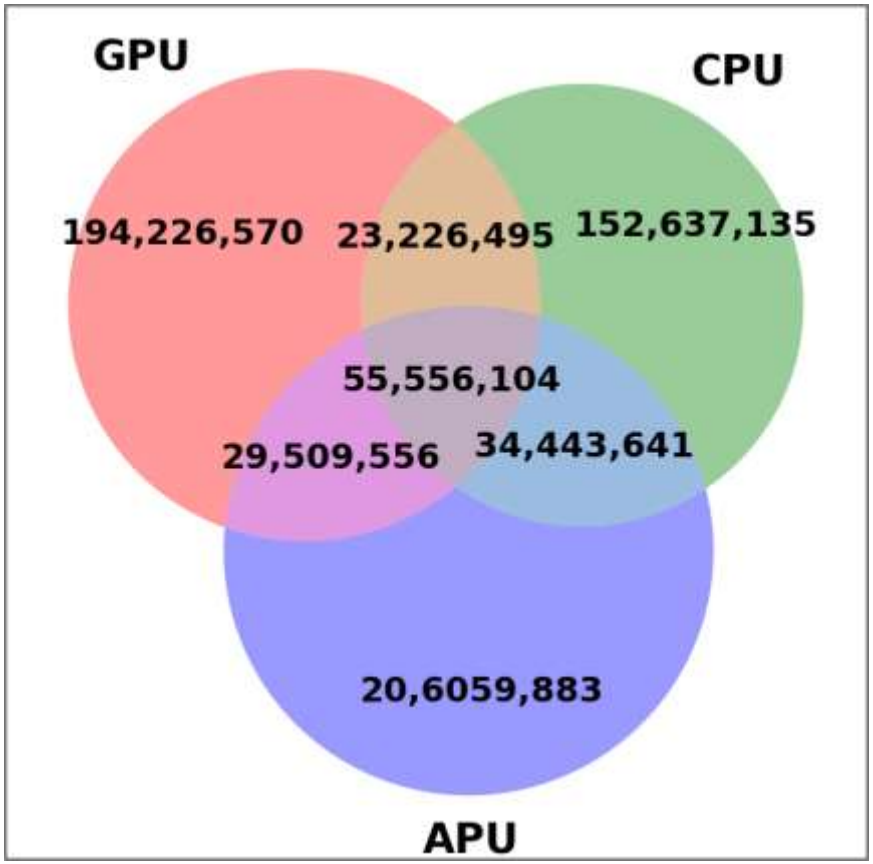
Inexact matching



Exact matching



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SUMMARY

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- Topological pattern analysis provides powerful tools for measuring physical design complexity.
- Pattern extraction can be used to identify all unique pattern topologies (with or without specific dimensions) in a layout.
  - Measurable decrease in 1x metal design complexity from 28nm to 20nm to 14nm confirms that layouts are becoming more regular.
- Extracted pattern topologies can be compared between layouts to identify differences and commonalities.
  - May be used to identify potential risks and/or drive improved layout regularity.

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