

# Pegasus Design Review Environment

Easy-to-use, high-performance, and standalone chip-finishing system

The Cadence® Pegasus™ Design Review Environment is an easy-to-use, high-performance, and standalone chip-finishing system that supports multiple formats of design, layout, and manufacturing data. The Pegasus Design Review Environment rapidly loads large layouts (GDSII, OASIS®, LEF/DEF, MEBES, and other industry-standard formats), providing a rich set of debugging and inspection features, including measurement, dynamic visualization, multiple database overlay, net connectivity tracing, cross-section viewing, and GDSII/OASIS editing.

## Overview

With the Pegasus Design Review Environment's high capacity, users can load extremely large layouts in seconds. The Pegasus Design Review Environment's signoff analysis environment allows users to place multiple layouts in one canvas and perform a range of chip-finishing functions.

The Pegasus Design Review Environment is tightly integrated with the Cadence Pegasus Verification System, and offers similar use models and flows to the Pegasus system in the Cadence Innovus™ Implementation System and Cadence Virtuoso® environment in a standalone capacity. It also works with third-party implementation and verification tools. The Pegasus Design Review Environment's high performance offers design and manufacturing teams a fast and extensible environment for efficient tapeout and chip finishing.

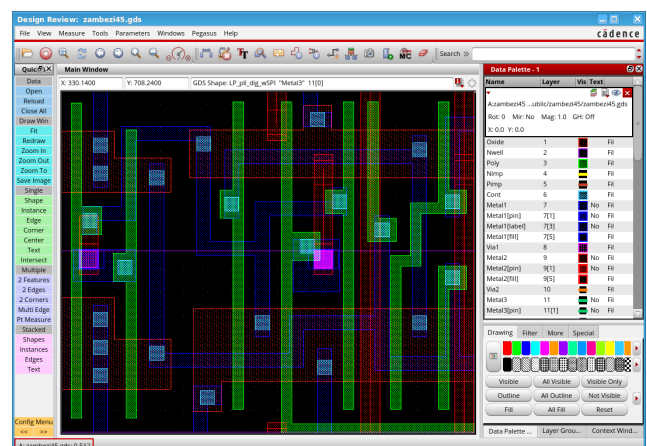


Figure 1: Pegasus Design Review Environment

## Benefits

- ▶ Improves full-chip signoff productivity via seamless integration with the Pegasus system, complete full-chip DRC/LVS/ERC review, job submission, and error analysis within a single cockpit
- ▶ Fast loading, editing, and analysis of large layouts for GDSII and OASIS
- ▶ Easy-to use, high-performance standalone chip-finishing system, with LEF/DEF support for digital design review
- ▶ Multi-format display enables viewing and superimposing of design data in any of its intermediate representations throughout the chip-finishing process
- ▶ High-performance, high-capacity data viewing with powerful options allows a full range of display, from deep sub-micron features to full reticle-level or full wafer databases
- ▶ Intelligent overlay and graphical XOR capabilities make graphical comparisons of data easy by providing an additional element of decision support
- ▶ Graphical verification of reticle designs based on the actual data used in mask manufacturing eliminates expensive jobdeck errors and improves the predictability of cycle times
- ▶ Enables coordinate scaling, offsetting, rotation, and/or mirroring for advanced data inspection or overlaying and comparing multiple disparate datasets
- ▶ Enables fast and powerful measurement and analysis
- ▶ Error browsing offers efficient and generic means of displaying and stepping through DRC error diagnostics results
- ▶ Overlay of common image formats allows graphical comparison with design and manufacturing data
- ▶ Cross-section viewing combined with multiple layout overlay allows easy visualization of 3D-IC stacking alignment
- ▶ Accepts industry-standard formats
- ▶ Includes Python and Tcl programming API for the development of custom data inspection applications
- ▶ Enables access to general data statistics and reports

## Features

### Multiple layout formats

- ▶ Supports multiple layout formats:
  - GDSII
  - OASIS
  - LEF/DEF
  - LAFF
  - GL/1
- ▶ Can be viewed concurrently to verify changes, alignment, or interaction without the worry of cell name collisions
- ▶ View and inspect in any mirrored, rotated, scaled, and offset combination
- ▶ Supports advanced query and automatic stepping functions for locating and inspecting cell references, geometries, and annotations
- ▶ Extracts cells or clipped regions from GDSII or OASIS, maintaining or flattening the hierarchy in the output database

### Pegasus integration

- ▶ Pegasus integration enables job submission and DRC, XOR, LVS, and ERC debuggers within the single environment
- ▶ Error browsing and LVS/ERC data (cross) probing is interactive even for large layouts and error databases
- ▶ Imports and applies Virtuoso Tech files to loaded data

### Multiple manufacturing formats and jobdecks

- ▶ Supports leading manufacturing formats:
  - MEBES through Mode 5 (data, jobdecks)
  - JEOL 1.0, 1.1, 2.1, 3.0, and 3.1 (data and jobdecks)
  - Toshiba VSB 11and 12 (data and jobdecks)
  - HL800, HL900, and HL950 (data)
- ▶ Stripe and segment boundaries, as well as virtual addressing, may be superimposed on the pattern data
- ▶ Can be viewed and inspected in any mirrored, rotated, scaled, and offset combination
- ▶ Supports advanced query and automatic stepping functions for locating and inspecting chips, patterns, and geometries
- ▶ Rapid display of complete mask or reticle data in fractured format using manufacturing-ready jobdecks and appropriate data files

## Robust signoff analysis environment

- ▶ The Pegasus Design Review Environment's integration with the Innovus Implementation System provides pan/zoom, layer visibility, and error marker synchronization, enabling the review of routing data in parallel with full chip design data during digital design implementation
- ▶ Connected geometries can be identified, highlighted, and analyzed based on layer-to-layer connectivity definitions
- ▶ Includes point-to-point path analysis through identified connected geometries
- ▶ Merges multiple GDSII or OASIS databases
- ▶ Converts between common database formats
- ▶ Replaces GDSII or OASIS cells in one database with cells from one or more other databases
- ▶ Supports direct geometrical modifications to GDSII or OASIS data and saves the output
- ▶ Allows layer reassignment (Move, Copy, or Delete) in GDSII or OASIS databases
- ▶ Enables visualization of 3D-IC and 3D packaging stacking alignment through cross-section viewing

## Cadence Services and Support

- ▶ Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training.
- ▶ Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- ▶ More than 30 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the internet.
- ▶ Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, Rapid Adoption Kits, software downloads, and more.
- ▶ For more information, please visit [www.cadence.com/support](http://www.cadence.com/support) for support and [www.cadence.com/training](http://www.cadence.com/training) for training.



**cadence**<sup>®</sup>

Cadence is a pivotal leader in electronic design and computational expertise, using its Intelligent System Design strategy to turn design concepts into reality. Cadence customers are the world's most creative and innovative companies, delivering extraordinary electronic products from chips to boards to systems for the most dynamic market applications. [www.cadence.com](http://www.cadence.com)

© 2021 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, and the other Cadence marks found at [www.cadence.com/go/trademarks](http://www.cadence.com/go/trademarks) are trademarks or registered trademarks of Cadence Design Systems, Inc. All other trademarks are the property of their respective owners. 14512 01/21 SA/DM/PDF

