CUSTOMER SUCCESS

Inphi Reduces Their Time to Market Taping Out 7nm Full Chip Flat with Tempus Timing Signoff

Inphi

Inphi is the leader in high-speed data movement interconnects. The company moves big data fast, around the globe, between and inside of data centers.

"We have used Tempus ECO and Tempus Signoff for all of our advanced-node initiatives. Our design sizes are big and the solution was to run flat STA and Tempus's DSTA and CMMMC capability. This allows our designers to signoff faster to meet our time-to-market demands. The Tempus solution also allows for faster convergence with Innovus Implementation, due to tight correlation, and provides better PPA. Our designers' signoff with confidence using Tempus ECO and Signoff."

Weikai Sun,
VP Engineering

Challenges

- Need to run a full chip flat signoff on 500GB machines
- STA takes almost all memory to fit a single corner on the same machines
- Need to run concurrent modes and corners instead of single-corner runs

Benefits

- Reduced iterations using Tempus™ ECO integrated in Innovus™ Implementation with Quantus™ Extraction
- Achieved additional 5% power reduction though most power optimization is done in Genus™ Synthesis
- Used DSTA to flatten CMMMC in reasonable time
  - With ~25views for setup/hold, CMMMC is most efficient in meeting our tapeout schedule
  - Runtime versus single-corner STA is less than 50% (DSTA CMMMC runs with reporting ~10hrs; STA single corner >20hrs)
- Better correlation and fastest design closure time because of shared signoff engines in Innovus, ECO, and signoff
- Ease of use with top scope allowed fixing top-level interfaces faster and with less licenses
- Excellent support provided by Cadence engineers throughout design cycle to tapeout

Design

- 7nm
- Using SOCV
- Using 16CPUs

2X
TURNAROUND TIME REDUCTION

5%
POWER IMPROVEMENTS

cadence