WHITE PAPER

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Consolidating RF Flow for High-Frequency Product Design

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Design flows are currently fragmented due to the use of poorly connected EDA tools for various design tasks. Fragmented flows are unable to meet new challenges such as increased system and circuit complexity, stricter bandwidth requirements, smaller device sizes, and changing packaging needs. In this white paper, we look at how the Cadence® Virtuoso® RF Solution provides a single, well-integrated flow that can facilitate collaboration across design teams to address these challenges and produce the next generation of high-frequency products.

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Introduction

Design flows have been disjointed since the introduction of the first circuit simulation tools. Flows have been further fragmented with the advent of specialized tools, such as those for electromagnetic analysis. Circuit simulation, layout, and electromagnetic analysis have been performed using separate tools and often by different design specialists. Earlier, designs were considerably simpler and common interface points could be defined within a subsystem. These designs led to single in-line packages mounted on high-frequency boards, such as alumina or fiberglass.

Older rudimentary packaging techniques have given way to a host of advanced techniques, including microbumps, stacked die, interposers, fan-out, multi-layer substrates, and so on, allowing for more complex design stackups.

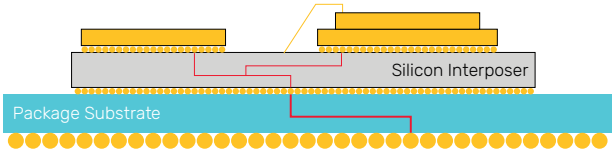


Figure 1: Design stackup

Let us consider the stacked designs illustrated in Figure 1. The designs act as a single interacting subsystem. Seen from a high-frequency design standpoint, electrical coupling in one area can easily impact other areas in the stack.

Different design teams still use disparate EDA tools for various design aspects of electronic products.

Understandably, fragmented design flows are unable to meet new challenges, some of which include:

- Increased system complexity
- Increased circuit complexity
- More stringent bandwidth requirements
- Reduced operating power requirements
- Shrinking device sizes
- Greater process complexity
- Evolving packaging and manufacturing requirements
- Product size restrictions
- Mounting costs

The Problem with Disjointed Design Flows

Device geometries have shrunk from hundreds of nanometers to a few nanometers. Integrated circuits produced at smaller technology nodes dramatically improve the end products, but to make the best use of smaller die, the packages or modules that house these die must also be smaller. More devices packed more tightly together in smaller packages increase the coupling between these devices, and a greater focus on electromagnetic (EM) analysis is needed to quantify and optimize the effects the physical layout has on the electrical design.

The CMOS environment is sufficient for most designs, but CMOS cannot meet the performance requirements necessary in the high-frequency space. Multi-technologies, such as SiGe, GaAs, GaN, and InP, and filter technologies, such as SAW and BAW, are required to meet advanced requirements. Decades ago, Gordon Moore advocated the use of multi-technologies for improved performance and cost benefits:

> *It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically. [1]*

Different portions of these extremely complex designs interact with one another and need more than the usual time for verification. The IC designer is required to meet new and difficult design challenges within aggressive timelines. Parallel design efforts might be deemed necessary to meet schedules. The paucity of time leads to incomplete simulation, both circuit and EM, and lack of complete LVS verification. Designers often need to go to tapeout without the EM simulations that are essential to verify the electrical performance.

An additional layer of ambiguity is introduced when various design teams use different design platforms. Sometimes, changes made in an analysis platform are not updated in the platform responsible for manufacturing. This can often result in layout-versus-schematic (LVS) errors or stale EM analysis results being used in electrical verification simulations.

Information exchanges across tools are also prone to errors because they do not share a common platform. Physical layouts are moved across tools, and analysis results are transferred to a simulation platform to verify electrical performance. Due to the lack of traceability of design changes, the changes are often dropped or lost, resulting in the manufacture of incorrect designs. EM analysis can be particularly faulty because multiple EM tools or EM analysis techniques are used depending on the EM problem that needs to be addressed.

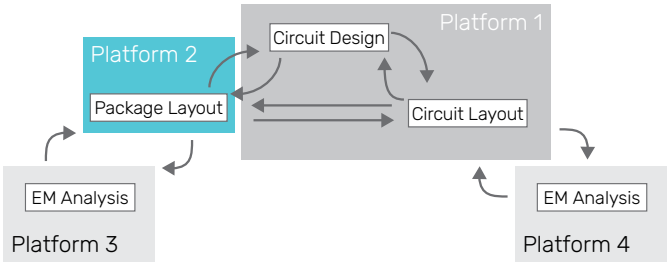


Figure 2: Information exchanges across multiple EDA tools

This fragmented design approach can ultimately lead to a working design, but the designer's effort is focused on creating a functional design and to catch and correct the errors generated due to the lack of a concerted, cohesive design flow. Designers tend to rely on previously tested designs with minimal design changes so that they can reduce the time required for verification. The hidden cost in this flow is that designers are unable to devote any time to design innovation, which is critical to differentiate the product in the market. Lack of innovation has proven to be extremely detrimental to many market leaders over the past 25 years.

What Is Required

Robust, well-integrated design flows that facilitate collaboration across design teams are required to rise above these challenges and produce the next generation of high-frequency products. Necessary capabilities should all be available in a single platform that the designer is already familiar with. Time-crunched designers would need to negotiate a substantial and expensive learning curve if they need to adopt a new platform.

The Cadence Virtuoso Analog Design Environment, along with the Cadence Spectre® Circuit Simulation Platform and the Spectre RF Option, is the most widely used platform in the electronics design industry. Most electronic designers are Virtuoso custom IC design platform users or have had some training on the platform. This platform is supported by more foundries than any other EDA tool. Most CAD organizations are also trained to support the platform.

The complexity of packaging technology requires a variety of packaging tools and checks. The Cadence Allegro® PCB design platform is an industry-leading PCB tool heavily relied on in the industry. The Virtuoso custom IC design platform has advanced multi-technology, schematic-driven, hierarchical design capabilities.

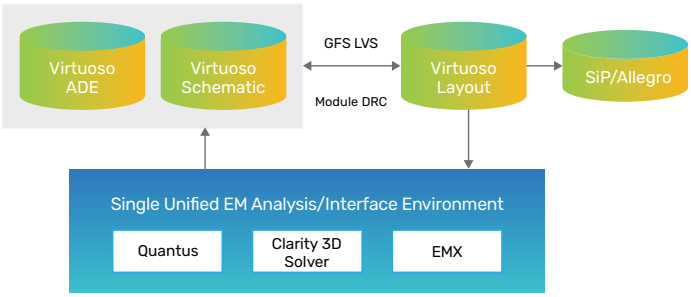


Figure 3: Virtuoso RF design flow

The Virtuoso RF Design Flow

The Virtuoso RF design flow leverages the combined strength of these platforms. It offers a schematic-driven environment with the necessary simulation, layout, analysis, and verification tools required to design module, package, and PCB designs in a single environment.

Let us look at some of the key benefits of the Virtuoso RF design flow.

Single Golden Schematic

The Virtuoso RF design flow provides a "master", or golden schematic, for simulation, LVS, EM analysis, and verification, without the need for special schematics for EM and LVS. It includes packaging connectivity information, unlike traditional IC schematics, and for not just the IC but for the entire module or package.

Multi-Technology Support

The Virtuoso RF design flow leverages the multi-technology support (MTS) within the Virtuoso platform. In Figure 4, the link between the schematic and the layout is shown over the routing of the package in the form of flight lines connecting the package pads, to SMDs and ICs. In this example, each die is a separate technology, and the package and SMDs are also a technology.

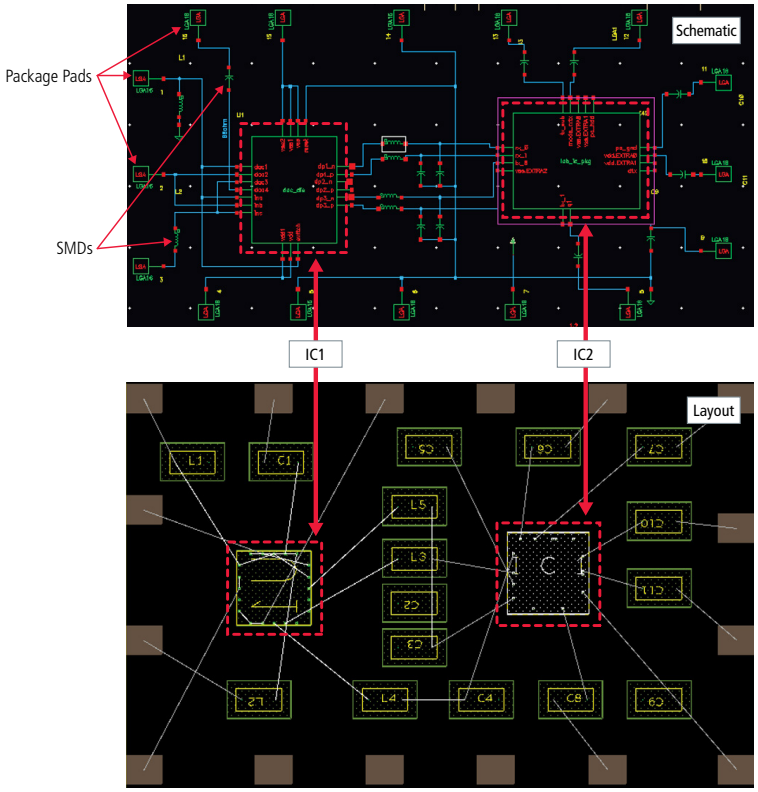
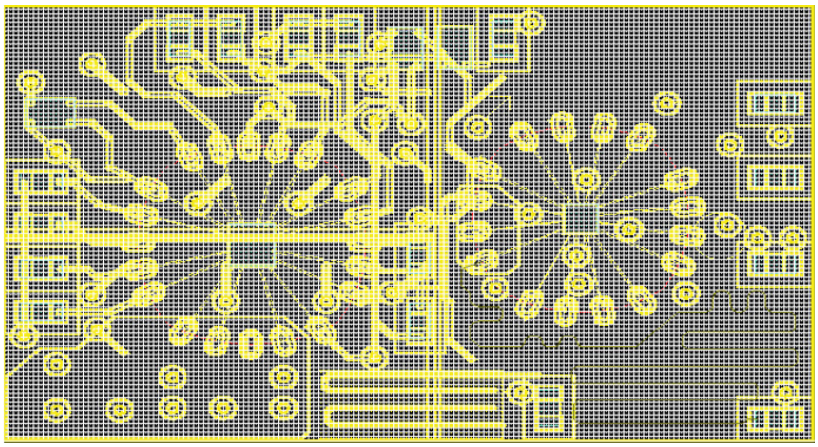


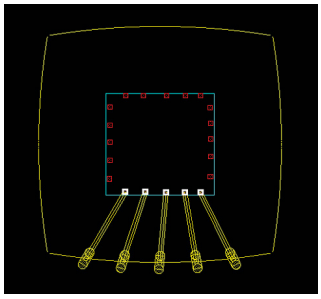
Figure 4: Schematic connectivity defines layout connectivity

Improved Routing Capabilities

The Virtuoso RF Solution adds package-style routing and wirebond capabilities, along with any angle routing and component placement, within the Virtuoso environment. The UI represents true arcs and circles and not faceted linearized segments. Additionally, dynamic voiding for power and ground planes is supported.

Figure 5 illustrates new routing features, including a bondwire guide for automatic bondwire placement. Individual bondwires can be placed one bond at a time.





- Any angle routing/placement
- Arcs, rounded end caps
- Wirebond tool
- Dynamic voiding

Figure 5: Package routing capabilities in Virtuoso RF Solution

For multi-chip modules (MCMs), the die, piece parts, and the routing in the module can be in flux within days of the tapeout and stream out.

Seamless Integration Between Virtuoso and Allegro Technologies

The Virtuoso RF flow includes the capability to develop package and module layouts while also allowing you to import package and module designs from the SiP/Allegro platform. Conversely, you can move Virtuoso layouts into Allegro Package Designer Plus SiP Layout Option for further editing and manufacturing checks and then import them back. This lets the high-frequency designer develop critical paths and structures in the flow and easily evaluate the portions of the layout that have electrical impacts on the design.

Parasitic Extraction and EM Analysis

As the design evolves and the physical layout is generated, the designer must consider the electrical effects caused by layouts, such as coupling, mismatch, insertion loss, transmission line dispersion, and so on. This leads to the need for parasitic extraction (PE) and EM analysis.

The Virtuoso RF Solution includes an enhanced EM simulation environment that allows the designer to identify and analyze a complete design or specific traces and instances within a layout. The EM simulation can be set up within the Virtuoso environment, and the resulting S-parameters or lumped equivalent circuits are captured within an extracted cell view of the golden schematic.

Representing the EM results in an extracted view, such as with PE results, has several advantages:

- There is no need for a separate EM schematic with S-parameter blocks instantiated within the schematic.
- The golden schematic contains the EM results without corrupting the schematic design and can be used for simulation with layout impairments and for LVS.
- The hierarchy editor can mix and match views for easy and quick tradeoffs of effects on the circuit design. This functionality is illustrated in Figure 6, where the two yellow traces in the schematic are represented by the M1 and M2 EM results selected in the *Back Annotate From Extracted View* window.

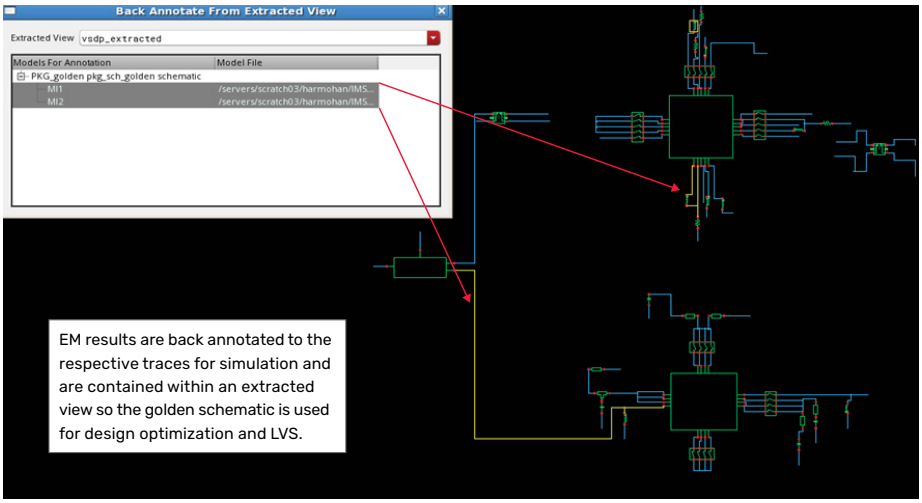


Figure 6: EM results back annotate to golden schematic cell view

The Virtuoso RF design flow offers these EM simulation techniques through the Clarity™ 3D Solver engine (full 3D adaptive finite element mesh (FEM)) and the Cadence EMX 3D Planar Solver engine.

Comprehensive Flow for IC, Package, and Module

The IC designer can include the complete die, package, and module layouts in a single layout for alignment and co-editing of the different technologies. Figure 7 illustrates the co-editing of the die and package. The die was created in the Virtuoso custom IC design platform, while the package, in this case, was imported from the Allegro Package Designer Plus SiP Layout Option. The tabs across the top of the window are the different individual designs used in the edit-in-concert mode.

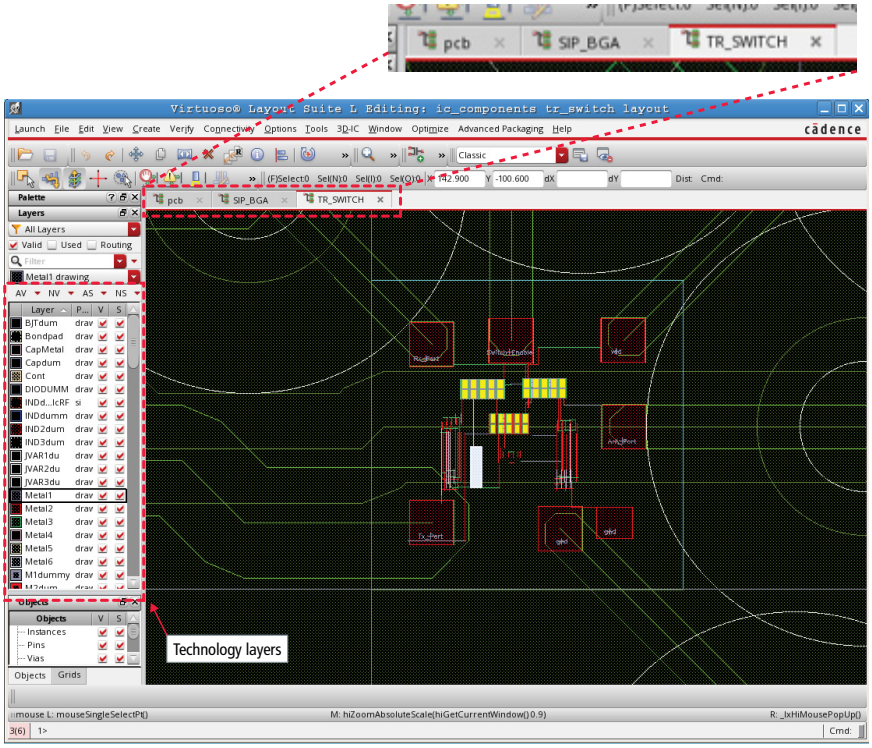


Figure 7: Co-editing a die and a package

You can select technology layers and SiP_BGA layers for editing while the die layers are still visible. The schematic definition for the die and package captured in the Virtuoso custom IC design platform also includes the interface from die to package. The pads and balls move together during editing and retain connectivity. If the package and die alignment are broken, a flight line indicates the schematic connectivity.

This allows IC and package design teams to work independently and still be able to catch design differences between die layout and the die footprint on the package layout. Conversely, design teams can edit the package and the die layouts in concert, thereby always keeping them in sync.

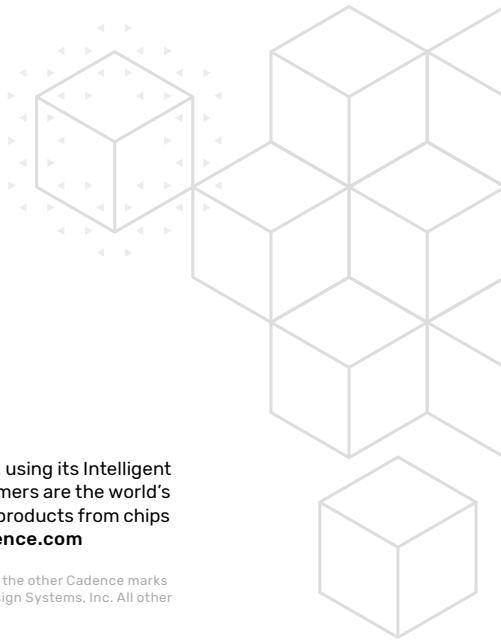
Conclusion

The Virtuoso RF design flow brings together in a single flow the necessary simulation, layout, PE, EM, LVS, and DRC tools required for the next generation of high-frequency products. The flow allows for greater collaboration across design disciplines and affords designers the time to innovate instead of spending precious time verifying layouts for intended functionality. The seamless integration of PE and EM tools further improves productivity by reducing the number of errors caused by fragmented flows. To conclude, the Virtuoso RF design flow is decidedly the most optimum environment to design the next-generation of high-frequency products.

For more information on Virtuoso RF Solution, visit www.cadence.com/go/virtuosorfni.

References

1. G. Moore, "Cramming More Components onto Integrated Circuits," *Electronics*, vol. 38, no. 8, p. 114, 1965.



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