DATASHEET

cadence®

Spectre Extensive Partitioning Simulator (XPS)

FastSPICE high-performance and capacity simulation needed to handle memory and mixed-signal designs

The Cadence® Spectre® Extensive Partitioning Simulator (XPS) is a high-performance transistor-level FastSPICE circuit simulator for pre- and post-layout verification of memories, custom digital, and analog/mixed-signal SoC designs. It delivers the capacity, accuracy, and speed required for verification of modern complex and tightly coupled full-chip designs. It uses advanced proprietary partitioning techniques to deliver unparalleled performance compared to traditional FastSPICE simulators, delivering the needed throughput for design and verification of the complex full-chip designs.

Spectre Simulation Platform

As the industry's leading solution for balancing high-performance and capacity needs with analog accuracy, the Cadence® Spectre® Simulation Platform encompasses multiple solvers that allow a designer to move easily and seamlessly between circuit-, block-, and system-level simulation and verification tasks. The foundation of the platform is a unified set of technologies shared by all of the simulators—the parser, device models, Verilog-A behavioral modeling, input data formats, output data formats, etc.—thereby guaranteeing consistent and accurate evaluation methods regardless of the simulator selected. In addition to the individual solvers, the Spectre simulation technology is well integrated into other Cadence technology platforms, including Xcelium™ Logic Simulation, Liberate™ Trio Characterization Suite, Legato™ Reliability Solution, Virtuoso® ADE Product Suite, Voltus™-Fi Custom Power Integrity Solution, and the Virtuoso RF Solution, to provide the industry's most comprehensive cross-domain simulation solution.

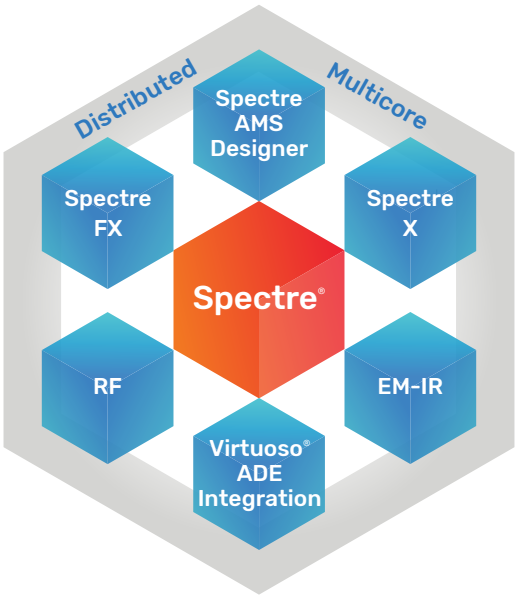

Figure 1: Spectre Simulation Platform

Spectre Extensive Partitioning Simulator (XPS)

Benefits

- Provides high performance and capacity pre-and post-layout simulation for design and IP characterization at the block and chip level
- Provides a comprehensive set of transistor-level electrical rule checks
- Delivers advanced EM-IR analysis for optimal throughput
- Supports large and complex post-layout designs, delivering a significant reduction in simulation run time compared to traditional FastSPICE simulator
- Proven Spectre use model for easy set up and post-processing of results
- Tightly integrated into the Cadence Virtuoso® ADE Product Suite and full command line support
- Built-in fast Monte Carlo statistical analysis
- EM-IR analysis with an advanced power network solver
- Built-in advanced parasitic reduction for faster post-layout simulation
- Static and dynamic circuits checks

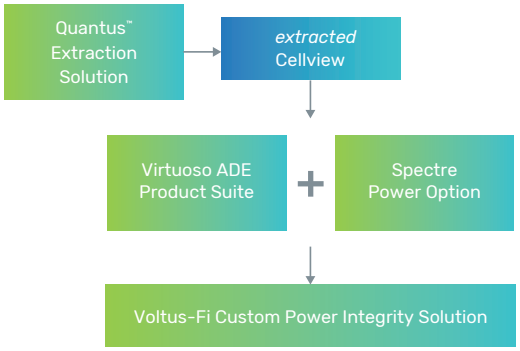

Figure 2: Cadence integrated EM-IR solution

Features

Advanced partition technology results industry-leading runtime performance

The advanced partition technology in Spectre XPS allows the netlist to be partitioned to a small number of devices. Different partitions can be simulated together based on the coupling effects and each partition can be simulated at multi-rate to ensure accurate and fast results. Once the user specifies the memory type, Spectre XPS utilizes a unique and automatic partition for mixed-signal designs to ensure that the analog components get the SPICE accuracy while the digital components get the speed.

Automatic partition provides analog accuracy and digital performance

Spectre XPS provides mixed-signal support. After the netlist is read in, it is automatically partitioned into analog and digital. The high-precision analog components are run with Spectre APS, and the digital components are run with Spectre XPS. Advanced island-based analog multi-rate technology is applied to ensure that you get the best performance without compromising accuracy.

Integrated EM-IR solution

Spectre EM-IR uses a voltage-based two-stage iterated method to increase throughput and capacity with good accuracy. It avoids the need to store a huge current database by running a fast voltage-only simulation with RC reduction in the first stage. It accurately calculates tap currents and RC effects on voltage in the second stage with multiprocessor support. Furthermore, it treats the power-gating transistor as-is without approximation, which leads to an accurate EM-IR ramp-up analysis. Spectre EM-IR is fully integrated with the Virtuoso ADE Product Suite and the analysis results can be post-processed with the Voltus-Fi Custom Power Integrity Solution (Figure 2).

Specifications

Comprehensive list of analog device models supported

- Advanced-node models, including the latest versions of the BSIM CMG, BSIM IMG, and UTSOI models
- MOSFET models, including the latest versions of the BSIM3, BSIM4, BSIM Bulk (BSIM6), PSP, and HiSIM
- High-voltage MOS models, including the latest versions of the HiSIM HV, MOS9, MOS11, and EKV
- Silicon-on-insulator (SOI), including latest versions of BTASOI, SSIMSOI, BSIMSOI, BSIMSOI PD, and HiSIM SOI
- Bipolar junction transistor (BJT) models, including the latest versions of VBIC, HICUM, Mextram, HBT, and Gummel-Poon models
- Diode models, including the diode, Phillips level 500, and CMC diode models
- JFET models, including the JFET, Phillips level 100 JFET, and Individual dual-gate JFET models
- IGBT models, including PSpice® IGBT model and HiSIM IGBT models

- Resistors, including linear resistor, diffused resistor, CMC two-terminal and three-terminal resistor, and physical resistor models
- GaAs MESFET models, includes latest versions of GaAs, TOM2, TOM3, and Angelov
- GaN MESFET models, including Angelov, ASM, and MVSG models
- Silicon TFT models, including RPI Poly-Silicon and Amorphous Silicon Thin-Film models
- Verilog-A compact device models
- Z and S domain sources
- User-defined compiled model interface (CMI), allowing for the rapid inclusion of user-defined models
- Josephson Junctions
- Specialized reliability models (AgeMOS) for simulating the effect of HCI and BTI
- Miscellaneous power models, including the relay, transformer, non-linear magnetic core, and winding
- Miscellaneous RF models, including the DC block, DC feedthrough, and microstrip and stripline elements (bend, cross, corner, curve, open line, tee models)

Language and netlist support

The netlist formats, behavioral modeling languages, parasitic netlist formats, and stimulus files are common across the Spectre Simulation Platform. Supported formats include:

- Spectre and SPICE netlist formats
- Spectre, SPICE, and PSpice models
- Verilog-A 2.0 LRM-compliant behavioral models and structural netlists
- DSPF/SPEF parasitic formats
- S-parameter data files in Touchstone, CITI-file, and Spectre formats
- SST2, PSF, PSF XL, and FSDB waveform formats
- Digital vector (VEC), Verilog-Value Change Dump (VCD), Extended Verilog-Value Change Dump (EVCD), and digital stimulus

Platform support

- x86 64-bit Red Hat Enterprise 6.5 (and higher) and V7, SLES 11 and 12
- Commercially available cloud solutions

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training.
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- More than 30 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the internet.
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, Rapid Adoption Kits, software downloads, and more.
- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training.