DATASHEET

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Spectre AMS Designer

Advanced mixed-signal simulation solution

The Cadence® Spectre® AMS Designer provides an advanced mixed-signal simulation solution for the design and verification of analog, RF, memory, and mixed-signal silicon realization. It is integrated with the Cadence Virtuoso® full-custom environment as well as the Cadence Xcelium™ Parallel Logic Simulator. Spectre AMS Designer provides a single-simulation executable with flexible abstraction support through the standard mixed-signal languages (Verilog-AMS and VHDL-AMS), SystemVerilog, and/or SPICE-level models. As the bridge between the analog and digital domains, it enables users to choose the right analog solver for the right design or verification task. Designers can choose Spectre technologies for SPICE-accurate block-level analog and RF designs: Spectre Accelerated Parallel Simulator (APS), Spectre RF Option, Spectre X Simulator, and Spectre eXtensive Partioning Simulator (XPS).

Spectre Simulation Platform

As the industry's leading solution for balancing high-performance and capacity needs with analog accuracy, the Cadence® Spectre® Simulation Platform encompasses multiple solvers that allow a designer to move easily and seamlessly between circuit-, block-, and system-level simulation and verification tasks. The foundation of the platform is a unified set of technologies shared by all of the simulators—the parser, device models, Verilog-A behavioral modeling, input data formats, output data formats, etc.—thereby guaranteeing consistent and accurate evaluation methods regardless of the simulator selected. In addition to the individual solvers, the Spectre simulation technology is well integrated into other Cadence technology platforms, including Xcelium™ Logic Simulation, Liberate™ Trio Characterization Suite, Legato™ Reliability Solution, Virtuoso® ADE Product Suite, Voltus™-Fi Custom Power Integrity Solution, and the Virtuoso RF Solution, to provide the industry's most comprehensive cross-domain simulation solution.

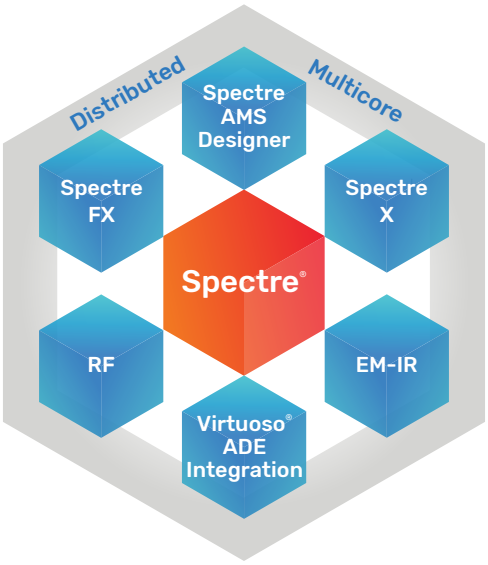

Figure 1: Spectre Simulation Platform

Spectre AMS Designer

Benefits

- Ensures design quality with proven Spectre and Xcelium simulation technologies
- Supports both analog design flow use models in Virtuoso ADE Product Suite as well as digital-verification use models in the Xcelium environment
- Supports both top-down and bottom-up methodologies to quickly detect and fix design failures early in the design cycle, helping to meet tapeout schedules
- Extensive language support allows a higher level of abstraction and accelerates simulation to achieve faster turnaround time
- Supports simulation of RF circuits at full SPICE accuracy by combining envelope analysis of RF transceivers with digital baseband simulation for faster convergence of results

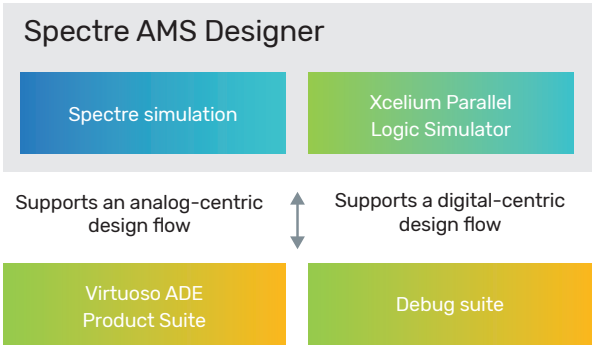

Figure 2: One simulator supports either verification flow

Features

Methodology-independent design convergence

Spectre AMS Designer provides the flexibility to combine IP from different sources and in different formats for today's SoC designs. It does more than just co-simulate analog and digital blocks. By treating Virtuoso Schematic Editor blocks and textual descriptions equally, Spectre AMS Designer allows different points of data entry. It accepts descriptions in the standard language formats of Verilog-AMS, VHDL-AMS, Verilog-A, Verilog, VHDL, SystemVerilog, and SystemC®, as well as SPICE, and performs simulation on any combination of these languages. This allows bottom-up and top-down design methodologies to converge into a fully functional design.

Different levels of abstraction, such as Verilog-AMS or VHDL-AMS behavioral models and schematic representation, are easily interchangeable to allow the design to change over time from full behavioral to full transistor. The entire design is configured using the hierarchy editor, which facilitates the viewing and design preparation of a complex mixed-signal design. Automatically inserted interface elements are used to translate signals from one domain to the next, leaving the user free to simulate with different design configurations to easily trade off simulation speed for simulation accuracy.

The SpectreAMS Designer also supports IP encryption using RSA technology, which allows the user to establish both IP reuse and virtual-prototyping methodologies.

Integrated with proven Spectre and Xcelium simulation technologies

Spectre AMS Designer is a mixed-signal simulator based on the proven technology of the Spectre Circuit Simulator, Spectre APS, Spectre X Simulator, and Spectre XPS, and the Xcelium digital simulation capabilities. You can choose different releases of Spectre and Xcelium technologies for your mixed-signal simulation.

Analog-centric flow with Virtuoso environment

Spectre AMS Designer is tightly integrated with the Virtuoso ADE Product Suite for mixed-signal block design. It uses native Analog Design Environment netlisting technologies to combine schematics and behavioral views, enabling users to independently manage the level of abstraction of each block. The entire design is configured using the hierarchy editor, which facilitates the viewing and design preparation of a complex mixed-signal design.

- Using Spectre AMS Designer ensures that the user gets golden simulation results for performance measurements
- Advanced circuit analysis such as Monte Carlo analysis can be performed with the Spectre AMS Designer interface, leveraging the performance benefits of behavioral models and using the same set-up as the other Spectre simulators
- Advanced-model validation capabilities allow users to automatically verify their circuit design against a behavioral model by comparing simulation waveforms

Digital-centric flow with Xcelium simulation

Spectre AMS Designer works natively in the Xcelium environment for digital-centric verification. A single control file is used to define how analog blocks are integrated into the digital SoC. Analog and RTL blocks can be easily interchanged to trade off accuracy and performance. It supports all features in the Xcelium environment including testbench analysis, Cadence® technology, and verification planning.

- Automatically inserted interface elements are used to translate signals from one domain to the next, leaving the user free to simulate with different design configurations to easily trade off simulation speed for simulation accuracy.
- In the verification flow, Spectre Circuit Simulator is used as the built-in analog simulation engine, enabling verification of large mixed-signal designs. The Xcelium digital simulation engine delivers high-performance native Verilog, SystemVerilog, VHDL, SystemC, and e simulation.
- The SimVision multi-language debugging environment allows users to view analog and digital signals in a single waveform environment.
- Cross-domain connectivity between testbenches and design IP blocks from multiple vendors is enabled by providing native connectivity between VHDL or SystemVerilog and SPICE.
- Assertion-based verification for analog and digital designs is supported by extending the syntax of PSL and SVA languages, providing an efficient and effective methodology for capturing design intent and verification automation.
- Mature digital verification methodologies, such as low-power verification, are extended to the analog domain, and support capturing power intent with CPF/UPF and automatically inserting "PowerSmart" connect modules on key interfaces.

Specifications

Virtuoso environment

- Direct Verilog-AMS netlisting
- Hierarchy editor AMS plug-in
- Hierarchy editor configuration
- Support for global design variables and global signals
- Inherited connections

Spectre AMS Designer

- Flexible integration of desired Spectre and Xcelium releases
- Digital and real number-modeling capabilities
- System-level simulations with links to MathWorks Simulink
- Save/restart
- Common mixed-signal waveform database

Design inputs

- OpenAccess database
- Verilog-AMS 2.0
- VHDL-AMS 1076.1
- Verilog (IEEE 1364-1995, IEEE 1364-2001 extensions)
- VHDL (IEEE 1076-1987, IEEE 1076-1993, IEEE 1076.4-2000 [VITAL 2000])
- Spectre and SPICE netlist formats
- SystemVerilog (IEEE 1800)
- Unified Power Format (UPF) or Common Power Format (CPF)

Xcelium platform

- SystemC (OSCI SystemC v2.01) and SystemC Verification Library (OSCI SCV 1.0)
- Specman technology

Specifications

Comprehensive list of analog device models supported

- Advanced-node models, including the latest versions of the BSIM CMG, BSIM IMG, and UTSOI models
- MOSFET models, including the latest versions of the BSIM3, BSIM4, BSIM Bulk (BSIM6), PSP, and HiSIM
- High-voltage MOS models, including the latest versions of the HiSIM HV, MOS9, MOS11, and EKV
- Silicon-on-insulator (SOI), including latest versions of BTASOI, SSIMSOI, BSIMSOI, BSIMSOI PD, and HiSIM SOI
- Bipolar junction transistor (BJT) models, including the latest versions of VBIC, HICUM, Mextram, HBT, and Gummel-Poon models
- Diode models, including the diode, Phillips level 500, and CMC diode models
- JFET models, including the JFET, Phillips level 100 JFET, and Individual dual-gate JFET models
- IGBT models, including PSpice® IGBT model and HiSIM IGBT models
- Resistors, including linear resistor, diffused resistor, CMC two-terminal and three-terminal resistor, and physical resistor models
- GaAs MESFET models, includes latest versions of GaAs, TOM2, TOM3, and Angelov
- GaN MESFET models, including Angelov, ASM, and MVSG models

- Silicon TFT models, including RPI Poly-Silicon and Amorphous Silicon Thin-Film models
- Verilog-A compact device models
- Z and S domain sources
- User-defined compiled model interface (CMI), allowing for the rapid inclusion of user-defined models
- Josephson Junctions
- Specialized reliability models (AgeMOS) for simulating the effect of HCI and BTI
- Miscellaneous power models, including the relay, transformer, non-linear magnetic core, and winding
- Miscellaneous RF models, including the dc block, dc feedthrough, and microstrip and stripline elements (bend, cross, corner, curve, open line, tee models)

Language and netlist support

The netlist formats, behavioral modeling languages, parasitic netlist formats, and stimulus files are common across the Spectre Simulation Platform. Supported formats include:

- Spectre and SPICE netlist formats
- Spectre, SPICE, and PSpice models
- Verilog-A 2.0 LRM-compliant behavioral models and structural netlists
- DSPF/SPEF parasitic formats
- S-parameter data files in Touchstone, CITI-file, and Spectre formats
- SST2, PSF, PSF XL, and FSDB waveform formats
- Digital vector (VEC), Verilog-Value Change Dump (VCD), Extended Verilog-Value Change Dump (EVCD), and digital stimulus

Platform support

- x86 64-bit Red Hat Enterprise 6.5 (and higher) and V7, SLES 11 and 12
- Commercially available cloud solutions

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training.
- Cadence-certified instructors teach more than 70 courses and bring their real-world experience into the classroom.
- More than 30 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the internet.
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, Rapid Adoption Kits, software downloads, and more.
- For more information, please visit www.cadence.com/support for support and www.cadence.com/training for training.

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