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Addressing the Challenges of Photonic IC Design Via an Integrated Electronic/Photonic Design Automation Environment

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Photonics—the science and technology of generating, controlling, and detecting light—is transitioning quickly into mainstream electronic designs. Photonic IC (PIC) design does, however, come with some unique challenges in areas including layout, error checking, and circuit modeling. While electronic designers would have expertise in using a traditional electronic design automation (EDA) flow, standard EDA flows simply aren't equipped to accommodate the integration of photonics circuits and components into their electronic counterparts reliably or effectively. In this paper, we examine how a new integrated electronic/photonic design automation (EPDA) environment solves these challenges, supporting first-time-right designs with a high level of design productivity.

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Introduction

The movement of information using light is nothing new. Fiber optic communications networks are commonplace in data and telecommunications systems across the world. Advances in IC technology and fabrication are now making it possible to move optic, or more accurately photonic communications, to the device level. Using traditional CMOS fabrication processes and materials, it's now possible to design PICs, carrying photons instead of electrons. These devices, capable of moving, modulating, and detecting light, integrate tens to thousands of discrete components into a single chip and offer very high-bandwidth performance at low power.

According to Transparency Market Research, the photonic IC market, valued at US$0.19 billion in 2013, is anticipated to reach US$1.3 billion globally by 2022[1]. Delivering high bandwidth, low power, and small form factors, PICs address a variety of application areas:

- Telecommunications hardware for high-speed networks, coherent receivers, and fiber-to-the-home systems
- Datacenters, including data communications, computer communications, and consumer electronics equipment
- Antenna and RF systems, including wireless access networks, radio over fiber, phased array antennas, and LIDAR systems
- Bio-photonics, including life science research, clinical diagnostics, protein and nucleic acid testing, food safety, and medical imaging systems
- Environmental sensing systems, e.g. oil and gas and water quality

Relative to electronic IC design, PIC design and fabrication is in its infancy. Most design is vertically integrated, from fabrication processes to component designs. Chip-scale design is comprised of tens of components and is often layout driven and completed by the same designers who develop the fundamental components. The efficiencies, reliability, and scale that have long driven electronic IC design are only beginning to emerge in photonics.

As the potential applications for integrated photonics continues to expand, and system designers seek to utilize the best technology available to address their needs, PIC and electronic IC design methodologies must combine. Reliable, repeatable component libraries and fabrication processes for photonic elements must replace custom libraries and fabrication methods. Automated design tools must enable seamless and reliable design, analysis, and optimization of both electronic and photonic circuits. While simple in principle, in practice there are significant challenges to overcome in merging electronic and photonic design. Photonics presents physical and analytical challenges that require unique design tools and methods not used in traditional electronic IC design (Figure 1).

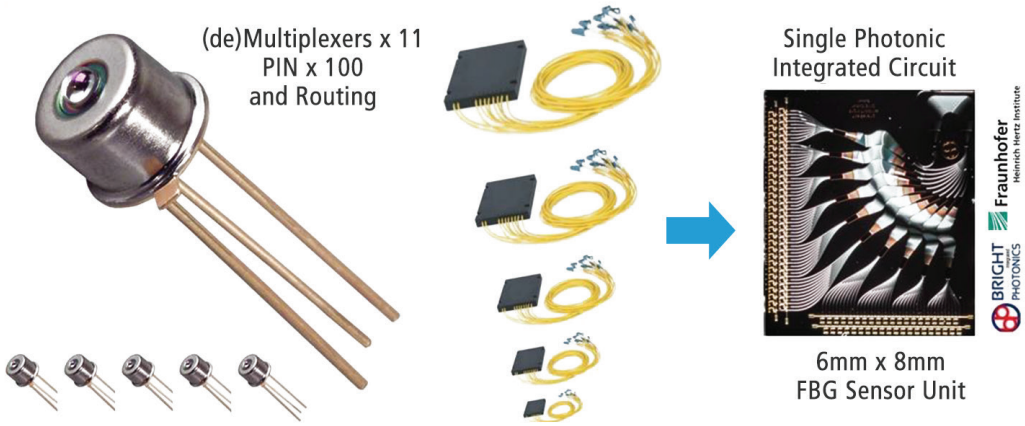

Figure 1: Designing a PIC requires meeting challenges that are much different than those of a typical electronic circuit. Image courtesy of PhoeniX Software.

PIC Design Challenges

Bringing integrated photonics design into an electronic IC EDA environment has challenges:

- Curvilinear layout. Photonic structures require smooth bends and curves not used in electronic IC design.
- Photonic circuit modeling and analysis capable of addressing the unique characteristics of photonic components. There is no widely accepted SPICE equivalent for circuit modeling.
- Process Design Kits (PDKs) that include the fundamental photonic components, design rules, and processes that form the basis of all electronic IC design flows
- Improved verification methodologies and tools to address the inclusion of integrated photonic circuits, including layout vs. schematic (LVS) and design rule checking (DRC)

The curvilinear layout of PIC components presents one of the toughest design challenges. Waveguide routing requires a curved format instead of rectilinear/Manhattan-style routing to ensure that light stays in a waveguide. Most basic photonic components contain curvilinear features. Layouts for mask fabrication are polygon based and defined on a grid with a given resolution; therefore, the discretization of curvilinear shapes like a circle, or bend, has to be properly defined to keep a smooth sidewall.

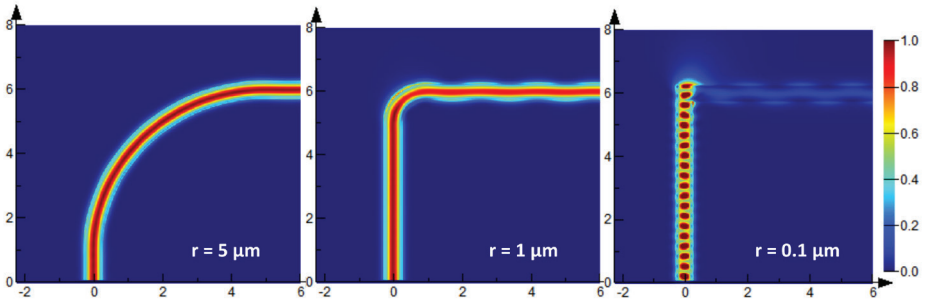

Figure 2: Waveguide routing requires a curved format instead of rectilinear/Manhattan-style routing to ensure that light stays in a waveguide. Simulation of a curved waveguide with different radii. Image courtesy of Lumerical Solutions, Inc.

Photonic circuit modeling is also a challenge, particularly since there isn't a widely accepted SPICE equivalent for modeling and simulation of complicated optical signals. Compared to an electrical signal, an optical signal is bidirectional and multi-mode, and a simulator needs to be able to handle both amplitude and phase. Simulation in both the frequency- and time-domain is also required. Traditional SPICE simulators typically are unable to meet these requirements.

A compact or behavioral model of the photonic element needs to describe the device using multi-physics effects, i.e., not only pure optical characteristics, but also electro-optical, thermo-optical, and mechano-optical effects. In applications like a transceiver, the photonic circuit is designed together with an electrical driver circuit, and the simulation framework has to allow for either co-design through waveform exchange (sequential simulation) or for true co-simulation, such as in a control loop to stabilize the output frequency of an integrated laser. Often, PIC designers find themselves redefining the same circuit in different tools for simulation and for layout implementation due to the lack of an integrated design environment. This duplication of design for analysis and implementation is time consuming and error prone. While it would be useful to extend electrical SPICE simulator capabilities to cover photonics, it is better to have a dedicated simulation engine for optical circuits to capture their unique characteristics effectively. For co-simulation to be possible, the optical circuit simulation engine would need to be able to communicate with traditional SPICE simulators.

Design automation tools, along with reliable, repeatable fabrication processes, are at the core of what has enabled electronic IC design to deliver extremely large-scale, complex systems and devices. Similar to what has happened with electronic IC design, there is an emerging separation of photonic circuit designers and photonics component designers. Circuit designers rely on a schematic-driven design flow to build systems that address their end applications. They rely on components from a Process Design Kit (PDK) and the corresponding calibrated compact models for system design and simulation. Component designers, on the other hand, typically use a layout-driven approach, and they are interested in the fundamental device physics, employing TCAD simulation tools to design and optimize individual elements such as a modulator or waveguide splitter. To simulate a component from layout, process simulation tools are used to generate 3D structures that are then fed to a TCAD simulation. Device compact models are generated based on these multi-physics simulations, which can be computationally expensive. The compact models allow system designers to model the behavior of hundreds, thousands, or millions of devices, a scale which is entirely unrealistic using TCAD simulators and solvers. Such compact models are often specific to a given fabrication process and calibrated with measurements. Automated workflows help to validate/calibrate the models. This is an iterative process that ultimately enables the creation of mature photonic PDKs which enable the electronic/photonic circuit designer to confidently implement chip and system-level applications without always returning to component-level-first principles and design.

Today, most PIC designers are both component and circuit designers. PDKs provide the fundamentals to meet the reliability, scale, and cost target of a particular design. For PICs, the availability of robust PDKs isn't very widespread. Many PDKs are developed by the designers, rather than the foundries offering fabrication services. Many foundry-generated PDKs for photonics are still very primitive, offering a limited amount of fixed GDS layout cells and text documents outlining specifications and process rules. Fortunately, generic photonic design libraries are available to fill in most of the gaps, allowing PIC designers to design reliable circuits, even without a complete PDK.

Similar to the challenge of creating a curvilinear structure in a layout tool, the discretization of a curvilinear shape into a polygon can introduce many false DRC errors. The capabilities of an error checker need to be extended to handle photonic structures along with the creation of proper rule files specifically developed for photonics. For LVS, the challenge lies more in the fact that a given PDK does not contain all the necessary components. In other words, some layout customization will always be necessary here.

What's Needed to Enhance the PIC Design Flow?

Dedicated photonic simulation and layout capabilities are needed to meet the unique challenges of PIC design. For system designs, the ideal flow is a schematic-driven approach where you can run circuit simulations directly from the schematic. Most systems are comprised of both electrical and photonic sub-circuits; to simulate and optimize the overall circuit performance, it's important to have the capability to design the full system within the same framework. This is especially true for components that need to be included in both the electrical and photonic circuit simulation, such as a modulator which acts as a load in a CMOS driver simulation and as a modulator in a photonic circuit simulation.

In order to calculate key metrics for photonic circuits such as S-parameters, eye diagrams, and bit error rates, you need to be able to perform time and frequency domain simulations. A circuit simulation is only meaningful if the underlying compact models are validated and calibrated to measurement data. Component-level simulators that are capable of modeling optical, electro-optical, and thermo-optical effects are invaluable to understand the device physics and extract compact models. Such models are not always just based on TCAD simulations but are informed by measurements, e.g. the loss in an optical waveguide, or analytical formulas. The parameter extraction and refinement of the compact models has to be automated as much as possible.

As much as a proven photonic PDK containing validated compact models is needed for system simulations, a PDK is also invaluable for generating the layout. A PDK component has to include all the information necessary to generate a layout in the form of either a fixed or a parameterized cell. While a layout-driven design is viable for smaller circuits, for more sophisticated circuits integrating photonics and electronics components, more familiar schematic-driven tools are essential as component counts and complexity rise.

Having the right tools for modeling and layout implementation not only shortens the design cycle but also reduces the number of cycles necessary for a successful design.

New Automated Flow for Photonic Design

Cadence, Lumerical Solutions, and PhoeniX Software have developed a new electronic/photonic design automation (EPDA) environment that is well suited to designers of hybrid photonic ICs (a 3D-IC stack with a traditional electronics chip on top of a photonic chip) and monolithic photonic ICs (single chip carrying both traditional electronics and photonics). The EPDA environment is based on the proven and familiar schematic-driven EDA flow offered by Cadence and extended accommodate the design of photonic circuits through the seamless integration of Lumerical INTERCONNECT, a simulation engine for multi-mode, bi-directional, time- and frequency-domain mixed-signal circuit modeling, and PhoeniX Software's advanced algorithms for the accurate generation of waveguide and photonic component layout and mask layers. This flow uses a photonic PDK with layout information, design rules, and compact models aligned and calibrated to the foundry fabrication process.

The EPDA flow not only enables the incorporation of integrated photonics into a design, but also takes advantage of innovative electronic design methodologies such as 3D-ICs and hybrid monolithic designs, and allows for scaling towards more complex systems while improving yield and quality. The EPDA framework as shown in Figure 4 consists of:

- Schematic capture of both the photonic and electronic circuits using Cadence® Virtuoso® Schematic Editor
- Photonic circuit simulation and optimization within Cadence Virtuoso Analog Design Environment, using Lumerical INTERCONNECT, a dedicated PIC simulation engine.
- INTERCONNECT, working together with the Cadence Spectre® simulation environment and Virtuoso Analog Design Environment, also features an electrical/optical co-simulation capability. Both the electrical and optical domains are updated as they interact with each other during each simulation time step in the co-simulation scenario. A Verilog-A direct programming interface (DPI) synchronizes and performs data exchange between the Spectre electrical circuit simulator and the INTERCONNECT photonic circuit simulator. An automatically generated interface in Verilog-A allows you to use optical sub-circuits within the Spectre environment.
- Photonic layout implementation in Cadence Virtuoso Layout Suite XL
  - The same golden schematic used in simulation is used for schematic-driven layout
  - Support for PCells and advanced generators via integration of PhoeniX Software's advanced curvilinear shape core
  - Layout-to-schematic back annotation of device and waveguide parameters for iterative circuit verification and optimization

  - Device and compounded waveguide parameters back-annotation to the schematic provides layout-accurate optical simulation
- Photonic component parameter extraction and model generation for custom-defined components
- Compact model management including library generation and distribution management
- Co-floorplanning of the electronic and photonic components for hybrid systems

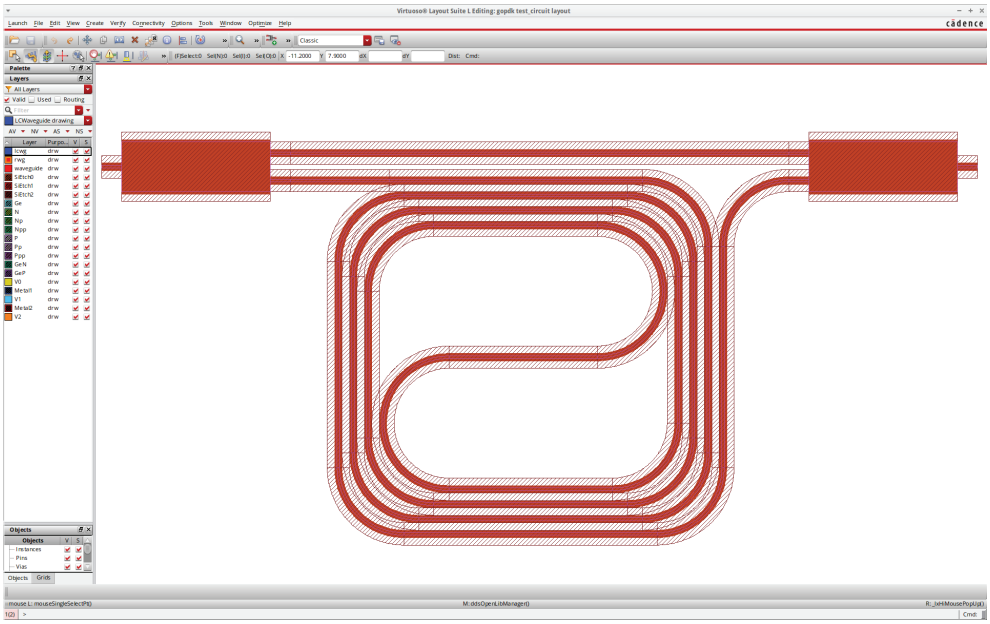

Figure 3: Example layout of an unbalanced Mach-Zehnder interferometer in Virtuoso Layout Suite.

The steps of the flow are as follows:

1. Capture optical and electrical circuit in Virtuoso Schematic Editor
2. Simulate photonic circuits in Virtuoso Analog Design Environment using Lumerical INTERCONNECT
3. Define and perform sequential electrical/optical circuit simulations via waveform exchange using the Spectre platform and INTERCONNECT. Alternatively, perform electrical/optical co-simulation using the Spectre platform and INTERCONNECT in concert.
4. Run circuit optimization and yield analysis
5. Implement the layout in Virtuoso Layout Suite XL, using PhoeniX Software's algorithms for waveguide routing and photonic PCell generation in its OptoDesigner photonic chip design environment (See Figure 3 for a component layout image)
6. Run realtime in-design DRC using PhoeniX Software's curvilinear DRC engine
7. Complete final validation, mask generation, and tape out to foundry

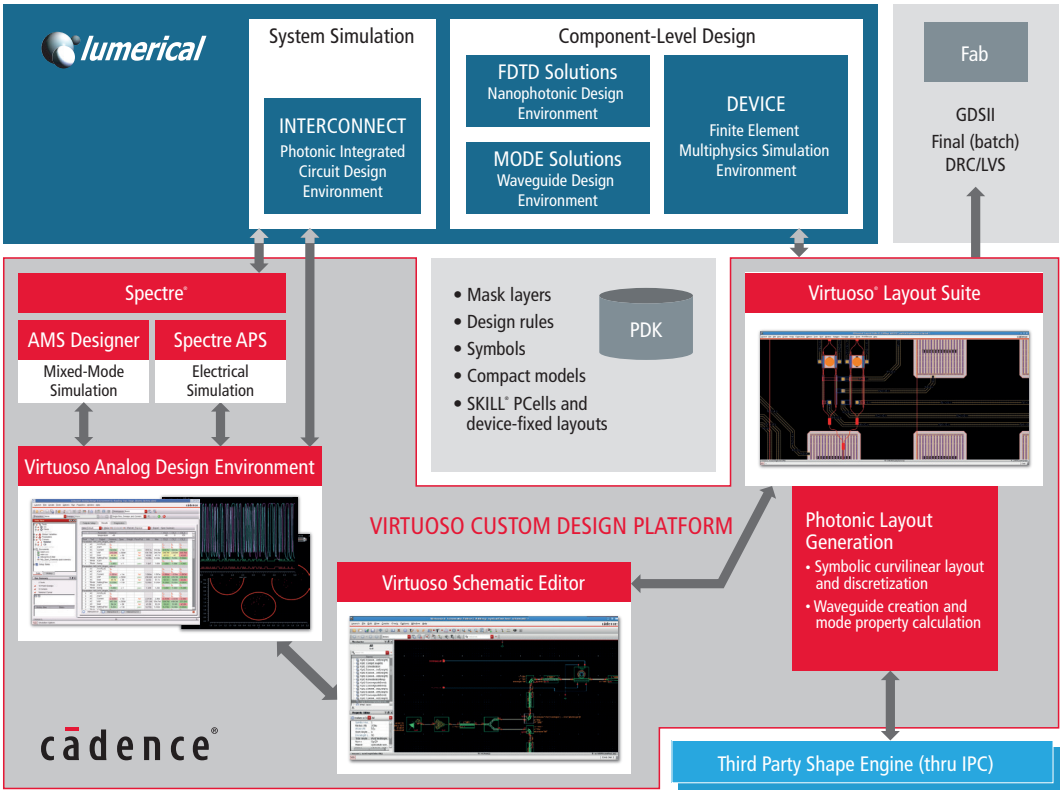

Figure 4: Electronic/photonic design automation (EPDA) environment

Summary

The market is ripe for widespread adoption of integrated photonics. Therefore, now is the time for a production-ready design flow that can accelerate the development process for first-time-right PICs. Standard EDA flows do not adequately support the integration of photonic circuits and components into their electronic counterparts. A new integrated EPDA environment brings together a proven schematic-driven EDA flow, a simulation engine for multi-mode, bi-directional, time- and frequency-domain mixed-signal circuit modeling, and advanced algorithms for the accurate generation of waveguide and photonic component layout and mask layers. By using PDKs and generic processes in integrated photonics, PIC designers have demonstrated the ability to reduce their design turnaround time from months to weeks. Environments like the EPDA flow promise to further improve design productivity for PICs.

For Further Information

Learn more about the EPDA environment at: https://www.cadence.com/content/cadence-www/global/en_US/home/solutions/photonics.html

Notes

[1] Source: http://globenewswire.com/news-release/2015/11/19/788696/10156806/en/Photonic-IC-Market-Poised-for-Strong-Growth-to-Reach-US-1-3-bn-Globally-by-2022-Transparency-Market-Research.html

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