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Melexis and Cadence

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Gael Close, System Architect, Melexis

The Customer

Melexis Microelectronic Integrated Systems, headquartered in Belgium, with R&D and manufacturing centers around the globe, develops advanced mixed-signal semiconductors, sensor ICs, and programmable sensor IC systems for the automotive electronics industry. In business for more than a decade, Melexis engineers the sustainable future with products that meet stringent quality, cost, and operating environment requirements.

System Architect Gael Close works on a team that designs mixed-signal, integrated magnetic sensors for a variety of automotive applications. Recently, the team developed a Hall effect-based sensor that's used for gear-tooth detection for wheel angle and speed sensing in a vehicle engine management system. The mixed-signal design consists of a magnetic wheel that rotates in front of the sensor. The magnetic field varies based on a mechanical wheel profile, and the chip senses the field via several Hall plates. The software in this application keeps the analog signal accurately centered so that the output comparator toggles at the right moment (i.e., when a magnetic tooth is in front of the sensor).

In this design, the sensor covers mechanical, magnetic, analog, mixed-signal, and software signal domains. Simulating the behavior of this complete system early on called for a model—a complete virtual testbench—that covers all of these domains.

The Challenge

With embedded software playing a larger role in highly integrated, single-chip automotive sensors, Melexis was experiencing greater design and verification challenges. In the automotive electronics industry, designers must deal with an increased the amount of software and, as a result, a need for new co-debug and co-verification processes.

Business Challenges
- Accelerate design process
- Increase design productivity
- Lower design costs

Design Challenges
- Streamline design and verification process
- Find and fix bugs faster
- Achieve higher level of design abstraction

Cadence Solutions
- Cadence Incisive Enterprise Simulator
- Cadence Incisive Software Extensions
- Cadence SimVision Debug
- Cadence Virtuoso Analog Design Environment

Results
- 15% reduction in IC development time
- 200X faster simulation via transaction-level model
- Earlier detection/resolution of bugs
- Enhanced collaboration between analog and software teams

Melexis has a register-transfer level (RTL) processor running Cadence® Incisive® Enterprise Simulator. However, the company lacked a hardware and software co-validation process that could bring greater efficiency to its design process. Instead, the engineers would simulate each segment at the same time, but independently, which led to verification inconsistencies.

"The software," explained Close, "would show up as a compiled binary with very little visibility into what was going on, so it was really painful. We had noticed this gap in our tool suite for months, so we needed a good opportunity to explore new tools."

Because of these gaps, the team found bugs at lower levels of abstraction, when it was so late in the process that the engineers would have to redo aspects of the design to resolve the issues. Melexis needed a methodology to provide more clarity into its design at a much higher level of abstraction, as well as tools that would facilitate true hardware and software co-validation.

The Solution

Melexis had been using Cadence® design tools for years. "What we wanted to do was leverage the best of the existing simulation tool we have—Cadence Incisive Enterprise Simulator—and find out how we could improve it," said Close.

The team had been using Incisive Enterprise Simulator to provide top-level validation and Cadence SimVision Debug, integrated into the simulator, as its unified simulation and debug environment. But there was no visibility into the embedded software. So, the team contacted Cadence, which recommended a trial of the Cadence Incisive Software Extensions embedded software trace plug-in that provides the view into the software side that had been missing. The embedded software trace provides full visibility into the activities of the embedded software right next to the analog IC. Essentially, the team combined hardware/software co-debug with analog/mixed-signal simulation.

"Incisive Enterprise Simulator and the embedded software trace provided a big productivity boost," said Close. "We had a complete framework with a virtual environment to test and debug our system from both the hardware and software sides, and to bring it fully functional at first pass."

The Melexis team also implemented a transaction-level model that captures primary functions of the sensor (hardware or software). Since the model is architecturally accurate, it allows progressive system integration and verification of the implemented blocks, including synthesis-ready RTL, compiled embedded software, and analog transistor-level schematics. This model serves as a "golden reference" and provides a system-level testbench for each subsystem that the Melexis engineers continue to refine during the development process. By accelerating hardware and software co-simulation, the model fosters efficient software debugging.

The transaction-level model is coded in SystemVerilog. With the Verilog family, the team found a common language they could apply at all levels of abstraction in their design:

- SystemVerilog at the transaction level
- Verilog for synthesis-ready digital RTL
- Verilog-AMS for mixed-signal blocks at the behavioral level
- And Verilog and Verilog-A for gate-level and transistor-level netlists

Because Melexis could reuse the same simulator and simulation environment, the company took advantage of verification consistency across all abstraction levels.

The model-based approach that Melexis implemented works well with the Cadence Virtuoso Analog Design Environment, which the company uses for fast and accurate design verification of its custom ICs. With the transaction-level model in place, the company's verification engineers could take advantage of the embedded software trace to pinpoint the source code that is the cause of the discrepancy from the transaction-level golden reference model.

The Results

Thanks to its transaction-level model, Melexis streamlined its design and verification process for its magnetic sensor and replaced what was previously a disjointed process for bug reporting. Now, the engineers can identify and resolve hardware and software problems early on, refine and clarify block-level specifications, and also start top-level integration and test case development early. The model simulates 200X faster than the corresponding RTL, which also prevents late detection of problems and, ultimately, the need for any related redesigns.

According to Close, without the Incisive tools, it would be very difficult for Melexis to fully understand and efficiently debug its system. "With our transaction-level model and Incisive tools, were able to reduce by 15 percent the time required on a 9-month IC development cycle," noted Close. "We also saved about one cycle of metal change."

He added, "Using the Incisive Enterprise Simulator plug-in, we're able to see things in our system that we didn't see before."

Summary and Future Plans

Since its successful trial of its new methodology and Incisive tools, Melexis now applies the same approach to every new project and is continuing to train more engineers on SystemVerilog and on writing models at higher levels of abstraction.

The company also plans to take advantage of some useful tips gleaned from this year's CDNLive EMEA developer conference in Munich, Germany.

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