Virtuoso Integrated Physical Verification System

Enabling higher quality layout, faster

At advanced nodes, traditional design rule checking (DRC) does not scale for layout verification. That's where Cadence® Virtuoso® Integrated Physical Verification System (IPVS) comes in, to bridge the gap and improve productivity between the custom implementation and physical verification tools. With Virtuoso IPVS, you can achieve productivity improvements of at least 15% at mature nodes and more than 50% at advanced nodes.

Dynamic In-Design Signoff DRC

DRC turnaround time (TAT) at advanced nodes has grown exponentially due to the escalating design size and complexity, complex DRCs, higher DRC rule count, complex manufacturing, and multi-patterning coloring rules. Traditional DRC verification flows are post-processing oriented, relying on post-GDSII modifications of the design. Not only do these flows lead to suboptimal results, but they can also induce expensive implement-then-verify iterations between the implementation platform and physical verification tools. At advanced nodes, this step may be repeated for all the mandatory checks. Double-patterning coloring/checks, metal fill insertion, analog/mixed-signal process constraints, and forbidden lithography patterns are all mandatory manufacturability steps at advanced nodes.

Virtuoso IPVS delivers instantaneous signoff DRCs to guide you through a correct-by-construction flow (Figure 1). The tool integrates foundry-qualified PVS DRC rules decks into Virtuoso Layout Suite in an interactive "instantaneous" mode. Layout engineers just click a button and Virtuoso IPVS runs the signoff DRC check on the prescribed area and returns, within seconds, the DRC results as markers in the layout. Figure 2 illustrates some key productivity-enhancing features of the tool.

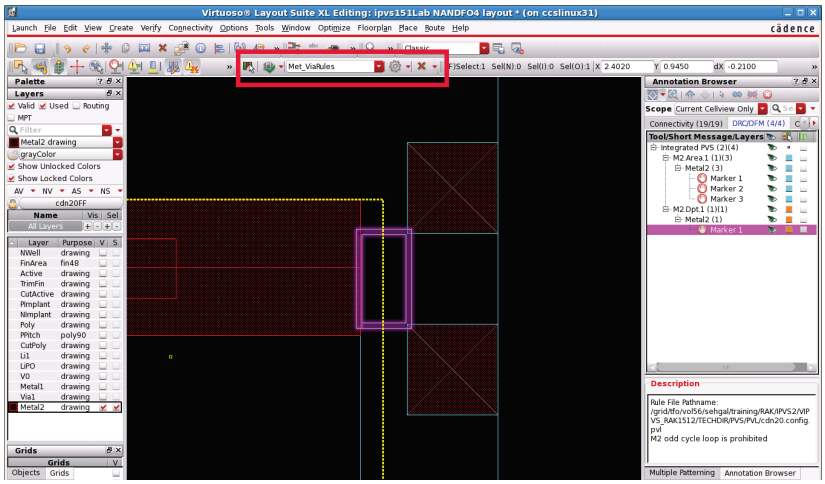

Figure 1: Virtuoso IPVS provides dynamic signoff verification of layouts at advanced nodes.

Accounting for Advanced-Node Challenges

At advanced nodes, you also must account for:

- FinFET design challenges, such as fin width measurements and special fin-to-fin DRC checks for spacing
- Layout coloring and color conflicts that can come with double, triple, and quadruple patterning

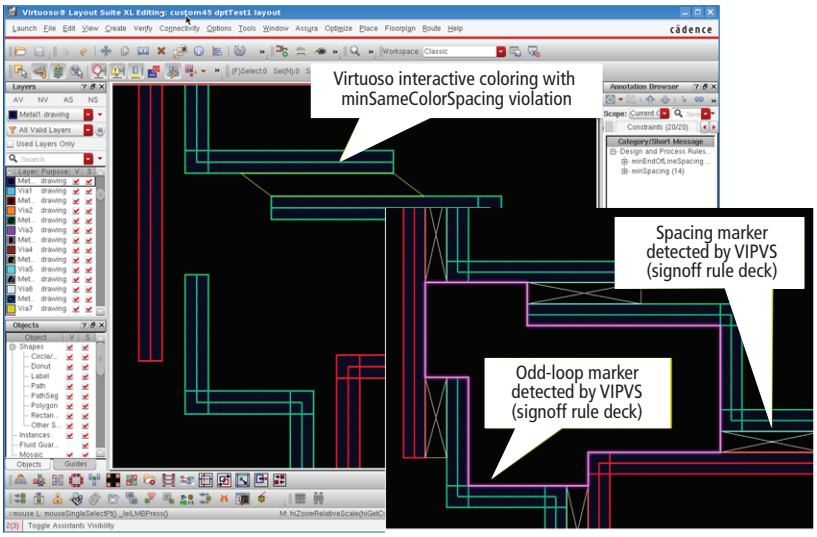

Figure 2: Virtuoso IPVS color decomposition checks and odd loop detection in-situ with Virtuoso native advanced-node coloring.

- Multiple cut and interconnect layers, which bring complex DRCs of spacing sizes and grouping relations
- Complex DFM metal fill and density requirements
- Flow complexities, such as the color checks and/or decomposition required at <=20nm

Virtuoso IPVS revamps the signoff DRC process, removing the need to stream in and out of your design tool and replacing a traditionally iterative, labor-intensive process (Figure 3). The tool:

- Provides precompiled rule sets at the start of your layout session
- Checks changes after each edit or on-demand via a one-button click
- Delivers results in the Virtuoso Layout Suite XL annotation browser or the PVS Results Manager browser
- Uses a foundry-certified PVS rule deck for instantaneous signoff DRC

Benefits

- One-button click for in-design DRC signoff in Virtuoso platform
- In-memory integration, eliminating expensive 'save/load' stream-out/in steps
- Flexibility to easily run selected rule checks
- Reduces total time spent in layout as well as DRC verification re-spins
- Flexibility to debug error markers in the Virtuoso Layout Suite XL annotation browser or with the PVS standalone browser (Figure 4)
- Reduces and restricts expensive signoff license usage to the end for large blocks

Summary

Virtuoso IPVS has helped numerous advanced-node customers reduce signoff DRC runs from several times per hour to a few times per day, improving design quality and reducing silicon area and costly use of expensive signoff licenses. Please contact your Cadence sales representative for more information.

Here's what some of our customers have said about Virtuoso IPVS:

"Without Virtuoso IPVS, it would be very difficult to reach the design target in time and be DRC-clean."

"Combining the power of DRD Notify with the signoff checking of Virtuoso IPVS the designer can achieve maximum productivity at all stages of the design"

"Knowing dynamically the width, spacing, coloring rules gives huge advantages for productivity improvement."

"Virtuoso IPVS allows us to avoid infinite loops among all coloring rules."

"Productivity improvement is largest at the most critical point of the design cycle."

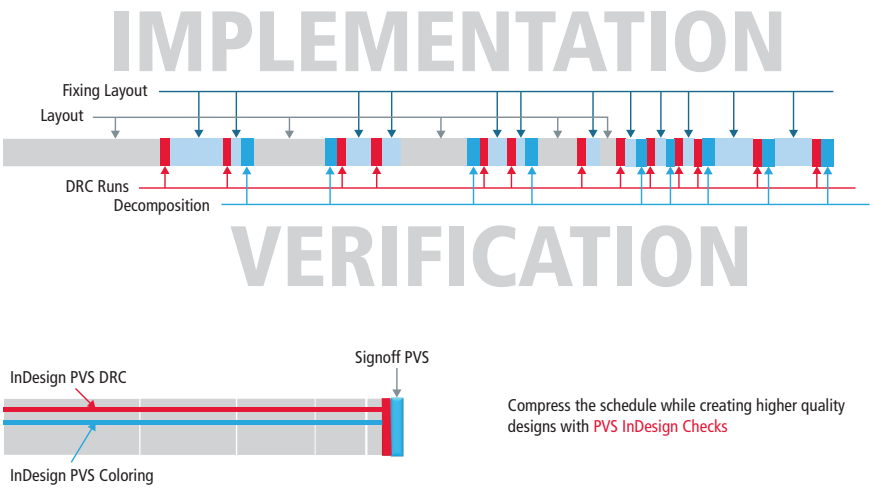

Figure 3: Virtuoso IPVS revamps the signoff DRC process, compressing the schedule while creating higher quality designs

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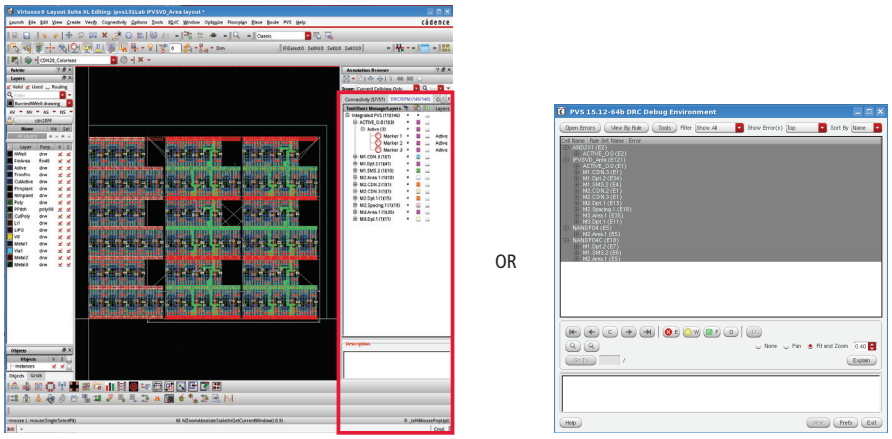

Annotation Browser PVS Results Manager Browser

Figure 4: View and analyze DRC errors in the Virtuoso annotation browser or in the PVS Results Manager

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