Moore's Law Is Still Accelerating

Hyperscalers, mobile, and automotive companies are pushing the pace of advanced nodes

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There has been much said about the slowing, or even ending, of Moore's Law. But I'm here to say that Moore's Law is still accelerating. The semiconductor industry isn't giving up so easily, and the pace of innovation is faster than ever. The concept of "More than Moore" or redefining the goal from chip-specific gains to system-specific gains is also legitimate. Semiconductor foundries and EDA partners have made tremendous strides in the past five years, speeding innovation, building fabs, and improving yield faster than ever before.

So how can I justify my claim? I'm looking at Moore's Law differently, measuring the pace of new node arrivals. Let's look at the major nodes: 28nm, 16nm, 7nm, and now 3nm. We can see that the node-to-node transitions have accelerated from a three-year pace (from 28nm to 16nm) to a one-and-a-half to two-year pace (from 7nm to 5nm). And the transition from 5nm to 3nm occurred faster than ever as we now see 3nm rapidly approaching readiness. Cadence is a key part of this exciting journey.

Cadence is at the forefront of the transition to 3nm, actively working with early adopter customers to enable them in designing and taping out their advanced 3nm SoCs. These customers are led by the hyperscalers, the internet titans who are transforming our daily lives and driving the electronics industry. The insatiable demand for faster and faster cloud computing necessitates the move to the most advanced process technologies as soon as they are available. We are seeing this major market disruption playing out and the inter-dependency between supply-side and demand-side. Chip companies (fabless included) used to drive the early adoption of the newest advanced process nodes.

For example, CPUs, FPGAs, applications processors, and wireless modems were high volume and gained economic advantage from the smaller area, lower power, and higher performance of the new node. With the advent of cloud computing and artificial intelligence / machine learning (AI/ML) acceleration and computation, very large revenues are generated by providing cloud computing resources with next-generation compute performance facilitated by custom processors. These titans are investing in custom silicon by designing and optimizing the data center infrastructure for special workloads and are now bringing chip development in-house to support demands beyond what off-the-shelf chips can offer.

These industry leaders are also adopting the most advanced process technology they can get their hands on at the earliest opportunity. Similarly, smartphone manufacturers are also early adopters of advanced process nodes to deliver their next-generation products that support higher resolution display and cameras, better connectivity, longer battery life, and better usability and user experience. The result is that smartphones and high-performance computing are now the two largest segments of semiconductor consumption and the main drivers for 3nm technology adoption. If it weren't for smartphone application processors and hyperscale computing applications,

Moore's Law would likely still be focused on 7nm and maybe ramping up on 5nm.

To make all this possible, we are working with the foundries who have been investing aggressively, and we are now seeing the fruits of those investments. We have developed 3nm support in our design tools, now certified by leading foundries and used by our lead customers and our IP team. To meet the design challenges at 3nm—and there are many—we entered a three-way collaboration with these lead customers and the foundries to ensure success. For engineering teams working on 3nm design, this is very important, but it's most impactful for companies that are more vertically oriented and own the whole stack—from the firmware that will be written on the device to what the device is actually going to be. That way, they are able to achieve more when optimizing that whole system. The bigger the solution space, the bigger the set of variables to work with and the bigger the impact produced.

As a leading supplier of high-performance IP, we have been called upon to enable key IP in 3nm designs to support hyperscale computing applications. Such IP include a 112G SerDes switch SoC to support 400G networks, advanced memories including DDR5, LPDDR5/5X, and GDDR6, as well as high-speed protocols such as PCI Express® (PCIe®) 5.0/6.0 and CXL for systems that are sharing coherent memory and cache and establishing multi-host peer-to-peer connections.

3nm is at the vanguard of a renaissance in semiconductors, critical for servers, laptops, and smartphones. Cadence is investing heavily in semiconductor and system implementation technology. We have been developing computational software for over 30 years, now executing on our Intelligent System Design™ strategy. This calls for increased productivity, scalability, and quality of chip design to serve new consumer markets, enhance the internet infrastructure, and champion the continuously evolving semiconductor technology. We have a deep bench of technologists—knowledgeable in semiconductor technologies, device physics, reliability, simulation, chip layouts, packaging, and innovative computational strategies that we bring to bear to solve these big challenges. We are excited to be at the forefront of digital implementation and signoff technology advancement and to be playing a role in shaping the overall semiconductor industry and beyond. We are truly witnessing the dawn of a new renaissance in the semiconductor industry.