## **OrCAD** Tutorial

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## **Tutorial Overview**

This tutorial enables you to evaluate the power of the OrCAD tools for the PCB design process. You can run through the steps to perform the basic tasks in the PCB design process in sequence.

You will start with capturing the circuit diagram in Capture, followed by circuit simulation using PSpice, through to the PCB layout stages, and finally, complete the design cycle by generating the manufacturing output.

This document does not cover all the features of a tool. It only highlights the tasks that you need to perform in each OrCAD tool so that your design works smoothly through the flow.

### Audience

This tutorial is useful for a:

- Designer who wants to use OrCAD tools for the complete PCB design flow or for analog and digital simulation flow.
- First-time user of OrCAD Capture, PSpice, and OrCAD PCB Editor.

### Using the tutorial

To run through the complete tutorial, you need the following tools:

- OrCAD Capture CIS
- PSpice AD
- OrCAD PCB Editor

All these tools are available with the OrCAD PSpice Designer and CIS license.

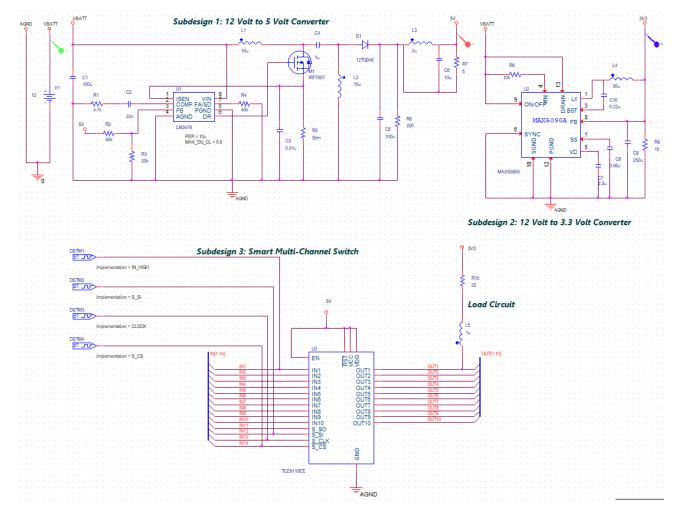
#### Sample Design

The design created by the end of this tutorial is available at the following location:

<17.4\_installation\_directory>\share\orcad\tutorial\tutorial.opj

## **Creating a Schematic Design**

In this chapter, you will create a schematic design for a fan-control module as shown in the following figure.



#### Figure 2-1 Schematic design for the complete fan-control module

As shown in Figure 2-1 on page 7, there are three subdesigns in this fan module. The Table 2- $\underline{1}$  on page 8 explains the function of each subdesign.

#### Table 2-1 Subdesigns in the fan module circuit

Subdesign	Function of this subdesign
Subdesign 1	A step-down DC-DC converter. It uses IC LM3478, a low-side n-channel MOSFET controller for switching regulators, which converts 12 volt to 5 volt.
	The output of 5 volts is the internal power supply for this circuit. It provides supply voltage to IC TLE8110EE (in subdesign 3).
Subdesign 2	A step-down DC-DC converter that uses the IC MAX5090A to convert 12 volt to 3.3 volt.
Subdesign 3	A smart multi-channel switch, TLE8110EE that is powered by 5 volt supply.
	This switching IC, TLE8110EE can control multiple load types (fan load in this tutorial). It has input 10 channels and a serial peripheral interface (SPI). It has 10 output pins, which can control up to 10 fans.

### **Creating a New Project**

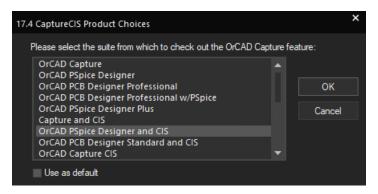
A project file (.OPJ) is a container for the design file (.DSN). In addition, a project file also includes simulation profile and layout information.

To create a new project, do the following:

1. From the Start menu, select *Capture CIS 17.4*.

The 17.4 CaptureCIS Product Choices dialog box opens.

Figure 2-2 Product Choices window



2. Select OrCAD PSpice Designer and CIS.

The OrCAD Capture CIS window opens.

- 3. Select File New Project.
- 4. In the New Project dialog box, specify the project name as tutorial.
- **5.** Specify the location where you want the project files to be created.

For this tutorial, specify the location as: C:\OrCAD\_Tutorial

6. Select Enable PSpice Simulation.

Figure 2-3 New Project window

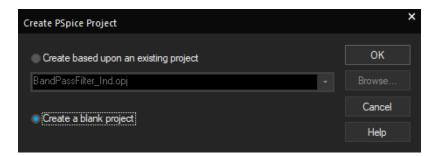
New Project				×
Name	tutorial			
Location	C:\OrCAD_Tutorial			
	Enable PSpice Simulation	n		
		ОК	Cancel	Help

**7.** Click *OK*.

The Create PSpice Project dialog box appears.

8. Select Create a blank project.

#### Figure 2-4 Create PSpice Project window

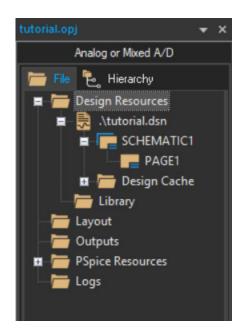


When you create a blank project, the project can be simulated in PSpice, but libraries are not configured by default. When you base your project on an existing project, the new project has same configured libraries.

**9.** Click *OK*.

The tutorial project is created. In the project manager window, a design file, tutorial.dsn, is created. Below the design file, a schematic folder with the name SCHEMATIC1 is created. This folder has a schematic page named PAGE1.

Figure 2-5 Project Manager window



**10.** Select *Options – Schematic Page Properties*, and choose the page size as B.

### **Creating the Design in Capture**

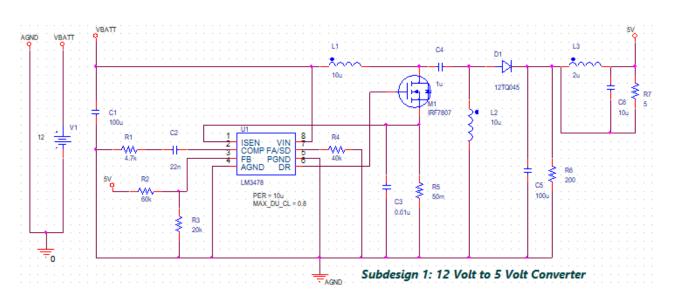
You will now create the three subdesigns of the fan module as shown in Figure 2-1 on page 7.

Subdesign No.	Instructions for subdesign creation are in the section
1	Adding 12 Volt to 5 Volt Converter
2	Adding 12 Volt to 3.3 Volt Converter
3	Adding Smart Multi-Channel Switch Circuit

#### Adding 12 Volt to 5 Volt Converter

Subdesign 1 shown in Figure 2-6 on page 12 has two parts, 12 volt main power supply and 12 volt to 5 volt converter.





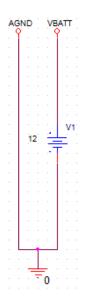
#### Part 1: Create the circuit for 12 volt main power supply

Perform the following tasks to create the circuit for the main power supply:

- 1. Placing DC voltage source (V1) using Modeling Application
- 2. Placing ground symbols

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- 3. Adding and placing power ports
- 4. Connecting the components
- Figure 2-7 Subdesign 1A: Main power supply



#### Placing DC voltage source (V1) using Modeling Application

1. Select *Place – PSpice Component – Modeling Application*, or click the Launch Modeling Application icon (

The Modeling Application pane opens.

- 2. Select Sources Independent Sources.
- **3.** Click *DC*.
- 4. Select Voltage and Ideal DC.
- 5. Specify the value of the voltage as 12 volts.



Independent Sources	×
Pulse Sine <b>DC</b> Exponentia	al FM Impulse Three Phase Noise
O Voltage O Current	
O Ideal DC ODC	
Parameter Name Parar	meter Value
DC Voltage 12	x
	VDe IDEAL DC Waveform
	Place Close Help

6. Click Place.

The PSpice component is attached to a pointer.

- 7. Click to place the component as required.
- 8. To save the design, select *File Save* or press *CTRL+S*.

#### Placing ground symbols

- **1.** Select *Place PSpice Component PSpice Ground*.
- 2. Click the schematic page to place the part.
- 3. Right-click and select *End Mode* or press *Esc*.

#### Adding and placing power ports

Place a power port, VCC with its value set to VBATT, and anther one with its value set to AGND from the CAPSYM library. To do so:

- 1. Select *Place Power*, press *F*, or click the Place power icon ( ) on the Draw Electrical toolbar.
- **2.** Select CAPSYM from the *Libraries* list box.
- **3.** Select VCC from the *Symbol* list box.
- 4. Click OK.
- 5. Click the schematic page to place this power port above the 12 volt DC source.
- 6. Double-click VCC to open the Display Properties dialog box.
- 7. Specify the *Value* as VBATT and click *OK*.
- 8. Repeat steps 1 through 7 to add another power port, VCC, and set its value to AGND.

#### Connecting the components

1. Select *Place – Wire,* press *W*, or click the Place wire icon (**[**]) on the Draw Electrical toolbar.

The pointer changes to a crosshair.

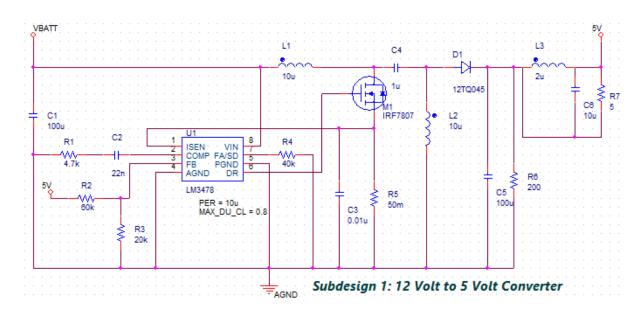
- 2. Draw the wire from the connection point of port AGND, PSpice ground, 12 volt DC voltage source, to the VBATT port.
- 3. Click any valid connection point to end the wire.

#### Part 2: Create the circuit for 12 volt to 5 volt converter

Perform the following tasks to create the circuit for the 12 volt to 5 volt converter:

- 1. Placing the DC-DC converter IC LM3478
- 2. Placing the MOSFET IRF7807
- 3. Placing the ports
- 4. <u>Placing the discrete components</u>
- 5. Changing the value of discrete components
- 6. Example Placing the 100u Capacitor, C1
- 7. Placing the remaining components in subdesign 1
- 8. <u>Connecting all the components in subdesign 1</u>

#### Figure 2-9 Subdesign 1B: 12V to 5V converter



#### Placing the DC-DC converter IC LM3478

1. Select *Place – PSpice Component – Search*, or click the Launch Part Search icon () on the PSpice toolbar.

The PSpice Part Search pane opens.

- **2.** Specify LM3478 in the search text box and press *Enter*.
- **3.** Right-click LM3478 from the search results and select *Place Symbol*.
- 4. Click the schematic page to place the converter IC.
- 5. Right-click and select *End Mode* or press *Esc*.
- 6. Double-click PER and set its value to 10u.

This value is modified because it sets the frequency of this IC. Changing the value to 10u (1/10u = 100KHz) means setting the IC frequency to 100 KHz.

#### Placing the MOSFET IRF7807

1. Select *Place – PSpice Component – Search*, or click the Launch Part Search icon (

The *PSpice Part Search* pane opens.

- **2.** Specify IRF7807 in the search box and press *Enter*.
- **3.** Right-click IRF7807 from the search results and select *Place Symbol*.
- 4. Click the schematic page to place the MOSFET.

#### Placing the ports

Place the VBATT and the two 5V power ports shown in subdesign 1 (Figure 2-9 on page 16) using the steps listed in the section, Adding and placing power ports.

#### Placing the discrete components

To place the commonly used discrete components, capacitor, inductor or resistor, do the following:

- 1. Select Place PSpice Component Capacitor.
  - OR

Select Place – PSpice Component – Inductor.

OR

Select Place – PSpice Component – Resistor.

The part symbol is attached to a pointer.

- 2. Click the schematic page to place the required component.
- 3. To stop placing the components, right-click and select *End Mode* or press *Esc*.

#### Changing the value of discrete components

**1.** Double-click the value of any discrete component.

The Display Properties window opens.

- 2. In the Value field, specify the required value of the discrete component.
- 3. Click OK.

#### Example - Placing the 100u Capacitor, C1

**1.** Select *Place – PSpice Component – Capacitor*.

- 2. Click the schematic page to place the capacitor C1 below the VBATT port as shown in Figure 2-9 on page 16.
- **3.** Right-click and select *End Mode* or press *Esc*.
- 4. Double-click the value, 1n.

The Display Properties window opens.

- 5. In the Value field, specify the value of C1 as 100u.
- **6.** Click *OK*.

#### Placing the remaining components in subdesign 1

1. Place the remaining discrete components in subdesign 1 (Figure 2-9 on page 16) using steps listed in section, <u>Placing the discrete components</u> and specify their value using steps from the section, <u>Changing the value of discrete components</u>.

PSpice Component Name	PSpice Component Value
C2	22n
R1	4.7k
R2	60k
R3	20k
R4	40k
L1	10u
C3	0.01u
C4	1u
R5	50m
L2	10u
C5	100u
R6	200
L3	2u
C6	10u
R7	5

- 2. Place the 12TQ045 diode using the PSpice Part Search window. For steps, see the section, Placing the DC-DC converter IC LM3478.
- 3. Place the AGND port using the steps listed in the section, Adding and placing power ports.

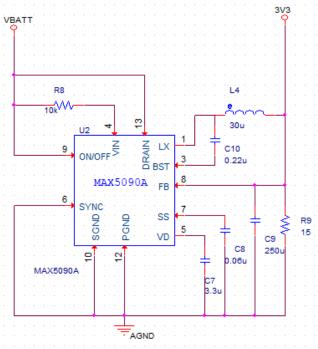
#### Connecting all the components in subdesign 1

- **1.** Draw wire from pin 1 of LM3478 to source of MOSFET M1, IRF7807.
- 2. Draw wire from pin 6 LM3478 to the gate of MOSFET M1, IRF7807.
- **3.** Draw wire from 10u inductor, L1 to the drain of MOSFET M1, IRF7807.
- **4.** Similarly, add wires to the subdesign 1 until all components are connected as shown in the Figure 2-9 on page 16.

#### Adding 12 Volt to 3.3 Volt Converter

The subdesign 2 of the fan module uses IC MAX5090A, which is a DC-DC converter that is down converting 12 volt to 3.3 volt. The output of 3.3 volt powers the fan.





Subdesign 2: 12 Volt to 3.3 Volt Converter

To create subdesign 2, do the following:

- 1. Place the DC-DC converter, MAX5090A.
  - a. Select *Place PSpice Component Search*, or click the Launch Part Search icon (

The *PSpice Part Search* pane opens.

- **b.** Specify MAX5090A in the search box and press *Enter*.
- c. Right-click MAX5090A from the search results and select Place Symbol.
- d. Click the schematic page to place this converter.
- **2.** Place the VBATT, AGND, and 3V3 power ports shown in subdesign 2 (Figure 2-10 on page 20) using the steps listed in the section, <u>Adding and placing power ports</u>.

**3.** Place the remaining discrete components in subdesign 2 (in <u>Figure 2-10</u> on page 20) using the steps listed in the section, <u>Placing the discrete components</u> and specify their value using steps from the section, <u>Changing the value of discrete components</u>.

PSpice Component Name	PSpice Component Value
L4	30u
C10	0.22u
R8	10k
C7	3.3u
C8	0.06u
С9	250u
R9	15

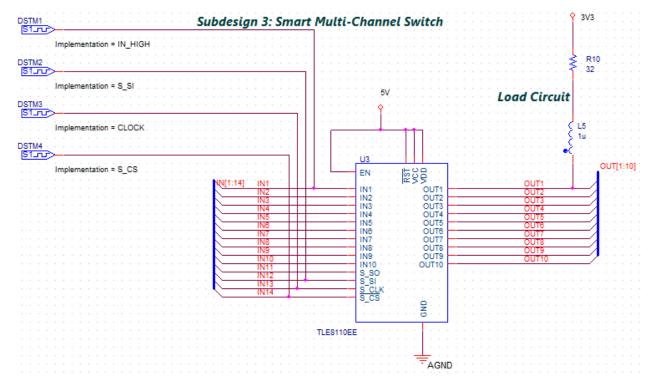
- **4.** Right-click C8 and select *Edit Properties*. Set value of *IC* as 0.
- 5. Add wires to the subdesign 2 until all components are connected as shown in Figure 2-10 on page 20.

#### Adding Smart Multi-Channel Switch Circuit

In subdesign 3, you will create the circuit for a smart multi-channel switch as shown in <u>Figure 2-11</u> on page 22.

In this subdesign, IC, TLE8110EE is placed to be interfaced with an off-board microcontroller. This means that the input to the 10 channels of this IC are digital signals generated from a micro-controller. For this tutorial, these digital signals are modeled using digital stimulus sources.





Perform the following tasks to create subdesign 3:

- 1. Placing components of subdesign 3
- 2. Placing and connecting buses in subdesign 3
- 3. Connecting components of subdesign 3

#### Placing components of subdesign 3

**1.** Place the IC, TLE8110EE using *PSpice Part Search*.

To go through the steps, see Placing the DC-DC converter IC LM3478.

2. Place the AGND, 5V, and 3V3 power ports shown in subdesign 3 (Figure 2-11 on page 22).

To go through the steps, see Adding and placing power ports.

**3.** Place the discrete components in subdesign 3 (<u>Figure 2-11</u> on page 22) using the steps listed in the section, <u>Placing the discrete components</u> and specify their value using steps from the section, <u>Changing the value of discrete components</u>.

PSpice Component Name	PSpice Component Value
R10	32
This resistor forms the RL circuit for the fan type of load.	
L5	1u
This inductor forms the RL circuit for the fan type of load.	

4. Place the digital stimulus sources using *PSpice Part Search*.

These are 1-bit digital stimulus sources.

To add these, search for  $\tt DIGSTIM1$  in PSpice Part Search and select  $\tt DigStim1$  from the results.

5. Double-click the Implementation property of a digital stimulus source.

The Display Properties window opens.

6. In the *Value* field, specify the value of this Implementation property as shown in the following table:

Digital Stimulus Source Name	Value of Implementation property
DSTM1	IN_HIGH
DSTM2	S_SI
DSTM3	CLOCK
DSTM4	S_CS

Note: The stimulus data from these sources is read from a .stl file, which will be

created and configured in Chapter 3, "Simulating a Design,".

#### Placing and connecting buses in subdesign 3

1. Select *Place – Bus*, press *B*, or click the Place bus icon ( ) on the Draw Electrical toolbar.

The pointer changes to a crosshair.

- 2. Draw the bus before the input pins and after the output pins of TLE8110EE as shown in Figure 2-13 on page 25.
- **3.** Select *Place Net Alias*, press *N*, or click the Place net alias icon (

The Place Net Alias dialog box appears.

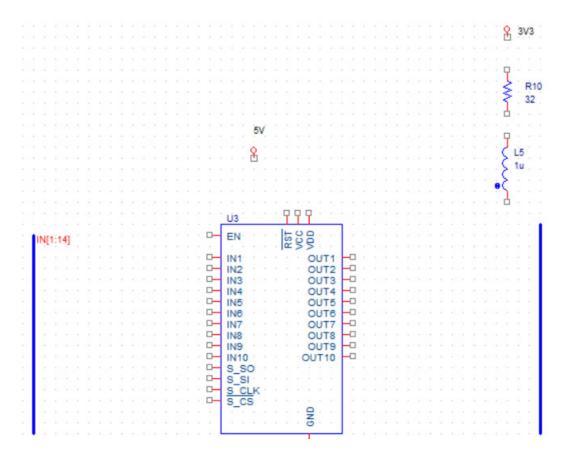
**4.** Specify the value in the *Alias* field as IN[1:14].

Figure 2-12 Place Net Alias window

Place Net Alias		×
Alias:		ОК
IN[1:14]		Cancel
		Help
Color Default	Rotation 0 90 1	80 270
Font Change Use Default	Arial 7 (default)	
NetGroup ☐ NetGroup Aware Aliases		•

- 5. Click OK.
- 6. Move the cursor on the bus and place the net alias name as shown in the following figure.

#### Figure 2-13 Placing bus and specifying net alias



7. Select all the input pins of TLE8110EE (except EN), right-click the selection, and choose Connect to Bus.

The pointer changes to a crosshair.

8. Click the bus placed before the input pins.

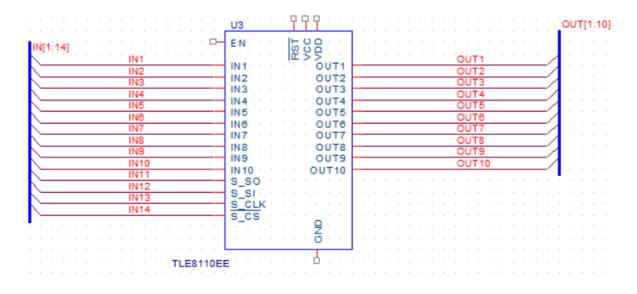
The Enter Net Names window appears.

Enter Net Names	?	×
Pins Selected :	14	
IN[1:14]		
ОК	Cancel	

**9.** Click *OK*.

Net names appear on each net from the input pins to the bus as shown in <u>Figure 2-14</u> on page 26.

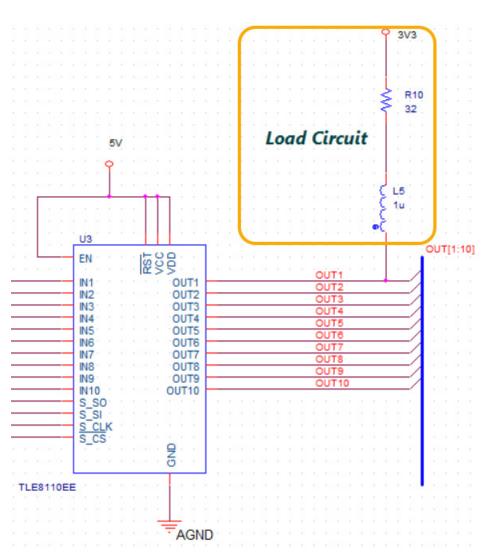
**10.** Repeat steps 3 thorough 10 to place the OUT[1:10] net alias on the bus placed next to the output pins of TLE8110EE, and to connect the output pins of TLE8110EE to this bus as shown in the following figure.



#### Figure 2-14 Connecting bus with pins

#### Connecting components of subdesign 3

- **1.** Draw a wires from the pins, RST, VCC, and VDD to the 5V power port.
- 2. Draw a wire from the 5V power port to the input pin, EN of TLE8110EE.
- **3.** Draw a wire from the GND pin to the power port, AGND.
- 4. Draw a wire from the output pin of:
  - DSTM1 (with implementation=IN\_HIGH) to net IN1.
  - □ DSTM2 (with implementation=S\_SI) to net IN12.
  - DSTM3 (with implementation=S\_CLK) to net IN13.
  - DSTM4 (with implementation=S\_CS) to net IN14.
- 5. Connect the load circuit to the net, OUT1 as shown in the following figure.



#### Figure 2-15 Connecting the load circuit

### Summary

This chapter covered the steps for creating schematic design using OrCAD Capture. In the process, you were introduced to basic design creation tasks, such as creating project, placing parts, editing property values, and connecting parts.

#### OrCAD Tutorial Creating a Schematic Design

## Simulating a Design

In this chapter, you will use PSpice to simulate the design created in <u>Chapter 2, "Creating a</u> <u>Schematic Design,"</u> using OrCAD Capture. You will also learn about the transient analysis that can be performed using PSpice.

### **Getting the Design Ready for Simulation**

To simulate a design, the PSpice simulator needs information about circuit topology, analysis type, and stimulus definitions.

The analysis type, stimulus definition, and the information related to the initial digital state of the simulation is provided by a simulation profile (\*.SIM). In the following section, you will create a simulation profile.

#### Prerequisite to Simulation Setup

Before creating the simulation profile, you need to specify the stimulus definition to be used for simulating the circuit. For this, you need to create a stimulus file and then specify its location in the Simulation Setting dialog box (used to create the simulation profile). To create the stimulus file, copy the following information in a text editor (.txt) file and save it as stimulus.stl.

```
.STIMULUS IN_HIGH STIM (1, 1)
+ 0 0
+ +0 1
.STIMULUS S_SI STIM (1, 1)
+0ms 0
+808.40000000u 0
+ +200ns 1
+ +200ns 1
+ +200ns 1
+ +200ns 0
+ +200ns 0
+ +200ns 0
+ +200ns 1
+ +200ns 0
.STIMULUS CLOCK STIM (1, 1)
+ 0 0
+ +0 1
+REPEAT FOREVER
+ +100n 0
 +100n 1
+
+ ENDREPEAT
.STIMULUS S_CS STIM (1, 1)
+0u 0
+807.763636u 1
+808.333363636u 0
+811.56335227u 1
+812.13370351u 0
```

#### **Creating a New Simulation Profile**

To view the behavior of this circuit over time, transient analysis will be used. To perform this analysis, you will specify this analysis type when creating the simulation profile.

To create a new simulation profile, do the following:

Select PSpice – New Simulation Profile, or click the New Simulation Profile icon (
 ) on the PSpice toolbar.

The New Simulation dialog box opens

- 2. Specify the name of the new simulation profile as TRAN.
- 3. In the Inherit From drop-down list, ensure that none is selected and click Create.

The Simulation Setting dialog box appears with the *Analysis* tab selected.

- **4.** In the *Analysis Type* drop-down list, Time Domain (Transient) is selected by default. Retain this default setting.
- 5. Specify the following options to run a transient analysis.
  - □ In the *Run To Time* text box, specify the time as 1ms.

#### Figure 3-1 Simulation Setup - Analysis tab

Simulation Settings - tran						×
Simulation Settings - tran General Analysis Configuration Files Options Data Collection Probe Window	Analysis Type: Time Domain (Transient) Options: General Settings Monte Carlo/Worst Case Parametric Sweep Temperature (Sweep) Save Bias Point Load Bias Point Save Check Point Restart Simulation	Run To Time : Start saving da Transient opti Maximum Ste Skip initial Run in resu	ons: p Size transient bia	1ms 0 as point calcular	seconds	ile Options
			ок	Cancel	Apply	Help

- 6. In the *Options* tab:
  - **D** To prevent any convergence issues, increase the tolerance to 1n. To do so:

Set ABSTOL as 1n.

	7			
Analog Simulation	Name	Value	Default Value	
General	SPEED_LEVEL	3	▼ 3	
Auto Converge	RELTOL	0.001	0.001	
MOSFET Option	VNTOL	1.0u	1.0u	
	ABSTOL	1.0n	1.0р	
Analog Advanced	CHGTOL	0.01p	0.01p	
General	GMIN	1.0E-12	1.0E-12	
Bias Point	ITL1	150	150	
Transient	ITL2	20	20	
Gate Level Simulation	ITL4	10	10	
General	TNOM	27.0	27.0	
	THREADS	0	0	
Advanced	ADVCONV			
Output File				
General				

#### Figure 3-2 Simulation Setup - Options tab

To set the initial digital state of the simulation to 0, make the following modification:
 Set *DIGINISTATE* as 0.

Analog Simulation	Name	Value		Default Value
General	DIGMNTYMX	Typical		Typical
Auto Converge	NOPRBMSG			
MOSFET Option		0	•	X
Analog Advanced	DIGIOLVL	1		1
General				
Bias Point				
Transient				
General				
Advanced				
Output File				
General				

- 7. In the Configuration Files tab, select Stimulus from Category list.
- 8. Click the *Browse* button to navigate to the stimulus.stl file.

Simulation Settings - tran							
General	Category:	Filename:					
Analysis	Stimulus	C:\OrCAD_Tutorial\stimulus.stl					Browse
Configuration Files	Library Include	Configured File	25		× +	÷	
Options							Add as Global
Data Collection							Add to Design
Probe Window							Add to Profile
							Edit
							Change
			OK	Cancel	Apply	Rese	t Help

#### Figure 3-3 Simulation Setup - Configuration Files tab

- 9. Click the Add to Design button.
- **10.** Click *OK* to save your modifications and to close the dialog box.

When the simulation is run from the schematic, the simulator reads the SPICE models connectivity information (netlist) from the design files, and the analysis type and the stimulus details from the simulation profile.

### **Running the Simulation**

To simulate the design, choose PSpice – Run or click the Run PSpice icon ().



The Schematic1-TRAN - PSpice window opens.

### Viewing Output Waveforms

To visualize the circuit behavior and determine the validity of your circuit design, you can plot the output waveforms in the Probe window. By analyzing the output waveforms you can evaluate your circuit for performance.

For PSpice to display output waveforms in the Probe window, you need to place markers in your circuit design in Capture to indicate the points where you want to see simulation waveforms displayed in PSpice.

Markers can be placed:

- before simulation to limit results written to the waveform data file, and automatically display those traces in the active Probe window.
- during or after simulation, to automatically display traces in the active Probe window.

To add markers:

Choose *PSpice – Markers* or use the icons provided on the PSpice toolbar.

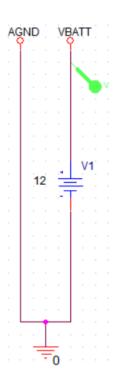
### Important

To view the markers in the simulation results, the schematic design must be open.

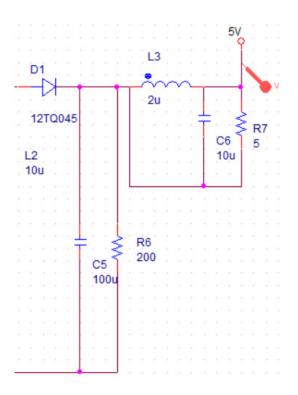
You will now add Voltage markers to view the output waveforms in the Probe window. To do SO:

1. <u>Select PSpice – Markers – Voltage Level</u>, or click the Voltage/Level Marker icon on the PSpice toolbar.

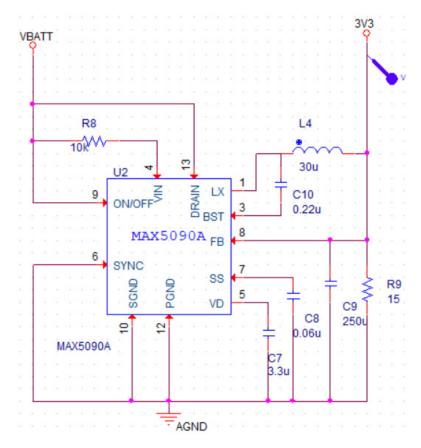
2. Place the marker at the main power supply, that is at the 12 Volt VBATT power net.



**3.** Place the marker at the end of the first subdesign (12V to 5V converter), that is at the 5V power net, as shown in the following figure.



**4.** Place another voltage marker at the end of the third subdesign (12V to 3.3V converter), that is at the 3V3 power net, as shown in the following figure.



**Note:** If you add markers before simulating the design, the output waveforms are displayed automatically in the Probe window after the simulation is complete.

5. To view the output waveform at the marker location, double-click the marker.

The output waveform appears in the Probe window in PSpice as shown in the following figure.

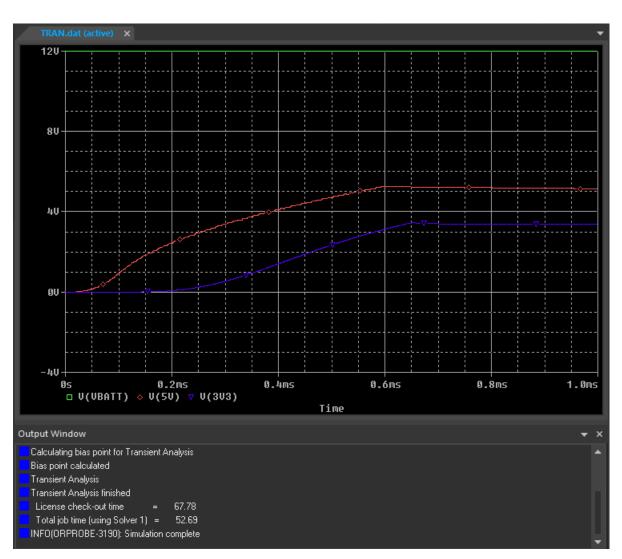
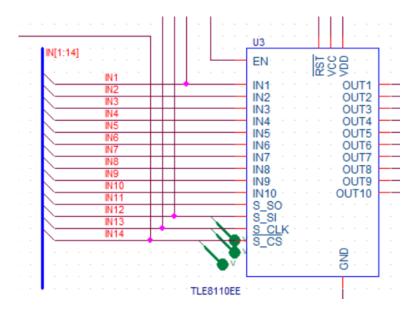


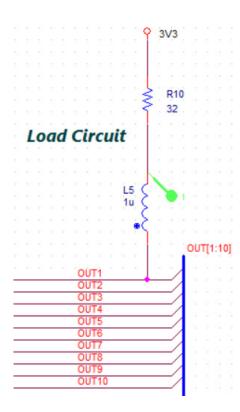
Figure 3-4 Output Waveform - Probe window

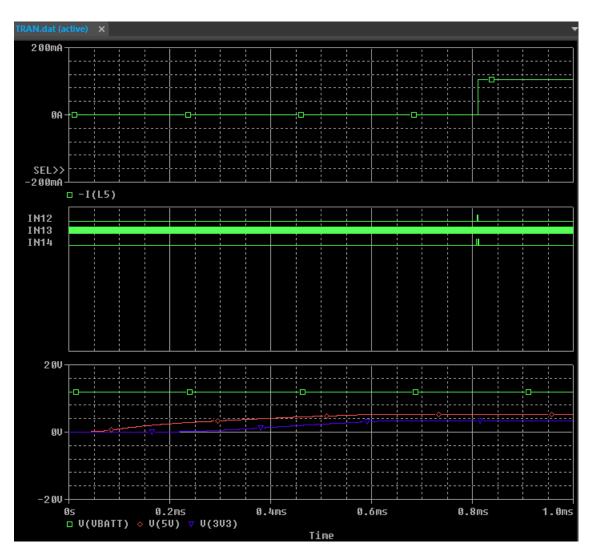
- **6.** To view the waveform of the digital stimulus sources at the input of the switching IC TLE8110EE, place voltage markers on the following nets:
  - □ IN12 (connected to pin S\_SI)
  - □ IN13 (connected to pin S\_CLK)

 $\hfill\square$  IN14 (connected to pin S\_CS)



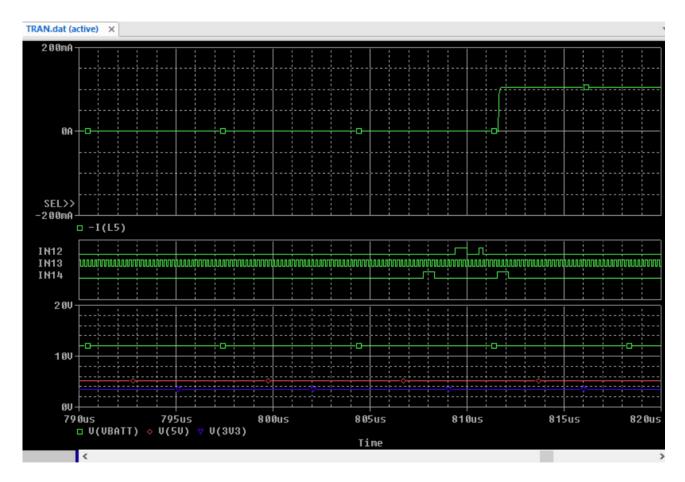
- 7. In PSpice, select Plot Add Plot to Window.
- 8. In Capture, place a current marker (using the Current Marker icon, ) on the pin of the inductor as shown in the following figure.





The changes in the waveform are displayed in the following figure.

The command to turn on the fan is sent to the  $S\_SI$  pin. This command is read and executed at the low to high transition of the  $S\_CS$  signal. The input signal through the  $S\_SI$  pin is sent from the duration 808us to 811us, as shown in the following figure.



# Summary

This chapter covered the steps for simulating the fan module design using OrCAD PSpice. In this chapter, you were introduced to various tasks involved in the simulation process, such as creating a simulation profile, running simulation, placing markers, and analyzing simulation results.

### OrCAD Tutorial Simulating a Design

# **Preparing for PCB Layout Creation**

Now that you have verified the performance of your logical circuit through simulations, you can start designing the physical layout of the PCB board for this schematic design.

Before you create the PCB layout for this schematic design, you need to ensure that the design has no open or unconnected signal, footprint information is available for all components, and electrical constraints, if any, are specified.

# **Adding and Placing Connectors**

To connect the fan module with a system, connector components are required to be placed in the schematic design.

To add and place connectors in this schematic design, do the following:

- 1. Open Capture.
- 2. Select Place Part, press P, or click the Place part icon (

The *Place Part* pane opens.

3. To add Connector.olb to the project, click the Add Library icon (

The Browse File dialog box opens.

4. Browse to

<installation\_directory>\tools\capture\library\Connector.olb.

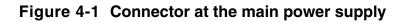
5. Select Connector.olb and click *Open*, or double-click Connector.olb.

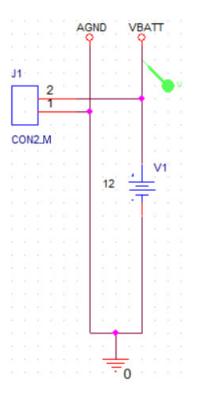
The CONNECTOR library appears in the *Libraries* list box.

- 6. Search for CON2\_M from the *Part* list box.
- 7. Click the *Place Part* icon (

The part symbol is attached to the pointer.

- 8. Click the schematic page where you have placed the 12 volt DC source and place the connector J1.
- 9. Right-click and select *End Mode* or press *Esc*.
- **10.** Right-click this connector and select *Rotate* and the connect it as shown in <u>Figure</u> on page 44.





Similarly, add a 14-pin connector ( $CON14_M$ ) to the input and output channels of the smart multi-channel switch IC.

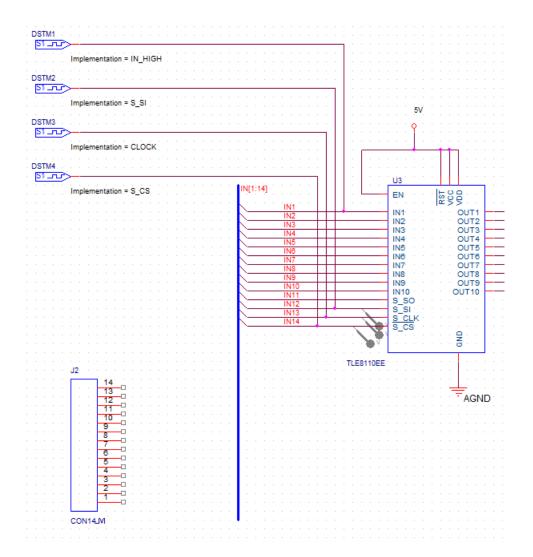
To add the connectors in the smart multi-channel switch circuit, do the following:

- 1. In the *Place Part* pane, search and select CON14\_M from the *Part* list box.
- 2. Click the *Place Part* icon ( ) or press *Enter*.

The part symbol is attached to a pointer.

- **3.** Click the schematic page before the IC TLE8110EE and place the connector J2 as shown in Figure 4-2 on page 45.
- 4. Right-click J2 and select Rotate.

**5.** Extend the bus before the input pins of TLE8110EE as shown in Figure 4-2 on page 45.



#### Figure 4-2 Placing connector, J2

6. Select all the pins of connector  $J_2$ , right-click the selection, and choose *Connect to Bus*.

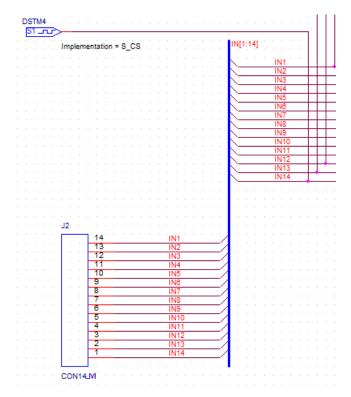
The pointer changes to a crosshair.

7. Click the bus that you had extended in step 5.

The Enter Net Names window appears.

8. Click *OK*.

Net names appear on each net from the connector pins to the bus.



### Figure 4-3 Connecting J2 to bus at the input of TLE8110EE

- **9.** Similarly, place another connector J3 and do the following:
  - **a.** Connect its first 10 pins as shown in Figure 4-4 on page 47.
  - **b.** Click the No Connect icon ( ) or press *X*, and connect it to pins 11 and 12 of connector J3.
  - c. Connect 3V3 and 5V power ports to pins 13 and 14 of connector J3.

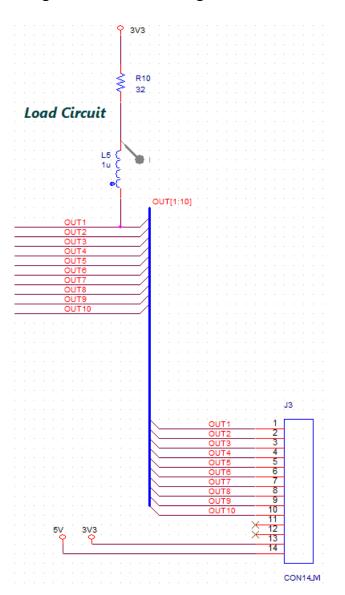


Figure 4-4 Connecting J3 to bus at the output of TLE8110EE

### **Updating Footprints**

As the first step, update footprint associated with all the resistors in the design.

### **Updating Footprints associated with Resistors**

To assign footprints to all the resistors, do the following:

1. Select Edit – Find or press CTRL+F.

The Find pane appears.

- 2. Specify part reference=R\* in the Find what field.
- 3. Select the Parts check box under Find in.
- 4. Select the *Property Name=Value* check box under *Find options*.

#### Figure 4-5 Specifying search criteria in Find pane

Find		•
Find what:		
part reference=R*		Find
Find in:		
Parts		ifferential Pair
Part Pins		hysical CSet
		lectrical CSet
Hierarchical Pins		pacing CSet
Hierarchical Ports		latched Group
Off-Page-Connectors		
Nets		ext
🗌 Flat Nets		RC Markers
Floating Nets		
Power/GND		itleBlocks
Variant Parts	B	ookmarks
Find options:		
Match case		
Use Regular Expresions		
Property Name=Value		
Property Name=value		
Result options:		
Highlight		

5. Click the *Find* button.

The Find Results window appears with all the resistors in the design.

Find Results								×
Parts								
Part Reference	Value	Source Part	Source Library	Page	Page Number	Schematic	Zone	Location X
R1	4.7k	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1	1	SCHEMATIC1	5D	220
R2	60k	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1	1	SCHEMATIC1	5D	240
R3	20k	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1	1	SCHEMATIC1	5C	280
R4	40k	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1	1	SCHEMATIC1	4D	470
R5	50m	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1	1	SCHEMATIC1	4D	570
R6	200	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1	1	SCHEMATIC1	3D	730
R7	5	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1	1	SCHEMATIC1	3D	830
R8	10k	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1	1	SCHEMATIC1	2D	930
R9	15	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1	1	SCHEMATIC1	2D	1150
R10	32	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1	1	SCHEMATIC1	3C	840
•								<u>۲</u>

- 6. To select all rows in the search result, click the first search results row, press SHIFT and then click the last search results row.
- 7. To modify the properties of the selected search results, right-click the selection and choose *Edit Properties* or press CTRL+SHIFT+E.

### Figure 4-7 Editing properties of search results

Find Results									
Parts									
Part Reference	Value	Source Part	Source Library	Page	Page	Number	Schematic	Zone	Locatio
R1	4.7k	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1			SCHEMATIC1	5D	220
R2	60k	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1			SCHEMATIC1	5D	240
R3	20k	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1			SCHEMATIC1	5C	280
R4	40k	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1			SCHEMATIC1	4N	470
R5	50m	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1		Edit P	Properties (Ctrl+S	hift+E)	
R6	200	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1		Save	as HTML		
R7	5	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1		Save	as CSV		
R8	10k	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1					
R9	15	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1		Assig	n Sl Model		
R10	32	R	C:\174\TOOLS\CAPTURE\LIBRARY\PSPICE\	PAGE1		Confi	gure Properties		

The Browse Spreadsheet window opens.

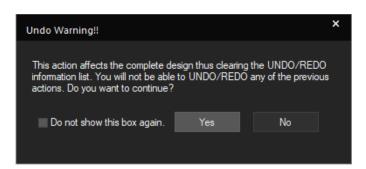
**8.** Change the value from AXRC05 to SMR2512 for *PCB Footprint* corresponding to each resistor.

	TC1	MAX_TEMP	DIST	VOLTAGE	POWER	PSpice Model Type	PCB Footprint	TOLERANCE	PSpice1	[emplat
1	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@R	EFDES
2	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@R	EFDES
3	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@R	EFDES
4	0	BTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@R	EFDES
5	0	BTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@R	EFDES
6	0	BTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@R	EFDES
7	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@R	EFDES
8	0	RTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@R	EFDES
9	0	BTMAX	FLAT	<b>BVMAX</b>	BMAX	0011	AXRC05		R^@R	EFDES
10	0	BTMAX	FLAT	RVMAX	RMAX	0011	AXRC05		R^@R	EFDES
•										

	TC1	MAX_TEMP	DIST	VOLTAGE	POWER	PSpice Model Type	PCB Footprint	TOLERANCE	PSpic	:eTempl	at
1	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@	REFDE	S
2	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@	REFDE	S
3	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@	REFDE	S
4	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@	REFDE	S
5	0	RTMAX	FLAT	RVMAX	RMAX	0011	SMR2512		R^@	REFDE	s
6	0	RTMAX	FLAT	RVMAX	BMAX	0011	SMR2512		R^@	REFDE	S
7	0	RTMAX	FLAT	RVMAX	BMAX	0011	SMR2512		R^@	REFDE	S
8	0	RTMAX	FLAT	RVMAX	BMAX	0011	SMR2512		R^@	REFDE	S
9	0	RTMAX	FLAT	RVMAX	BMAX	0011	SMR2512		R^@	REFDE	S
10	0	RTMAX	FLAT	RVMAX	BMAX	0011	SMR2512		R^@	REFDE	S
•											•

**9.** Click *OK*.

An undo warning appears to confirm the change.



**10.** Select the *Do not show this box again* check box and then click *Yes*.

### **Updating Footprints associated with Capacitors**

To update footprints associated with all the capacitors in the design, do the following:

- 1. Repeat step 2 to step 10 listed in the section, <u>Updating Footprints associated with</u> <u>Resistors</u> with the following changes:
  - □ In step 2, specify part reference=C\* in the *Find what* field.
  - □ In step 8, change the value to SMC0603 for *PCB Footprint* corresponding to each capacitor.
- **2.** Save the design.

### **Updating Footprints associated with Inductors**

To update footprints associated with all the inductors in the design, do the following:

- 1. Repeat step 2 to step 10 listed in the section, <u>Updating Footprints associated with</u> <u>Resistors</u> with the following changes:
  - **a.** In step 2, specify part reference=L\* in the Find what field.
  - **b.** In step 8, change the value to SML0805 for *PCB Footprint* corresponding to each inductor.
- **2.** Save the design.

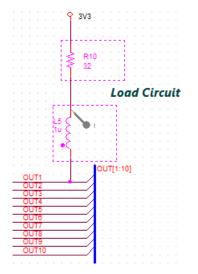
### Configuring the PSpiceOnly Property

These components are added only to represent the fan loads and are not required for the physical layout. To ignore them in board design, the PSpiceOnly property is specified.

To assign the PSpiceOnly property to the inductor and the resistor of the load circuit, do the following:

1. Select the inductor and resistor in the load circuit.

#### Figure 4-9 Selecting components of load circuit



- 2. Right-click and select *Edit Properties*.
- 3. Click the *Parts* tab in the *Property Editor* window.
- 4. From the Filter by drop-down list, select Capture PSpice.
- 5. Specify TRUE in the PSpiceOnly property for the selected inductor and resistor.

	-		
	Α	В	
	SCHEMATIC1 : PAGE1	SCHEMATIC1 : PAGE1	
Implementation			
Implementation Type	<none></none>	<none></none>	
IO_LEVEL			
IOMODEL			
MNTYMXDLY			
Name	INS15295494	INS15347008	
Part Reference	L5	R10	
Source Library	C:\174\TOOLS\CAPTU	C:\174\TOOLS\CAPTU	
Source Package	L	R	
PSpiceTemplate	L^@REFDES %1 %2 ?TOLE	R^@REFDES %1 %2 ?TOLE	
PSpiceOnly	TRUE	TRUE	
Reference	L5	R10	
Value	1u	32	
BiasValue Power	101.0e-30W	18.06e-18W	
CURRENT	ĽMAX/////		
DIELECTRIC	DSMAX		
DIST	FLAT/////	FLAT	
IC			
L1	0		
IL2	<u>/////////////////////////////////////</u>		
Location X-Coordinate	830	840	
Location Y-Coordinate	480	400	
MAX_TEMP		RTMAX	
POWER		RMAX	
PSpice Model Type	0011	0011	
SLOPE		RSMAX	
Source Part	L.Normal	R.Normal	
TC1	0		
TC2	0	0	
TOLERANCE			
VOLTAGE		RVMAX	

### Figure 4-10 Parts tab in Property Editor window

6. Save the design.

# **Adding Constraints**

To specify the minimum value of the total etch length of each net, Constraint Manager is launched from Capture.

To add this electrical constraint in the schematic design, do the following:

**1.** Select *PCB – Constraints Manager* or click the CM icon (

An information window appears to explain the Capture-Constraint Manager flow.

#### Figure 4-11 Enable Constraint Manager window

Enable Constraint Manager		×
To setup and manage constraints in your design:		
1. Complete the logical design.		
2. Add electrical constraints in Constraint Manager.		
3. Create or synchronize the PCB layout.		
4. Update electrical, physical, and spacing constraints in PCB layout.		
5. Run Update Layout and Update Schematic to synchronize constraints.		
Notes:		
- Specify the Voltage property for power nets.		
- Import technology file in Constraint Manager to add physical and spacing constraints in logic	cal design.	
For details about the Capture - Constraint Manager flow, click Help		
Do not show this message again	ОК	Help

2. Click OK.

The Migrate Constraints dialog box appears.

- 3. Select Migrate constraints from schematic design.
- 4. Specify the unit to be used for physical and spacing constraints in the Constraint Manger window.

PCB Editor uses Mils as the default unit. For this tutorial, select Mils from the Units drop-down list.

### Figure 4-12 Using option to migrate constraints from schematic design

Migrate Constraints			×
Select the option to migrate design constraints from schematic o	r PCB layout to Constra	aint Manager.	
<ul> <li>Migrate constraints from schematic design (For designs without PCB layout)</li> </ul>	Select the constrain	its unit and accuracy (decimal places	
Migrate constraints from PCB layout	Units	Mils -	
(For designs with constraints in PCB layout)	Accuracy	2	
		0/	
		ок	Help

5. Click *OK*.

The Assign Voltage to Power Nets window opens. This has predefined voltage values for all the power nets.

- 6. Modify these voltage values as follows:
  - □ VABTT = 12V
  - □ VCC=5V

	·
Power Nets	Voltage
VBATT	12V
GND	0.0V
0	0V
3V3	3.3V
VCC 5V	5V 5V
Auto-assign voltage values	s in subsequent designs
Specify default voltage	values for:
Ground Nets	0.0V
Power Nets	1.5V
	identify *GND*.*GROUND*.*VSS*

### Figure 4-13 Modifying predefined voltage values

You can open this dialog box from *SI Analysis – Identify DC Nets*.

**7.** Click *OK*.

The Constraints Manager window opens.

### Figure 4-14 Constraint Manager window

🎢 Constraint Manager (connected to capture	) [TUTORIAL] - [E	Electrical /	Net / Routing]	_	
File Edit Objects Column View	Audit Tools	Window	Help		-
			To To To To To	¶ (= + ⇒ +	
Worksheet Selector 🗗 🗙	TUTORIAL				
🖇 Electrical					Total Etch
Electrical Constraint Set			Objects		Length
_				Referenced Electrica	Min
, i i i i i i i i i i i i i i i i i i i	Туре	s	Name	CSet	
Y 🗀 Net					mil
✓ I Routing					
III Wiring	*	*	*	*	*
Impedance	Dsn		<b>J</b> TUTORIAL		
Min/Max Propagation Dela	Net		IN1		
Total Etch Length	Net		IN2		
Differential Pair	Net		IN3		
<ul> <li>Differential Pair</li> <li>Relative Propagation Delay</li> </ul>	Net		IN4		
	Net		IN5		
	Net		IN6		
+/+ Physical	Net		IN7		
+le Physical	Net		IN8		
Spacing	Net		IN9		
🖳 Same Net Spacing	Net		IN10		
	Net		IN11		
🏓 Properties	Net		IN12		
	Net		IN13		
esign Instance/Block filter 🛛 🗗 🗙	Net		IN14		
	Net		N00419		
	XNet		N00510		
	Net		N00682		
	Net		N00873		
	Net		N01131		
	XNet		N01720		
	Net	D	N02063		-
	<				>

**8.** Specify the minimum total etch length for the IN1 net as 100 mils as shown in the following figure.

TUTORIAL							
	Ob	jects		Total Etch Length			
<b>T</b>			Referenced Electrical CSet	Min	Actual	Margin	
Туре	S	Name		mil	mil	mil	
•	*	*	*	*	*	*	
Dsn		🖌 TUTORIAL			_		
Net	888888	S IN1		100.00	888888	3888888	
Net	38888	IN2					
Net		N3					
Net		IN4					
Net		IN5				XXXXX	
Net		N6					
Net		S IN7					
Net	8 8 8 8 8 8	S IN8					
Net	38	S IN9					
Net		S IN10					
Net		N11					
Net		N12					
Net		N13					
Net		🖔 IN14					
Net		N00419					
XNet	8188888	N00510					
Net		N00682					

### Figure 4-15 Specifying minimum total etch length value in schematic design

**9.** To specify the same value for *Total Etch Length* in all the nets, select the next row up till the last net in this window. Release the mouse and specify 100 in the last row.

	Obj	ects		Tot	al Etch Len	gth	
Туре	s	Name	Referenced Electrical CSet	Min	Actual	Margin	
Type	5	Marrie		mil	mil	mil	
*	*	*	*	*	*	*	
Dsn		▲ TUTORIAL					
Net		IN1		100.00		10000	
Net		IN2		100.00			
Net	30000	IN3		100.00			
Net	888888	IN4		100.00		88888	
Net	8	IN5		100.00			
Net		IN6		100.00			
Net		IN7		100.00			
Net		IN8		100.00		388888	
Net		IN9		100.00	888888	88888	
Net		IN10		100.00		8888	
Net		IN11		100.00			
Net	300000	IN12		100.00			
Net	80000	IN13		100.00		<u>                                      </u>	
Net	888888	IN14		100.00		80000	
Net		N00419		100.00			
XNet		N00510		100.00			
Net		N00682		100.00			
Net		N00873		100.00			
Net		N01131		100.00			
XNet		N01720		100.00			
Net	8	N02063		100.00			
Net	80000	N02685		100.00		10000	
Net	800000	N03504		100.00		8888	
Net	300000	N03592		100.00			
XNet		N04181		100.00			
XNet		OUT1		100.00		10000	
Net		OUT2		100.00			
Net	90000	OUT3		100.00			
Net		OUT4		100.00			
Net	80000	OUT5		100.00			
Net		OUT6		100.00			
Net	800000	OUT7		100.00		2000	
Net		OUT8		100.00			
Net		OUT9		100.00		10000	
Net	3000000	OUT10		100.00	<b>****</b> ****		

#### All the nets and xnets in the design are assigned the same value.

**10.** Save the design.

### Summary

This chapter covered the steps for preparing the schematic design for designing the physical layout of the PCB board. In the process, you were introduced to tasks, such as placing

connectors, adding footprint information, and adding electrical constraints using Constraint Manager.

# **Creating a Board Design**

Once the logic design is completed, the next step is to create the layout of the PCB. This chapter walks you through the basics of the layout creation steps, such as placement, routing, and generating output data to create a layout of the fan-control module design in the PCB Editor.

In this chapter, you will learn how to create a layout design tutorial.brd for the logic design you created and simulated in the previous chapters.

# **Creating a Blank Board**

The first task is to create a new blank board design. Perform the following steps to create a blank board design:

- 1. Open tutorial.opj in OrCAD Capture.
- 2. Choose PCB New Layout.

#### Figure 5-1 Creating a blank board design in Capture

New Layout		×			
Create New Layout and Associate in Project					
PCB Layout Folder	allegro				
Input Board File					
Board	.\allegro\tutorial.brd				
	Ok Cancel H	Help			

The new board design will be created in the default PCB Layout folder allegro inside the working project directory.

- **3.** To create a blank board design, leave the *Input Board File* name field blank.
- 4. Specify the output board file name as tutorial and click OK.

The Cadence 17.4 Product choices dialog box is displayed.

5. Select the OrCAD PCB Designer Professional w/PSpice option and click OK.

A blank design tutorial.brd is opened in PCB Editor. The logic design data is transferred to the layout and is saved in the allegro directory.

# **Creating Design Outline**

Design outline specifies the boundary within which components can be placed. It is necessary to create a design outline when transferring design data for ECAD-MCAD evaluation.

1. In PCB Editor, choose *Outline – Design*.

The Active Class and Subclass fields are by default set to Board\_Geometry and Design\_Outline in the Options tab.

- 2. In the Design Outline form, select *Place rectangle* and set *Width* and *Height* values to 2603 and 2333 mils, respectively.
- **3.** Set *Design edge clearance* value to 10 mils. This value defines the space between the board outline and package and route keepin boundaries which is required to accommodate manufacturing tolerances, testing, and assembly.

A rectangular design outline is attached to the cursor.

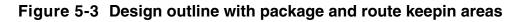
### Figure 5-2 Setting up design outline parameters

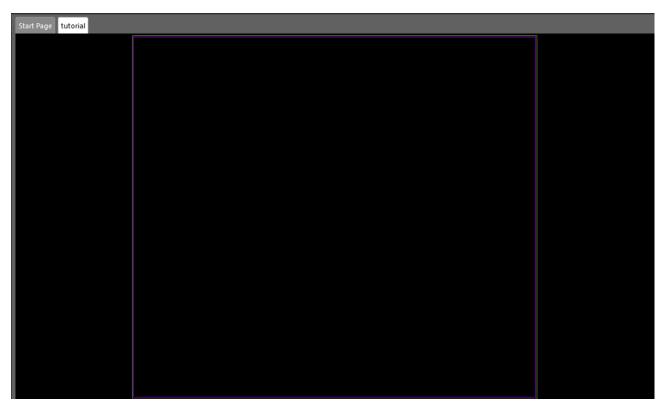
器 Design Outline		_		×
Command Operations Create Edit Design edge clearance:	• •	Move	Delete	
Create Options     Draw rectangle     Place rectangle     Draw polygon	Width: Height:	2603.00 MIL 2333.00 MIL		]
OK Apply	Cancel		Hel	p

- 4. Click anywhere in the design canvas to place the outline.
- 5. Click *OK* to close the Design Outline form.

A rectangular board outline is created with package and route keepin areas.

6. To view the entire board in the design canvas, choose *Display – Zoom – Fit* to center the board outline in the design window.





7. Choose *File – Save* to save the design.

# **Placing Components**

After creating the design outline you can start with component placement. All types of component symbols (discrete, ICs, mechanical, and format) can be placed either manually or by using automatic placement in the PCB Editor.

For this tutorial, place components interactively using the place manual command either in horizontal or vertical orientation using standard grid size of 25 mil, which makes them easy to align and assemble on the board.

- **1.** To start the placement, first enable the placement editing environment. Choose *Setup Application Mode Placement Edit.*
- **2.** Choose *Place Components Manually*.

By default, Placement form shows all the components listed by their reference designators. You can choose any reference designator and place it in the design canvas.

	🔐 Placement		_		×
	Placement List Advanced Settings				
		Selection filters			
	Components by refdes 🔹 🔻	O Match:			ı I
$\overline{C}$ 1 1	Y 🔤 🗁 Components by refdes				· 1
$\bigcirc$ I I	✓ <a>C11</a>	Property:			
	<ul> <li>C12</li> <li>C13</li> </ul>	Value			
	🗖 🔶 C14	Room:			- 1
	🗖 🔷 C15	Part #:		1 1	
	🗖 🔷 C16	• Net:		i i	
	C17	Net group:		i i	
	C18			Î	
	C19	Schematic page number		l	
	C20	Place by refdes     Quickview			
	□ ♦ D1 □ ♦ J1	quickness			- 1
					- 1
	↓ J2 ↓ J3				- 1
	• ÷ #				- 1
	↓ 12				- 1
	■ ♦ L3	O Graphics	Te	<del></del>	- 1
	■ ◆ L4	- O Graphics	10	XL.	
	Close Hide	Cancel		Help	

#### Figure 5-4 Selecting components from Placement form

3. Select the capacitor symbol C11.

The symbol gets attached to the cursor and is also visible in the *Quickview* window.

**4.** Right-click to choose *Rotate*. Use the handlebar to rotate the symbol by 90 degrees in anti-clockwise direction.

### Figure 5-5 Rotating component before placing

1	Done	/ F6	I 4
	Oops	F8	
	Cancel	F9	
$\sim$	Next	Ctrl+F2	
	Alt Symbol		
	Place on Layer		1
	Move		
	Mirror		
	Mirror Geometry		
	Rotate		
	Show		
	Snap pick to	•	

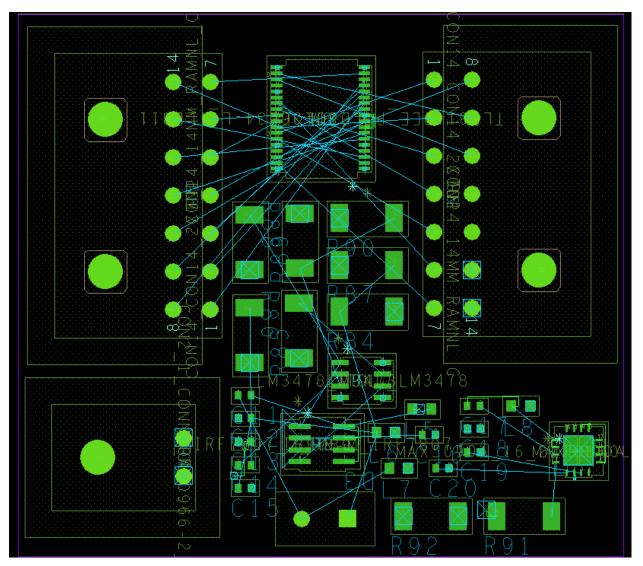
- 5. Left-click in the design canvas to place the capacitor symbol.
- **6.** Similarly, select each reference designator one by one to place all the component symbols.



Place the symbols according to their logically connectivity. You can refer to schematic design to know which components are logically connected and must be placed closely.

The following image depicts a sample placement.

Figure 5-6 Sample placement



7. Choose File - Save to save the design.

**Note:** The placement is the most important step of the PCB design and impact all the subsequent steps of the layout design. If you choose to place components differently, the final routed board will also be different.

# **Setting Up Constraints**

To meet manufacturing requirements you can configure the default constraint values in Constraint Manager either by creating constraint sets or by directly modifying the constraint values.

Before routing the board, specify the design constraints for routing. For this tutorial, specify two constraints for routing power nets: minimum thickness of the cline and maximum length of cline in neck mode.

- **1.** Choose Setup Constraints.
- 2. In the *Physical* domain, choose *Net All Layers*.
- 3. In the All Layers worksheet, select the net 5V.
- 4. Change the value of *Min Line Width* to 15 mil and *Max Neck Length* to 100 mil.
- 5. Similarly, select the nets 3V3 and 0 and change the values for *Min Line Width* and *Max Neck Length*.

New values are displayed in blue color for the power nets. When routing, any violation to these values will create a DRC error.

#### Figure 5-7 Setting overrides for physical constraints

Objects		Objects		Lir	ne Width		Neck
_	_		Referenced Physical CSet	Min	Max	Min Width	Max Length
Туре	S	Name		mil	mil	mil	mil
*	*	*	*	*	*	*	*
Net		OUT10	DEFAULT	5.00	0.00	5.00	0.00
Net		VBATT	DEFAULT	5.00	0.00	5.00	0.00
Net		0	DEFAULT	15.00	0.00	5.00	100.00
Net		3V3	DEFAULT	15.00	0.00	5.00	100.00
Net		5V	DEFAULT	15.00	0.00	5.00	100.00

6. Close Constraint Manager.

7. Choose *File – Save* to save the design.

### **Routing Nets**

Connecting the components in a layout is called routing. PCB Editor provides both manual and auto routing capabilities.

For this tutorial, use smart router for complete auto-routing.

**1.** Choose *Route – PCB Router – Route Automatic.* 

The Automatic Router opens and shows options to configure parameters for routing. For this tutorial, use the default values.

🔡 Automatic F	louter			_		Х
Router Setup	Routing Pas	ses Smart	Router Selections			
Strategy				1	Clo	se
<ul> <li>Specify rou</li> </ul>	iting passes	Use	smart router			
Do file:					Rou	te
Coptions ───				1	Und	io
Limit via cr	eation	Т	urbo Stagger			
Limit wrap	arounds		nable diagonal routing		Resu	ilts
Protect exi	sting routes					
└── Wire grid ──				]		
X grid: 0.0	1	Y grid:	0.01			
X offset: 0.00	)	Y offset:	0.00			
					Hel	D
┌ Via grid ——				1		-
X grid: 0.0	1	Y grid:	0.01			
X offset: 0.00	)	Y offset:	0.00			
Routir	ng Subclass		Routing Direction			
🔽 ТОР		Horizontal				
🗾 вопо	М	Vertical				
	_					

#### Figure 5-8 Automatic Router setup form

2. To start auto-routing, click the *Route* button.

The auto-route process starts and takes a few seconds to complete. The auto-router considers the design outline and keepin areas while routing nets.

**3.** To verify that routing is completed successfully, choose *Check – Design Status*.

Figure	5-9	Design	status	form
--------	-----	--------	--------	------

🚼 Status – 🗆 🗙						
Status						
Symt	ools and nets					
	Unplaced symbols:	0/31	0 %			
	Unrouted nets:	0/42	0 %			
	Unrouted connections:	0/98	0 %			

The Status window confirms that all the nets are routed.

- 4. Click *OK* to close the Status window.
- 5. Close Automatic Router.

The following image shows a routed board design.

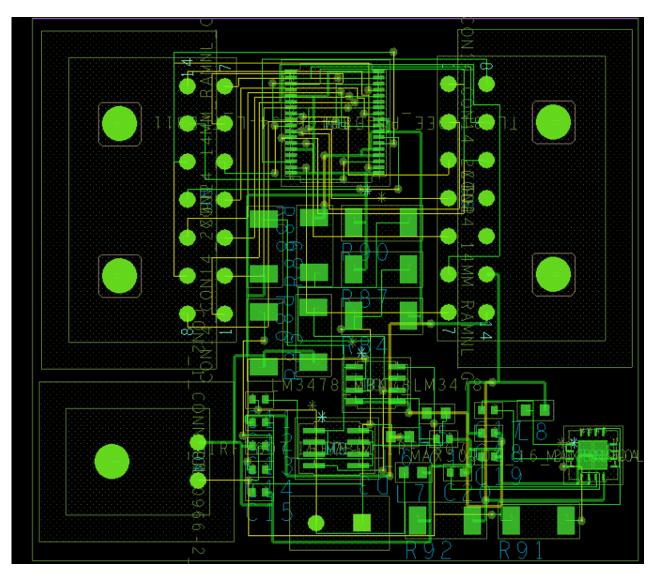


Figure 5-10 Auto-routed board design sample

6. Choose File - Save to save the design.

# **Renaming Components**

After you have completed the placement and routing you can reorder the reference designators of components on the board in a specific pattern. This steps makes the testing and assembly process easier.

**1.** Choose *Manufacture – Auto Rename Refdes – Rename*.

The Rename Refdes form opens showing grid settings and option to select all the components for renaming action.

Figure 5-11 Rename reference designators options

器 Rename RefDes	_		×
Grid Specification			
<ul> <li>User defined grid</li> <li>Use default grid</li> </ul>			
Rename all components			
Attach property, components			
Rename Setup			
OK Cancel		Hel	p

2. Click the *Setup* button to specify more options.

The Rename Ref Des Set Up form opens.

- **3.** In the *Reference Designator Format* section:
  - **a.** Remove layer identifier for TOP and BOTTOM layers.
  - **b.** Enable the *Preserve Current prefixes* check box.

🚼 Rename Ref Des Set Up	– 🗆 X
Layer Options	Reference Designator Format
Layer: BOTH 🔻	RefDes Prefix: *
Starting Layer: 🔹 Top Layer	Top Layer Identifier:
Component Origin: Body Center 🔻	Bottom Layer Identifier:
	Skip Character(s): IOQ
Directions for Top Layer	Renaming Method: Sequential 🔻
First Direction: Horizontal 🔻	Preserve current prefixes
Ordering:	Sequential Renaming
Left to Right 🔻 then Downwards 🔻	
	Refdes Digits: 1 🔻
	└────────────────────────────────────
Directions for Bottom Layer	
First Direction:	1st Direction Designation:
Ordering:	2nd Direction Designation:
Right to left 🔻 then Downwards 🔻	Suffix:
Close Cancel Reset	Help

#### Figure 5-12 Rename reference designator settings

- 4. Close the *Rename Ref Set Up* form.
- 5. Click the *Rename* button in the Rename RefDes form.

Renaming of reference designators starts from the upper-left corner of the board in the horizontal direction and the numbers are increasing in the downward direction.

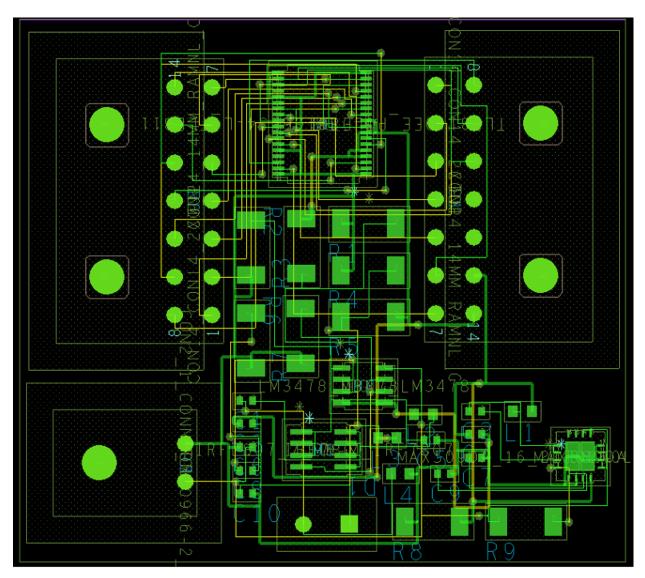


Figure 5-13 Board design with renamed reference designators

- 6. Click OK to close the Rename RefDes form.
- 7. Choose *File Save* to save the design.

# Visualizing Design in 3D

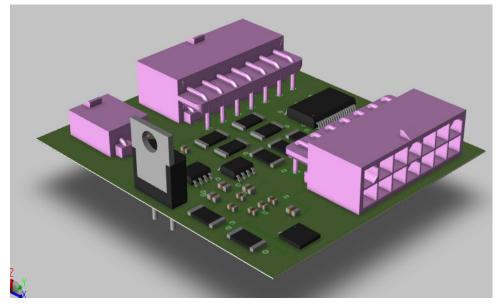
The built-in 3D visualization tool of PCB Editor lets you preview the board design at any time during the design. You can open the design in 3D Canvas and verify the design as a complete assembly.

To analyze the design in the 3D Canvas, 3D models must be assigned to all the symbols. You can map a 3D model either at a symbol level or at the design level. PCB Editor, by default, supports STEP models for 3D visualization. For the components used in this tutorial, 3D models are assigned at the symbol level.

1. Choose Display – 3D Canvas.

A progress bar displays while loading the design into 3D Canvas.

Figure 5-14 3D view of board design



- 2. Choose *View Camera* options to view the design in different perspectives.
- 3. Close 3D Canvas.

### **Generating Manufacturing Files**

The final task is to generate various types of output files of the physical design data. You can create Gerber files, Excellon NC Drill files, DXF files, IPC2581, ODB++, and printer/plotter

files. These files are standard files and are required by the fabrication houses to manufacture a PCB.

For this tutorial, create three types of output files:

- Artwork (Gerber)
- NC Drill
- IPC2581

### **Creating Artwork**

To create artwork files, PCB Editor reads film control records to determine the number of artwork files to produce, their names, and list of classes and subclasses to include in each artwork file.

To specify classes and subclasses for an artwork file, use Color Dialog to set the visibility of required classes and subclasses.

1. Choose Setup – Colors.

The Color Dialog opens.

2. In the *Layers* tab, click the *Off* button for *Global Visibility*.

The visibility of all the classes and subclass are turned off.

**3.** Expand the *Stack-Up – Conductor* folder, select *Soldermask\_Top* and *Pastemask\_Top* layers and enable the check box for *Pin* only.

The soldermask and pastemask layers of pins becomes visible in the design canvas.

**4.** Similarly, in the *Geometry* folder, select *Soldermask\_Top* and *Pastemask\_Top* layers and enable the checkbox for *All* objects.

The visibility of soldermask and pastemask layer is set on both board and package geometry.

- 5. Click *OK* to close the Color Dialog.
- 6. Choose *Export Gerber*.

The Artwork Control Form opens which reads the cross-section and auto-generates one film record for each etch subclass and includes etch, pins, and vias.

- 7. In Artwork Control Form, select both the TOP and BOTTOM layers.
- 8. Click *Create Artwork* to generate artwork.

### Figure 5-15 Artwork generation settings

🔐 Artwork Control Form		- 0	×
Film Control General Parameters			
Available films	Film options ————		
Domain Selection Create Missing Films	Film name:	воттом	
	PDF Sequence:	2 🔨 🔨	
> 🗹 🛅 воттом			
> 🗹 🧰 тор	Rotation:	0 🔻	
	Offset X:	0.00	
	Y:	0.00	
	Undefined line width:	0.00	
	Shape bounding box:	100.00	
	Plot mode:	O Positive	
	Film mirrored	Negative	
Select all Add Replace	Full contact thermal-reliefs		
Check database before artwork	Suppress unconnected pads		
	Draw missing pad apertures		
	Use aperture rotation Suppress shape fill		
Create Artwork	Suppress shape fill Vector based pad behavior		
	Draw holes only		
OK Cancel Apertures.	Viewlog	Help	
	viewiog		

Two artwork files (TOP.art and BOTTOM.art) are created in the allegro directory.

- 9. Click Viewlog to review the log file.
- **10.** Click *OK* to close the Artwork Control Form.

### **Creating NC Drill**

NC Drill output files are created for numerically-controlled (NC) drills and router and helps in assessing the cost of PCB manufacturing. The drill output files includes drill legend tables and drill files.

#### **Generating Drill Legend**

Drill legend tables are used in fabrication drawing and shows the number, type, and tolerance of plated and non-plated holes in the design.

- 1. Choose Setup Colors, click On to enable Global Visibility and click OK to close the dialog box.
- 2. Choose Manufacture Create Drill Table.

The Drill Legend form opens.

**3.** Click *OK* to generate the drill legend symbol.

The drill legend symbol gets attached to the cursor.

4. Left-click to place the drill legend in the design canvas.

#### Figure 5-16 Drill legend parameters and table

🔐 Drill Legend		- 🗆 🗙		
Template file: default-mil.dlt Output unit: Mils		Browse Library		
Legend title:				
Drill: DRILL CHART: \$lay_nams\$				
Backdrill: BACKDRILL: Slay_namsS		DRILL CHART: TOP	to BOTTOM	
C-Bore: COUNTERBORE/COUNTERSI		ALL UNITS ARE	IN MILS	
└ Hole sorting method: ────	FIGURE	FINISHED_SIZE	PLATED	QTY
By hole size	•		PLATED	47
Ascending		54.0	PLATED	
Legends:	۵		PLATED	
● Layer pair ● By layer	ंठ :	58.0	PLATED	28
Include backdrill     Include     Other Options:	L.		NON-PLATED	
Drill Legend Columns:	ы	154.0	NON-PLATED	
Tolerance drill ✓ Tolerance tr	avel Von-standa	and huma		
<ul> <li>Display total slot/drill count</li> <li>Separate slots from drills</li> <li>Suppress tolerance column if all valu</li> <li>Suppress tool size column if all valu</li> <li>Suppress rotation column if all valu</li> <li>OK</li> </ul>	ues are 0's lues are empty	Help		

#### **Generating NC Drill**

NC drill file is created based on the parameters specified for the drill coordinate data format.

**1.** Choose *Export – NC Drill*.

The NC Drill form opens.

- 2. Click *Parameters* to open NC Parameters form.
- **3.** Enable the *Enhanced Excellon format* checkbox.

A header in the NC Drill and NC Route output files is generated that uses Excellon commands.

- 4. Click *OK* to save the parameters.
- 5. Click Drill to generate the drill file.

### Figure 5-17 NC Drill setup options

R NC Drill	– 🗆 X	R NC Parameters		- 🗆 🗙
Root file name: brd.drl Scale factor: Tool sequence: O Increasing O Decreasing	Drill Parameters	Parameter file:	nc_param.txt	
Auto tool select Separate files for plated/non-plated holes FRepeat codes Optimize drill head travel Definice	Close Cancel Viewlog	Header:	none	
Drilling:     O Layer pair         By layer     Include backdrill     Include counterdrill	Help	Leader: Code: ✓ Automatically crea	12 O ASCII ate drill ncroutebits_auto	• EIA
		Excellon format: Format: Offset X: Coordinates: Output units: Leading zero supp Trailing zero supp Equal coordinate Enhanced Excellor	2 . 5 0.00 O Absolute O English pression rression suppression	Y: 0.00 Incremental Metric
		ОК	Cancel	Help

The NC Drill file (tutorial.drl) is created in the allegro directory.

- 6. Click *Viewlog* to review the log file.
- 7. Close the form.

### Creating IPC2581 Files

IPC2581 is an XML-based data exchange format used for providing physical design data for fabrication and assembly of PCBs.

For this tutorial, create IPC2581 output using default values.

1. Choose *Export – IPC2581*.

The IPC2581 Export form opens.

### Figure 5-18 Generating IPC2581 output

PC2581 Export       Export Property         Output file name:       tutorial	IPC2581 Export					—	×
IPC2581 version: IPC2581-B   Global package pin one orientation: OTHER   File Segmentations and Function Apportionment   Functional Mode: DESIGN   Level: Image: Imag	PC2581 Export Export Prope	erty					
Global package pin one orientation:   File Segmentations and Function Apportionment   Functional Mode:   DESIGN   Level:   AVL (Components and Materials)   AVL (Components and Materials)   Gavities   Cavities   Component Descriptions   Component Packages   DFX Analysis   Device Descriptions   Documentation Layers   Dirilling and Routing Layers   Hierarchical Conductor Routing Files   Hierarchical Layer/Stack Instance Files   Inner Layers     Vector text   Compress output file(.zip)	Output file name:	tutorial					
File Segmentations and Function Apportionment   Functional Mode: DESIGN Level: 3   Image: AVL (Components and Materials)   Image: AVL (Components and Materials)   Image: BOM (Components and Materials)   Image: Component Descriptions   Image: Component Descriptions   Image: Component Packages   Image: DFX Analysis   Image: Device Descriptions   Image:	IPC2581 version:	IPC2581-B 🔍	c	utput units:	Millimete	r 🔻	
Functional Mode: DESIGN      AVL (Components and Materials)       BOM (Components and Materials)       Cavities       Component Descriptions       Component Packages       DFX Analysis       Device Descriptions       Documentation Layers       Drilling and Routing Layers       Hierarchical Conductor Routing Files       Hierarchical Layer/Stack Instance Files       Mapping Edit          Vector text	Global package pin one orie	ntation:	OTHER				
<ul> <li>AVL (Components and Materials)</li> <li>BOM (Components and Materials)</li> <li>Cavities</li> <li>Component Descriptions</li> <li>Component Packages</li> <li>DFX Analysis</li> <li>Device Descriptions</li> <li>Documentation Layers</li> <li>Documentation Layers</li> <li>Documentatical Conductor Routing Files</li> <li>Hierarchical Conductor Routing Files</li> <li>Hierarchical Layer/Stack Instance Files</li> <li>Inner Layers</li> <li>Vector text</li> <li>Compress output file(.zip)</li> </ul>	- File Segmentations and Fun	nction Apportionme	nt				
<ul> <li>BOM (Components and Materials)</li> <li>Cavities</li> <li>Component Descriptions</li> <li>Component Packages</li> <li>DFX Analysis</li> <li>Device Descriptions</li> <li>Device Descriptions</li> <li>Documentation Layers</li> <li>Documentation Layers</li> <li>Documentation Layers</li> <li>Export Cross Section Data Only</li> <li>Hierarchical Conductor Routing Files</li> <li>Hierarchical Layer/Stack Instance Files</li> <li>Inner Layers</li> <li>Layer Mapping Edit</li> <li>Film Creation</li> <li>Vector text</li> <li>Compress output file(.zip)</li> </ul>	Functional Mode:	DESIGN	<b>•</b>	Level:	3  🔻	]	
<ul> <li>Cavities</li> <li>Component Descriptions</li> <li>Component Packages</li> <li>DFX Analysis</li> <li>Device Descriptions</li> <li>Documentation Layers</li> <li>Documentation Layers</li> <li>Drilling and Routing Layers</li> <li>Export Cross Section Data Only</li> <li>Hierarchical Conductor Routing Files</li> <li>Hierarchical Layer/Stack Instance Files</li> <li>Inner Layers</li> <li>Layer Mapping Edit</li> <li>Film Creation</li> <li>Vector text</li> <li>Compress output file(.zip)</li> </ul>	🔳 🛅 AVL (Compone	ents and Materials)					
<ul> <li>Component Descriptions</li> <li>Component Packages</li> <li>DFX Analysis</li> <li>Device Descriptions</li> <li>Documentation Layers</li> <li>Documentation Layers</li> <li>Drilling and Routing Layers</li> <li>Export Cross Section Data Only</li> <li>Hierarchical Conductor Routing Files</li> <li>Hierarchical Layer/Stack Instance Files</li> <li>Inner Layers</li> </ul> Film Creation Vector text Compress output file(.zip)	🗹 🧰 BOM (Compo	nents and Materials)	j				
<ul> <li>Component Packages</li> <li>DFX Analysis</li> <li>Device Descriptions</li> <li>Documentation Layers</li> <li>Documentation Layers</li> <li>Drilling and Routing Layers</li> <li>Export Cross Section Data Only</li> <li>Hierarchical Conductor Routing Files</li> <li>Hierarchical Layer/Stack Instance Files</li> <li>Inner Layers</li> </ul> Layer Mapping Edit Film Creation Vector text Compress output file(.zip)	🗖 🧰 Cavities						
<ul> <li>DFX Analysis</li> <li>Device Descriptions</li> <li>Documentation Layers</li> <li>Drilling and Routing Layers</li> <li>Export Cross Section Data Only</li> <li>Hierarchical Conductor Routing Files</li> <li>Hierarchical Layer/Stack Instance Files</li> <li>Inner Layers</li> </ul> Layer Mapping Edit Film Creation Vector text Compress output file(.zip)	🗹 🧰 Component D	escriptions					
<ul> <li>Device Descriptions</li> <li>Documentation Layers</li> <li>Drilling and Routing Layers</li> <li>Export Cross Section Data Only</li> <li>Hierarchical Conductor Routing Files</li> <li>Hierarchical Layer/Stack Instance Files</li> <li>Inner Layers</li> </ul> Layer Mapping Edit Film Creation Vector text Compress output file(.zip)	🗹 🧰 Component P	ackages					
<ul> <li>Documentation Layers</li> <li>Drilling and Routing Layers</li> <li>Export Cross Section Data Only</li> <li>Hierarchical Conductor Routing Files</li> <li>Hierarchical Layer/Stack Instance Files</li> <li>Inner Layers</li> </ul> Layer Mapping Edit Film Creation Vector text Compress output file(.zip)	🗖 🧰 DFX Analysis						
<ul> <li>Drilling and Routing Layers</li> <li>Export Cross Section Data Only</li> <li>Hierarchical Conductor Routing Files</li> <li>Hierarchical Layer/Stack Instance Files</li> <li>Inner Layers</li> </ul> Layer Mapping Edit Film Creation Vector text Compress output file(.zip)	🗹 🧰 Device Descrip	ptions					
<ul> <li>Export Cross Section Data Only</li> <li>Hierarchical Conductor Routing Files</li> <li>Hierarchical Layer/Stack Instance Files</li> <li>Inner Layers</li> </ul> Layer Mapping Edit Film Creation Vector text Compress output file(.zip)	🗹 🧰 Documentatio	on Layers					
<ul> <li>Hierarchical Conductor Routing Files <ul> <li>Hierarchical Layer/Stack Instance Files</li> <li>Inner Layers</li> </ul> </li> <li>Layer Mapping Edit Film Creation</li> <li>Vector text Compress output file(.zip)</li> </ul>	🗹 🧰 Drilling and R	outing Layers					
Hierarchical Layer/Stack Instance Files Inner Layers Layer Mapping Edit Film Creation Vector text Compress output file(.zip)	📃 🧰 Export Cross S	Section Data Only					
Inner Layers       Layer Mapping Edit       Film Creation       Vector text       Compress output file(.zip)	🔲 🧰 Hierarchical C	onductor Routing F	iles				
Layer Mapping Edit     Film Creation       Vector text     Compress output file(.zip)	📃 🧰 Hierarchical La	ayer/Stack Instance F	iles				
Vector text Compress output file(.zip)	🗹 🧰 Inner Layers						
Vector text Compress output file(.zip)							
	Layer Mapping Edit	F	ilm Creation				
Export Close Viewlog Help	✓ Vector text	Compress out	tput file(.zip)				
	Export	Close	Viewlog		Help		

- 2. Leave the IPC2581 version to default, which is set to the latest version IPC2581-B.
- 3. Select Output units to Millimeter.
- 4. Set the Functional Mode to DESIGN and Level to 3.

Five functional modes are supported and each mode consists of three levels that define the complexity and detail of the output file.

5. Click *Film Creation* to add class and subclass for film records.

The Artwork Control Form opens.

6. Select both the TOP and BOTTOM layers and click OK to close the form.

Figure 5-19 Film record creation settings

Htwork Control Form				_		×
Film Control General Parameters						
Available films Film	n options ——					
Fi Fi	ilm name:		воттом			
Domain Selection Create Missing Films Pl	DF Sequence:		2	^ V		
> ☑ 🗂 тор	otation:		0			
	lotation:		U			
•	Offset X	i:	0.00			
	Y		0.00			
	Indefined line w	vidth:	0.00			
	hape bounding	hov	100.00		i i	
	nape bounding	007.	100.00			
	lot mode:		<ul> <li>Positiv</li> <li>Negat</li> </ul>			
	Film mirrored		e nega			
Select all Add Replace	Full contact the	rmal-reliefs				
Check database before artwork	Suppress uncor	nnected pads				
	Draw missing pa					
	Use aperture ro					
Create Artwork	Suppress shape Vector based pa					
	Draw holes only					
OK Cancel Apertures	Viev	vlog		l	Hel	р

)<sup>\_\_</sup> Tip

When exporting IPC2581, it is recommended to enable *Dynamic unused pads suppression* option in Cross-section Editor to suppresses unconnected pads for the selected object types (pin/via) on the selected inner layers.

- 7. Click Layer Mapping Editor to specify layer type for each artwork film.
- 8. Select the check boxes for *Soldermask and SolderPaste Layers* for both the artwork films and click *OK* to close the form.

Figure 5-20 Layer mapping editor

🔡 IPC2581 Layer I	Mapping Editor			-		$\times$
Artwork Film	Outer Copper Layers	Inner Layers	Documentation Layers	SolderMask SolderPaste Layers	Miscellan Image La	
BOTTOM				✓		
TOP				$\checkmark$		
ОК	Cancel				Hel	p

9. To generate IPC2581 file, click Export.

An XML file (tutorial.xml) is created in the allegro directory.

**10.** Click *Viewlog* to review the log file.

### Summary

This completes the task of creating a board design and generating manufacturing files for the PCB. In this chapter, you were introduced to the flow of tasks required for creating a board design using PCB Editor. For detail description of layout creation tasks, refer to PCB Editor information set.