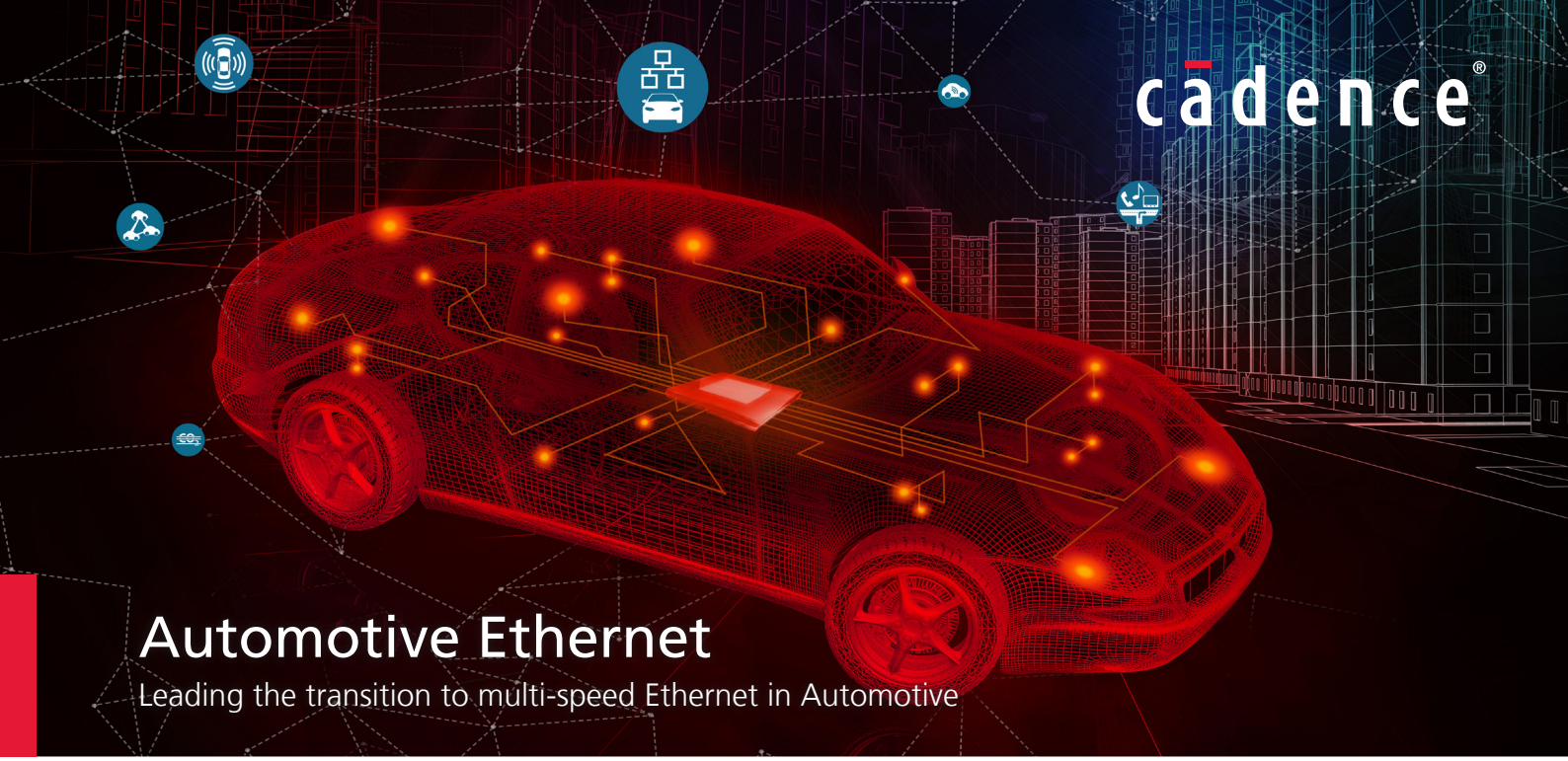

Automotive Ethernet

Leading the transition to multi-speed Ethernet in Automotive

Design and verify high-speed Automotive Ethernet communication links between advanced driver assistance systems (ADAS), infotainment, cameras, sensors, and other electronic control units (ECUs) by leveraging the Cadence® Ethernet solution.

This solution comprises a multi-speed Automotive Ethernet MAC Design IP, Verification IP (VIP) for Ethernet TSN, Ethernet rapid prototyping, and Cadence Sigrity™ technology for physical channel simulation and simulation-based Ethernet compliance testing.

Overview

Meanwhile the automotive industry has successfully introduced Ethernet for in-vehicle networking (IVN) based on open IEEE standards. Driven by the OPEN Alliance SIG and the IEEE 802.3 Working Group, these standards aim to develop a simpler, but more powerful, automotive electrical/electronic architecture. By supporting Ethernet speed grades from 10Mbps up to 10Gbps, a more homogeneous Ethernet-based IVN can be realized. In addition, the demand for deterministic and high-performance bandwidth features are accelerating Ethernet-based networks. Ethernet for IVN provides the lowest cost cabling solution with low-weight, single-pair, unshielded twisted-pair cable.

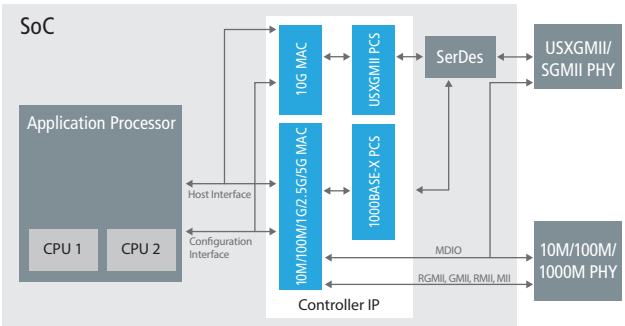

Figure 1: SoC Block Diagram with Ethernet Controller IP

10G/2.5G/1G Multi-Speed Ethernet Controller IP for Automotive Applications

In order to build highly integrated Ethernet-based systems on chip (SoCs), Cadence provides a 10G/2.5G/1G Multi-Speed Ethernet Controller for Automotive applications ,which is a highly customizable s oft controller IP, and is ISO 26262 ASIL-B ready (Figure 1).

The push for autonomous driving requires multiple streams of data from cameras, sensors, and radars be transferred and processed in real time. To meet the low-latency and safety requirements of mission-critical control systems like braking, steering, etc., Time Sensitive Networking (TSN) is being developed. TSN enables robust, low-latency, and deterministic synchronized packet transmission and is a super-set of the Audio-Video Bridging Transport (AVB) protocol standard. To support a range of Ethernet applications, the Controller IP features integrated 1000BASE-X and USXGMII PCS modules, a high-performance DMA with advanced AXI offloading capabilities, and descriptor caching, QoS, and IEEE 1588 support (Figure 2). The IP supports time synchronization such as IEEE 1588/802.1AS precision time protocol (PTP) via a Time Stamping Unit (TSU).

Key Features

- 10G/2.5G/1G Multi-Speed Ethernet Controller
- 100M and 10M speed grades
- TSN/AVB hardware support, including priority queuing, traffic shaping, and time-aware scheduling
- Time synchronization protocols IEEE 1588/802.1AS
- Embedded real-time clock and time-stamp unit
- Full-duplex flow control
- Deficit Weighted Round Robin (DWRR) and Strict Priority
- ISO 26262 ASIL-B ready
- Enhanced active functional safety features
- TCP/IP offloading capability and IEEE 1588 support

- Seamless DMA interfacing to Arm® AMBA® 3 AXI and AMBA 4 AXI and AHB interconnects
- MII, RMII, GMII, RGMII, USXGMII, and SGMII interfaces
- Integrated 1000BASE-X PCS and USXGMII PCS
- Seamless interoperability with 100Mbps, 1Gbps, and 10Gbps Ethernet PHYs
- IEEE 802.3 compliant and UNH tested
- Reference drivers, including Linux support
- Functional Safety including safety manual, and ISO 26262 ASIL-B readiness certificate

Functional Safety Features and Documentation

The Ethernet MAC has additional functional safety features targeting automotive applications. This includes memory protection using ECC, datapath and address parity protection, fatal fault detection, reporting, and recovery mechanisms. The deliverables also include the safety manual and ISO 26262 ASIL-B readiness certificate.

Supported IEEE 802.1 Standards

Standard	Description
IEEE 802.1AS-Rev	Timing and Synchronization for Time-Sensitive Applications
IEEE 802.1Qbu/ IEEE 802.3br	Frame Pre-Emption
IEEE 802.1Qbv	Enhancements for Scheduled Traffic
IEEE 802.1Qcc	Stream Reservation Protocol (SRP) Enhancements and Performance Improvements
IEEE 802.1CB	Frame Replication and Elimination for Reliability
IEEE 802.1Qav	Forwarding and Queuing Enhancements for Time-Sensitive Streams
IEEE 802.1Qci	Per-Stream filtering and receive traffic policing
IEEE 802.1Qaz	Enhanced transmission selection (ETS)

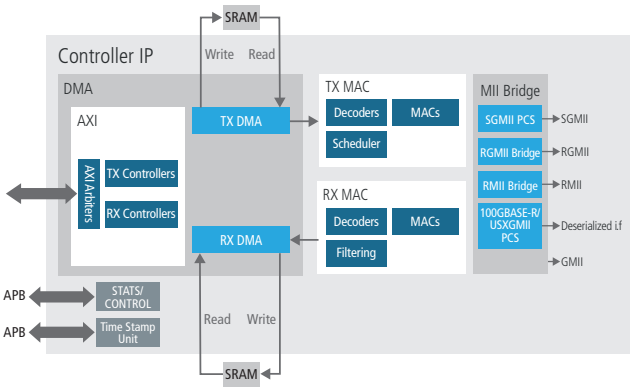

Figure 2: IP-level block diagram of Controller IP

VIP for Ethernet up to 100G

Incorporating the latest protocol updates, the mature and comprehensive Cadence Verification IP (VIP) for the Ethernet up to 100G protocols provides a complete bus functional model (BFM) including error insertion, integrated automatic protocol checkers, and coverage model. Designed for easy integration in testbenches at IP, SoC, and system levels, the VIP for Ethernet up to 100G helps you reduce time to test, accelerate verification closure, and ensure end-product quality.

The VIP for Ethernet up to 100G runs on all major simulators, and supports SystemVerilog and ***e*** verification languages along with associated methodologies, including the Universal Verification Methodology (UVM) and Open Verification Methodology (OVM).

The VIP for Ethernet up to 100G enables verification of Ethernet interfaces in standalone, partial-stack, and full-stack mode for speeds from 10Mbps to 100Gbps:

- XMII level: Between MAC and PHY
- PHY sub-layers: Between PCS, FEC, PMA, and PMD
- Link partners: Between TX Station and RX Station

The VIP for Ethernet up to 100G complies with IEEE 802.3 Ethernet standards and draft specifications. It supports other widely popular Ethernet interfaces, which are proprietary and based on IEEE 802.3. Hence, the VIP supports different configurations, as shown in Figure 3 and Figure 4.

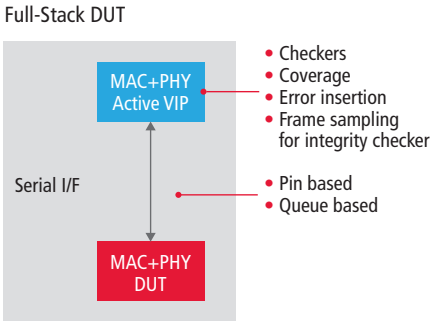

Figure 3. Ethernet VIP usage with a MAC+PHY DUT

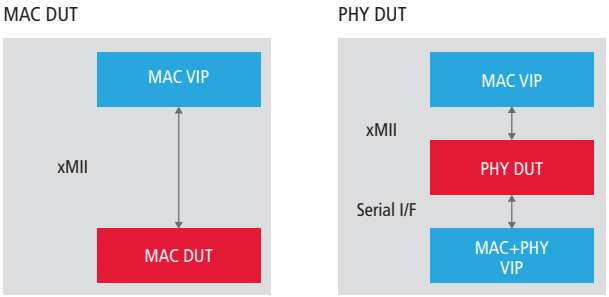

Figure 4. Ethernet VIP usage with a MAC DUT and PHY DUT

VIP for Ethernet TSN

The Cadence VIP for Time Sensitive Networks (TSN) provides a mature, highly capable compliance verification solution for the TSN protocol stack, incorporating BFM including error insertion, integrated automatic protocol checkers, and coverage model. The VIP for Ethernet TSN is designed for easy integration in testbenches at IP, SoC, and system levels, helping to reduce time to test, accelerate verification closure, and ensure end-product quality.

The following set of protocols are a part of the VIP for Ethernet TSN:

- IEEE 802.1AS PTP
- IEEE 802.1Qbu
- IEEE 802.3br
- IEEE 802.1Qav
- IEEE 802.1Qbv
- IEEE 802.1Qat
- IEEE 802.1AE
- IEEE 1722

The TSN protocols are usually designed to work over a framework of Ethernet MAC and PHY layers working at speed of 1Gbps or below.

VIP for Standard Interface Compliance

The increasing number and complexity of interfaces in automotive SoCs make it difficult to thoroughly verify designs. Cadence VIP boosts quality by providing VIP components that check compliance with standard interface specification such as CAN, LIN, Ethernet, DDR, Flash, USB, and dozens of others.

Benefits:

- Proven VIP provider, chosen by over 500 customers
- VIP available for over 100 interface and memory standards
- Verifies compliance to standard interface specifications for mission-critical designs

Sigrity SystemSI Automotive Ethernet Channel Simulation

Implement automotive Ethernet networks and analyze the ECU-to-ECU communication performance via the physical Ethernet channel with Cadence Sigrity™ SystemSI™ technology for automated chip-to-chip signal integrity analysis.

Simulate full physical channel to ensure Ethernet compliance:

- Test different PHY, connector, and cable combinations
- Supports cable segmentation (different cable length)
- With or without jacket, shielding
- Simulation-based EMI verification and optimization from ECU to ECU
- Analyze cable aging effects
- Run power integrity analysis on PCB
- Supports automotive Ethernet compliance checks for 100Base-T1 and 1000Base-T1 PHYs

Automotive Ethernet Compliance Tests for 100Base-T1 PHY and 1000Base-T1 PHY

- IBIS AMI models of PHY working on any cable topology
  - TX and RX models
- Physical channel simulated in Sigrity SystemSI technology
- Supported compliance tests:
  - Transmitter output droop
  - Transmitter power spectral density
  - Transmitter jitter (master/slave)
  - Transmitter clock frequency (PAM3)
  - Transmitter distortion
  - Return loss measurement

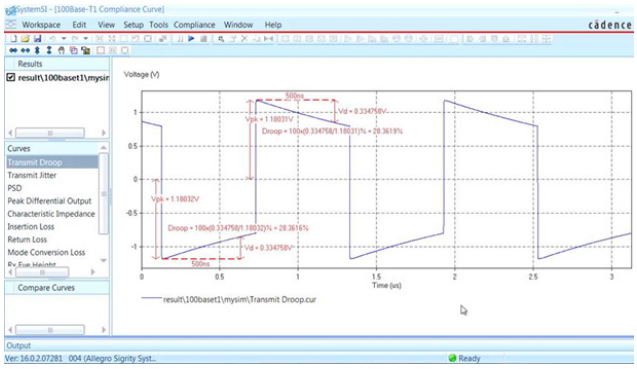

Figure 5: 100Base-T1 transmitter output droop

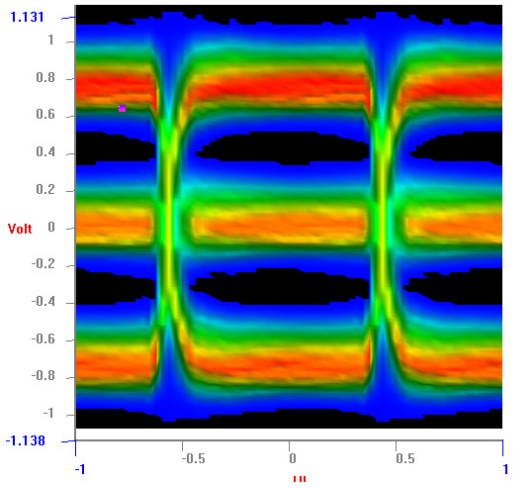

Figure 6: 100Base-T1 eye diagram

Ethernet Rapid Prototyping

For fast FPGA-based prototyping, Cadence has developed a BroadR-Reach PHY interface card that can be plugged into the Cadence Protium™ FPGA-Based Prototyping Platform. By doing so, external hardware like Ethernet cameras, infotainment head units, and other devices can be directly connected via an unshielded twisted-pair cable with the FPGA system. In this way, a SoC that was initially implemented as a FPGA prototype can also run software to do early hardware/software validation of the system leveraging the Protium solution. This setup also helps to analyze the impact of using different cables, connectors, and other hardware configurations on the overall system performance.

A relevant application for Ethernet rapid prototyping is using cameras within parking-assist systems in a top-view or rear-view configuration. Leveraging a hardware/software co-design methodology allows engineers to develop and test drive their Automotive Ethernet application (hardware/software) before the hardware—including the SoC—is available.

The Cadence BroadR-Reach Interface card can connect any external Ethernet device with the ECU or other control unit via the Cadence Automotive Ethernet MAC.

Further Information

To learn more about Cadence's IP options for automotive, visit www.cadence.com/automotive.

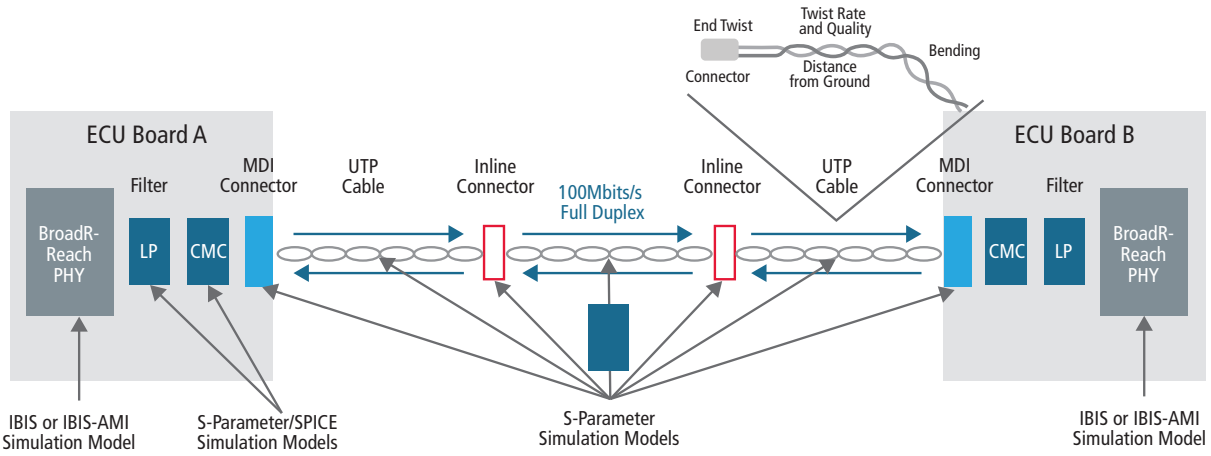

Figure 7: Key components of the physical Ethernet channel

cadence®

Cadence software, hardware, and semiconductor IP enable electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work, and play. The company's Intelligent System Design strategy helps customers develop differentiated products—from chips to boards to intelligent systems. **www.cadence.com**