

High-Performance and Low-Power Tensilica Processors for ADAS Designs

Plus a wide range of silicon-proven interface, memory, sensor IP for automotive safety and driver awareness

ADAS Design

The advanced driver assistance system (ADAS) segment—essential for enhancing the driver experience and overall safety—is one of the fastest growing segments of the automotive semiconductor space. The amount of electronics is growing fast with the level of the vehicle automation. As a consequence, autonomous driving is leading to major disruptions in the automotive industry because it requires a performance level that goes far beyond popular microcontrollers.

A new class of high-performance systems-on-chip (SoC) is needed to process all sensor data and fuse them together. In addition, high-definition digital maps and cloud-based services are leveraged to control the car in real time. Hence ADAS SoCs enable vehicles to become “aware” of their surroundings—but at a cost in terms of chip area, power consumption, and performance.

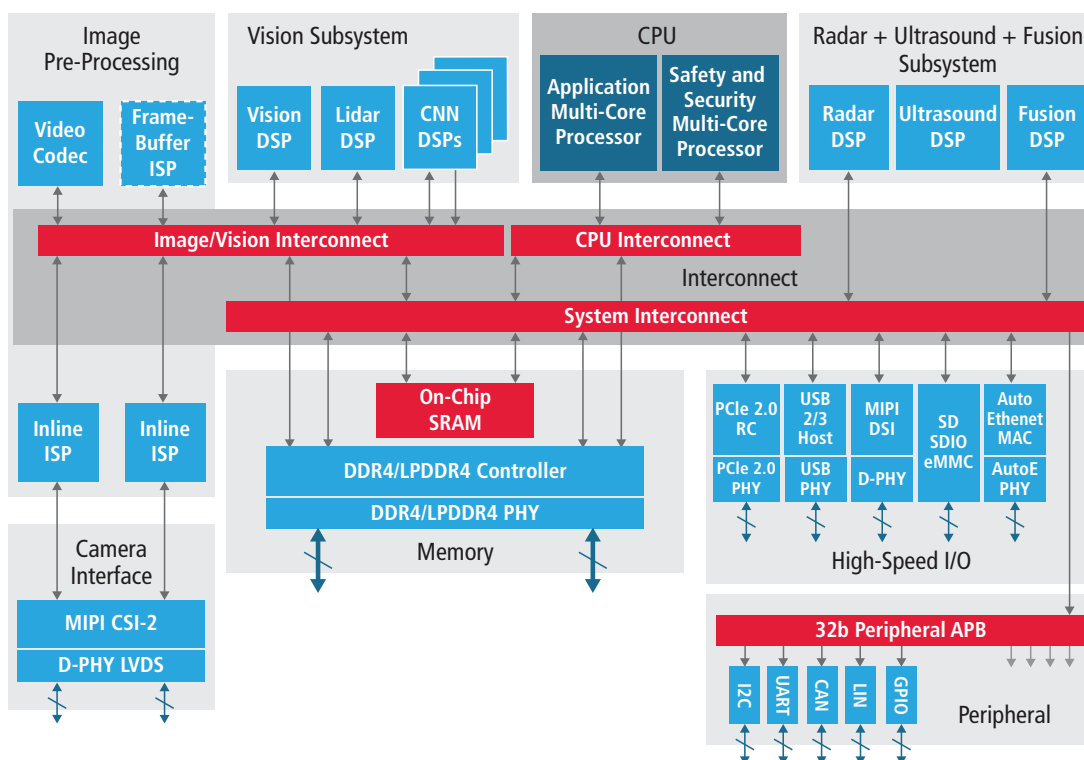


Figure 1: Example of an ADAS SoC architecture

High-performance ADAS SoC requirements include:

- High compute performance: 1TMAC/sec in < 1mm² to support a digital signal processing architecture tuned to process compute-intensive algorithms, all while delivering an optimal SoC power, performance, and area (PPA) ratio
- High network bandwidth: 1Gbit/s or more to support a low-latency transmission of high video/image resolution, rapid frame rates, video streams, and images
- High memory bandwidth: >3Gbit/s data rate and sufficient memory space required to store and access intermediate results generated by highly complex algorithms
- Low power consumption: <9W power consumption for the ADAS system

In addition, SoC-based ADAS electronic control units (ECUs) provide some key advantages over traditional microcontroller control units (MCUs) such as enabling a functional consolidation, physical miniaturization, and reduced power consumption.

All these essential technologies are evolving at a very fast rate, and Cadence is ready to help you with proven IP, tools, and services that will enable you to develop smarter and safer cars.

Tensilica IP

With optimizable Cadence® Tensilica® DSPs and the associated software partner ecosystem, applications for computer vision, imaging, neural networks, lidar, radar, ultrasound, and V2X can be efficiently implemented, saving silicon area and significantly reducing the power consumption compared to other solutions.

Regardless of the sensor type, a machine needs to efficiently analyze the data and reliably recognize objects. Recently neural networks have become very popular for this task enabling high object recognition rates of more than 99%. However current solutions based on CPUs or GPUs consume way too much power and therefore cannot be used in production cars.

Tensilica DSPs can help to efficiently offload the host CPU and accelerate the sensor data processing to significantly reduce the power consumption. Imaging and vision algorithms can run on a DSP that's specifically optimized for the imaging and vision functions required. Thus the Tensilica DSP can be leveraged in the sensor itself, within the ADAS ECU, or in the central sensor fusion platform, regardless of the ADAS application.

The huge amount of data generated by these sensors—up to 1Gbyte/s (4000GByte/day)—requires very powerful data-processing platforms with an AI performance of up to 30TMAC/s.

There are two key things that need to be addressed for the efficient deployment of neural networks:

- Hardware: A scalable, low-power multi-core hardware platform that is fully programmable
- Software: An automated development flow to automatically optimize and map neural networks on the target platform

Imaging, Computer Vision, and Neural Networks

The Tensilica Vision DSP family offers three Vision products:

- The Vision P5 DSP, introduced in 2015, offers up to 4X-100X the performance relative to traditional mobile CPU+GPU systems at a fraction of the power/energy.
- The Vision P6 DSP, introduced in 2016, set a new standard in neural network performance for a general-purpose imaging and computer vision DSP by offering 4X the peak performance compared to the Vision P5 DSP.
- The Vision C5 DSP, introduced in 2017, is the industry's first standalone, self-contained neural network DSP IP core with 1TMAC/sec computational capacity to run all computational tasks. It is architected for multi-core designs, enabling a multi-TMAC solution in a small footprint.

The combination of neural network computational hardware accelerators attached to imaging DSPs, with the neural network code split between running some neural network layers on the DSP and offloading convolutional layers to the accelerator, is inefficient and consumes unnecessary power.

Architected as a dedicated neural network-optimized DSP, the Vision C5 DSP accelerates all computational layers (convolution, fully connected, pooling, and normalization), not just the convolution functions. This frees up the main vision/imaging DSP to run image enhancement applications independently while the Vision C5 DSP runs inference tasks. By eliminating extraneous data movement between the neural network DSP and the main vision/imaging DSP, the Vision C5 DSP provides a scalable, lower power solution than competing neural network accelerators. Compared to commercially available GPUs, the Vision C5 DSP is up to 6X faster in the well-known AlexNet CNN performance benchmark and up to 9X faster in the Inception V3 CNN performance benchmark. It also offers a simple, single-processor programming model for neural networks.

The Vision C5 DSP, targeted for the automotive, surveillance, drone and mobile/wearable markets, is optimized for vision, radar/lidar, and fused-sensor applications with high-availability.

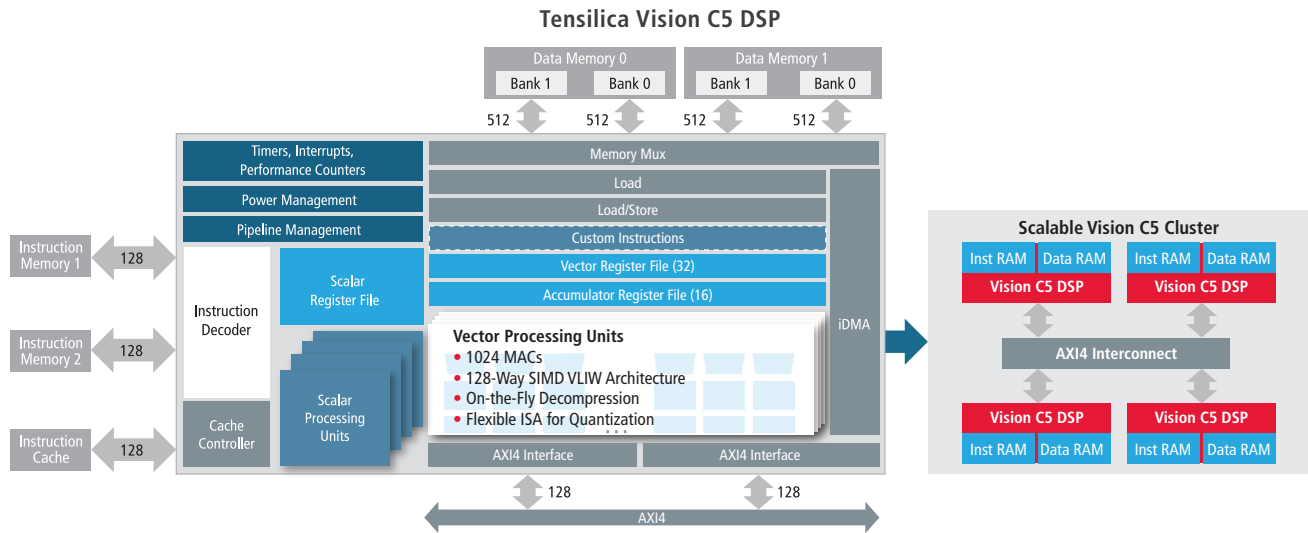


Figure 2: Scalable Vision C5 DSP cluster for multi-TMAC performance

Xtensa Neural Network Compiler

The Vision C5 DSP and the Vision P6 DSP also come with the Tensilica Xtensa® Neural Network Compiler, which will map any neural network trained with tools, such as TensorFlow, into executable and highly optimized code for the Vision C5 DSP, leveraging a comprehensive set of hand-optimized neural network library functions.

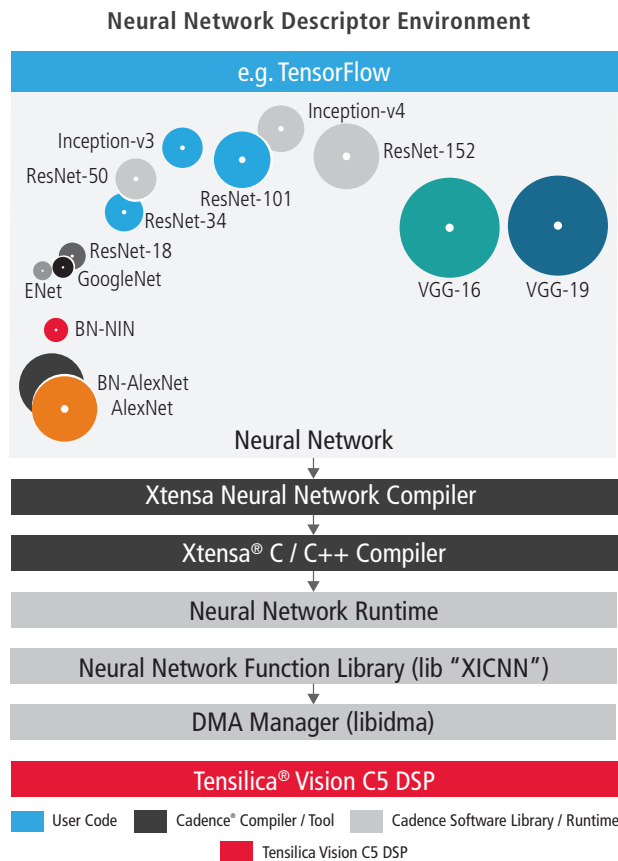


Figure 3: Automated neural network flow

OpenCV and OpenVX Library Support

The Vision P5 and P6 DSPs come with over 1000 OpenCV-like functions. These functions are highly optimized to achieve the best performance on these DSPs.

The Vision P5 and P6 DSPs are the first imaging/vision DSPs to pass Khronos Group’s conformance tests for the OpenVX 1.1 specification.

In addition, a dedicated, highly optimized function library (XICNN) and a DMA manager library (libidma) are provided as well.

The Vision C5 DSP, together with the Xtensa Neural Network Compiler and comprehensive library support, provide an efficient solution for the development of neural network applications.

Radar, Lidar, and Communications

Today, companies are already working on communications systems that will allow vehicles and roadside units to exchange information, such as safety or traffic information. Car2X communications systems, as well as radar and lidar sensors, require high-throughput DSPs to handle the heavy data communication bandwidth.

The Tensilica family of ConnX DSPs supports the required communication protocols like IEEE 802.11p and LTE Advanced, providing the responsiveness and throughput needed for low-latency and high-bandwidth communication standards, for applications like:

- 360° awareness of the car
- Camera-based vision processing for object detection/recognition
- Radar and lidar sensor processing
- Vehicular communications systems (Car2X or V2V)
- 5G communication to enable cloud-based services
- Emergency breaking
- Safety and Reliability Support

In order to support cost-effective automotive SoC designs, Cadence IP is area- and power-optimized for the AEC-Q100 Grade 2 temperature range, eliminating the need to carry Grade 1 power and area penalties into cost-sensitive automotive SoC designs. Cadence IP is designed to be ASIL-B ready and ASIL-C/D capable based on end users' safety goals and safety requirements as outlined in the ISO 26262 standard.

Pre-Silicon FPGA-Based Prototyping

ADAS SoCs are some of the most complex ICs in a car and are usually realized in an advanced process technology. Test chips (silicon) usually are available very late and re-spins are very expensive. Using Cadence FPGA-based prototyping technology, design and verification teams can rapidly bring up a prototype and provide a pre-silicon platform for early software development, system validation, and throughput regressions.

Verification IP for Standard Interface Compliance

The increasing number and complexity of interfaces in automotive SoCs makes it difficult to thoroughly verify designs. Cadence Verification IP (VIP) boosts quality by providing VIP components that check compliance with standard interface specifications such as CAN, LIN, Ethernet, DDR, Flash, USB, and dozens of other interfaces.

Benefits:

- Proven VIP provider, chosen by over 500 customers
- VIP available for over 100 interface and memory standards
- Verifies compliance to standard interface specifications for mission-critical designs

Further Information

To learn more about Cadence IP options for automotive, visit

www.cadence.com/automotive



Cadence software, hardware, and semiconductor IP enable electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work, and play. The company's Intelligent System Design strategy helps customers develop differentiated products—from chips to boards to intelligent systems. www.cadence.com

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