Silicon Photonics Variation and Design-for-Manufacturability (DFM)

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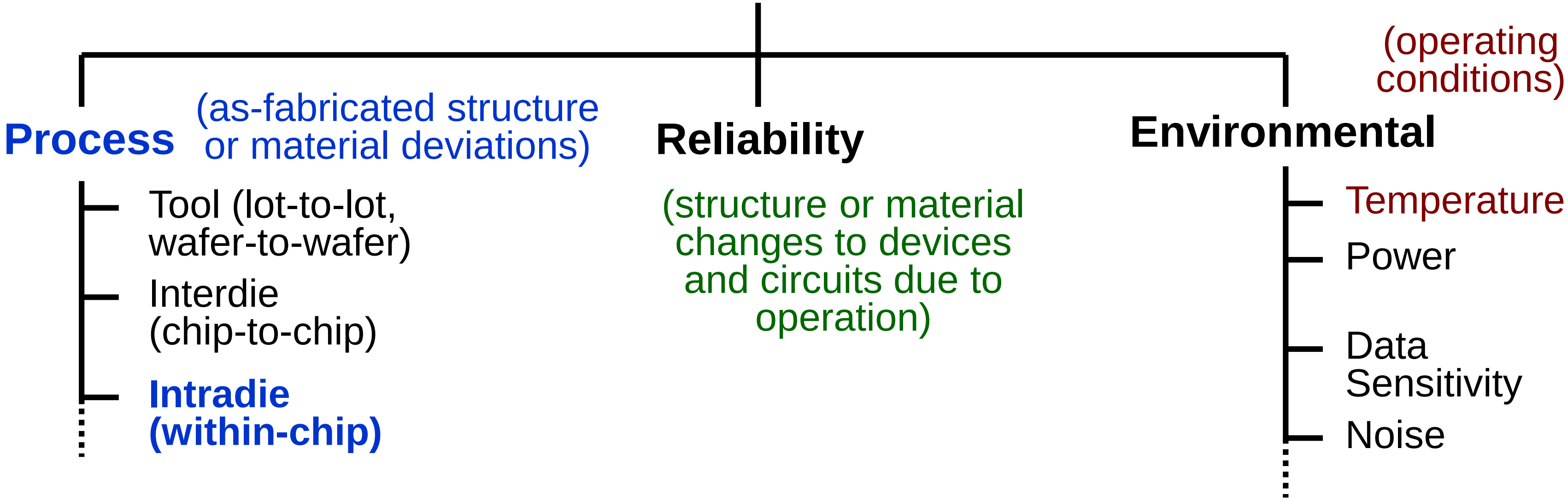
Problem: Variation in Photonic Process/Device/Circuits

- ❑ **Variation in photonic ICs arise with scaling & complexity…**



Process (as-fabricated structure or material deviations)

- Tool (lot-to-lot, wafer-to-wafer)
- Interdie (chip-to-chip)
- **Intradie (within-chip)**

Reliability

(structure or material changes to devices and circuits due to operation)

Environmental (operating conditions)

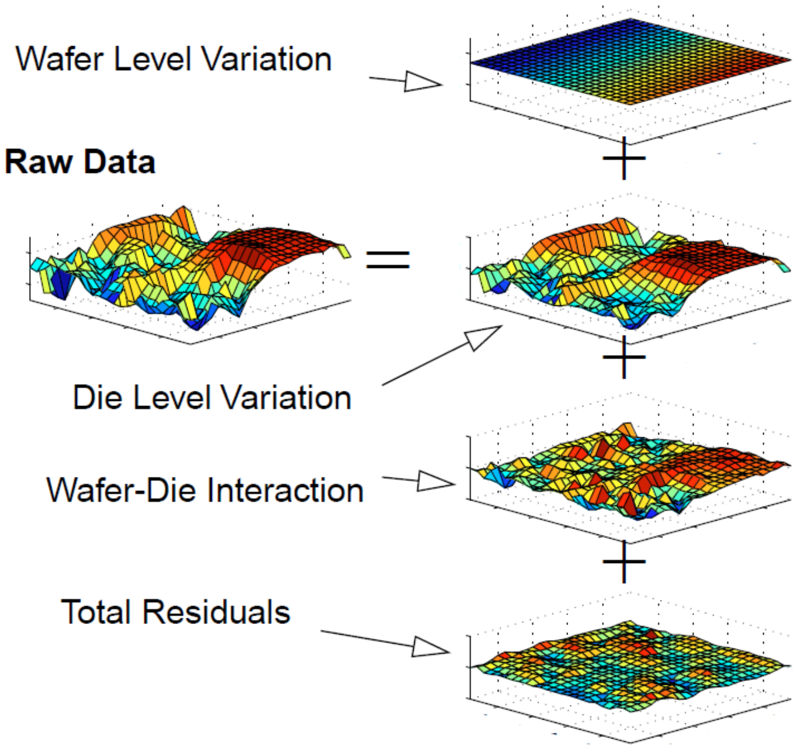
- Temperature
- Power
- Data Sensitivity
- Noise

Solution Approach: Design for Manufacturability

- ❑ Requires *understanding* of variations
  - Research focus: – process variations: *measurement & modeling*
    – photonic device & circuit: *impact analysis*
    – *mitigation*: design optimization & robust design
- ❑ Design for Manufacturability (DFM) necessary to achieve photonic circuit and system specifications in face of above variations

Decomposition/Modeling of Variation

$$P = P_0 + P_W(x,y) + P_D(x,y) + P_I(x,y) + P_\epsilon$$



Each device on each chip is subject to a combination of variations:

- P_0: nominal parameter value
- $P_W(x,y)$: **wafer-level variation**
  - Position or spatially dependent
  - Sometimes approximated as $P_W(i,j)$ offset for each chip (the same for all devices on that chip) based on worst-case corners or Gaussian model
- $P_D(x,y)$: **chip- or die-level variation**
  - Within-die spatially dependent
  - Systematic (highly repeatable) layout dependent models for within-die pattern
  - Separation-distance correlated random models also sometimes used
- $P_I(x,y)$: wafer-die interaction
  - Usually ignored (folded into residual)
- P_ϵ: **residuals/random variation**
  - Typically modeled as a Gaussian random variable, different for each device

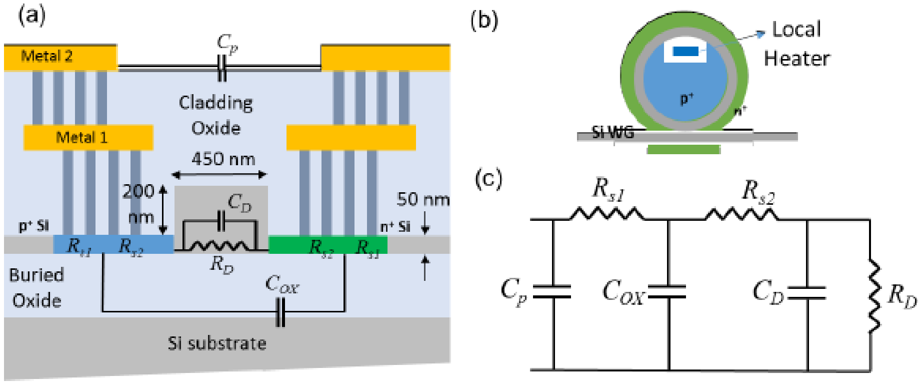
Photonics Process Variation: Examples and CAD/DFM Approaches

- ❑ Wafer-Scale Variations
  - Wafer-scale spatial decomposition and modeling
  - Sensitivity analysis, DOE, and RSM
  - Worst case/corner analysis of device/circuit impact

- ❑ Chip-Scale Variations
  - Separation distance correlation models
  - Physical or empirical models of layout pattern dependencies
  - Dummy fill approaches to minimize layout pattern effects

- ❑ Random, Correlated, and Combined Variations
  - Statistical models of variation sources
  - Monte Carlo and sampling based simulation
  - Design centering and robust design

Spatial Decomposition of Process Variations – Silicon pin Microring Modulators



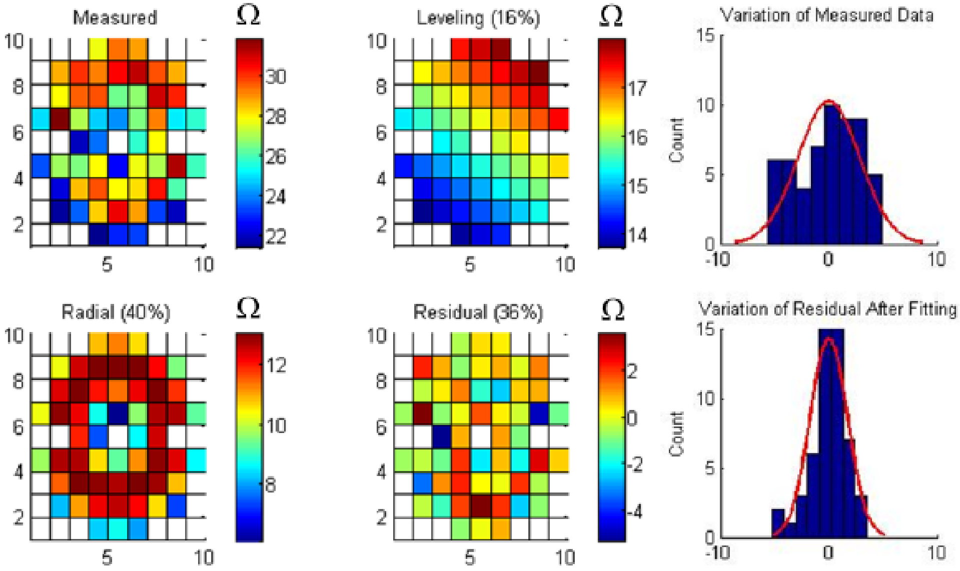
Device:

a) Cross section of 5 um radius microring 250nm/50nm Si rib waveguide

b) Planar view of Si pin microring modulator and local heater

c) Small signal pin diode circuit model

Problem: what are the wafer-scale variations that the ring and heater are sensitive to?



Approach:

- ☐ Decompose wafer spatial variation into **leveling** and **radial** components
- ☐ Use those patterns to reason about process variation sources

Results:

- ☐ R_D measured/fit for 61 die; perform spatial decomposition of variations:
  - 16% leveling; 40% radial; 36% other
- ☐ Suggests
  - Leveling variation due to waveguide width variation (litho)
  - Radial variation due to SOI thickness and dry etch depth variation

R. Wu et al., OIC2016. (UCSB/HP)

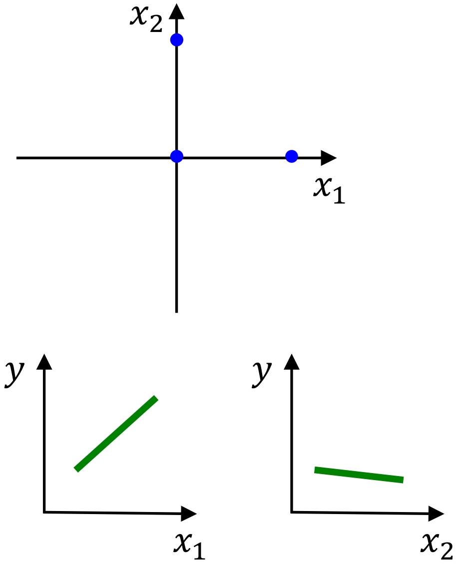
Sensitivity Analysis, DOE and RSM

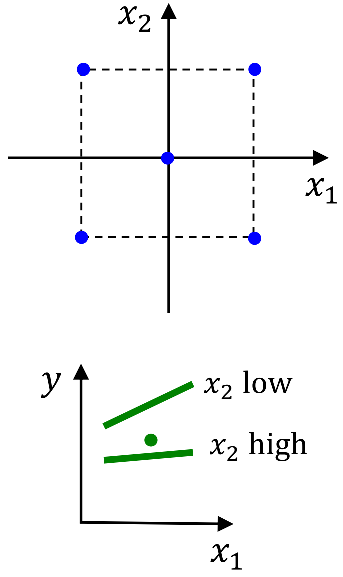
Sensitivity Analysis

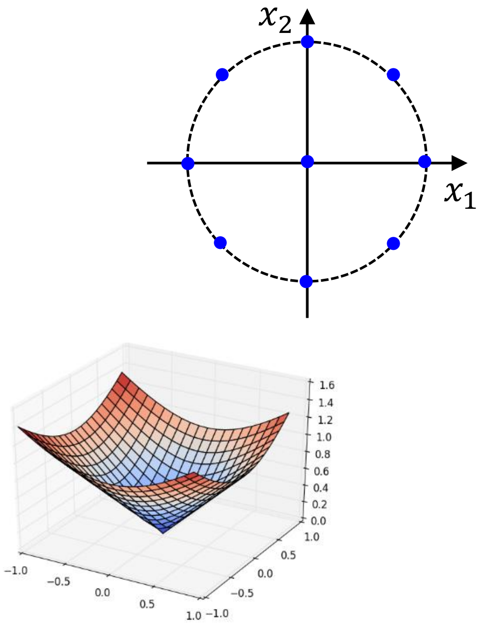
- “One variable at a time” simulations or experiments
- Provides nominal response, and relative impact of inputs: $\boldsymbol{y}_0, \frac{dy}{dx_1}$, and $\frac{dy}{dx_2}$ but not interactions

Design of Experiments (DOE)

- Multifactor simulations or experiments that are better able to map/explore design spaces
- Identification and modeling of interactions
- Typical DOEs:
  - Corner points + center point: interactions; (non)linearity
  - Central composite: polynomial response surface models (RSM)
  - Latin hypercube sampling (LHS): control number of simulations in high dimensional cases





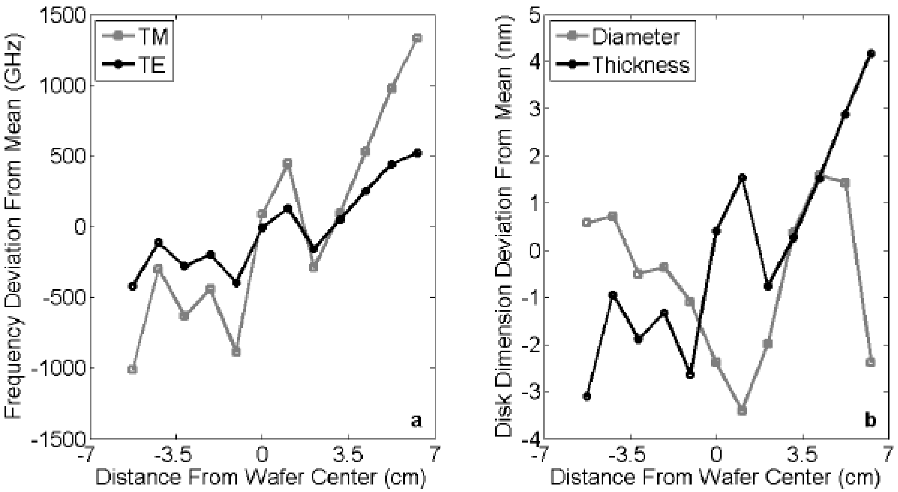


Wafer-Level Silicon Layer Thickness Nonuniformity Impact on Microdisk Resonators

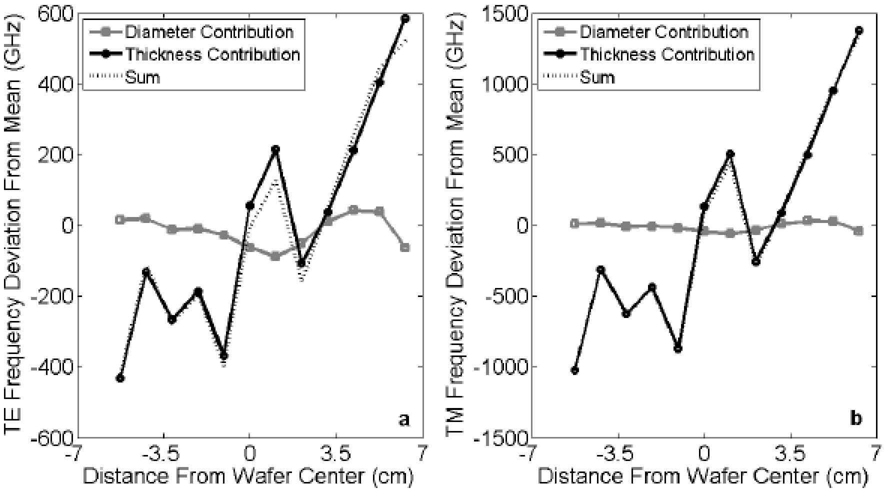
Process: 150 mm SOI wafers with 260 nm silicon

Device: 6 um diameter microdisk resonator coupled to a ~370 nm wide Si waveguide with gap of ~330 nm between waveguide and disk.
16 replicates at different wafer locations.

- Approach: sensitivity simulations to infer linewidth (diameter) and thickness variation contributions
- Result: Thickness non-uniformity on the SOI silicon wafer determined to be the driving factor for deviation in the devices tested



(a) Measured variation in resonant frequency for the TE mode. (b) Simulated deviation in diameter and thickness from FE modesolver required to produce the measured frequency variations.



Calculated contributions of thickness and diameter variation to the (a) TE and (b) TM resonances.

Inferred thickness variations consistent with expected Si layer thickness range of ±4 nm.

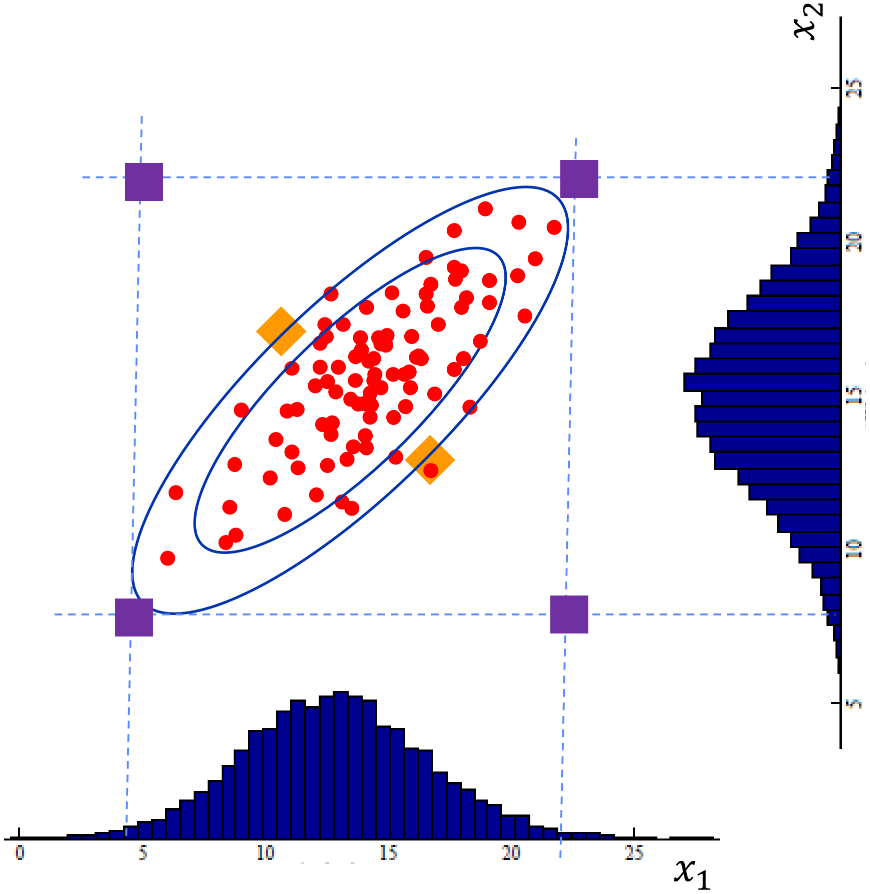
W. A. Zortman et al., paper IMC5, OSA/IPNRA/NLO/SL 2009. (Sandia)

Worst-Case/Corner Analysis

Goal: Verify/achieve design across range of die-to-die variations

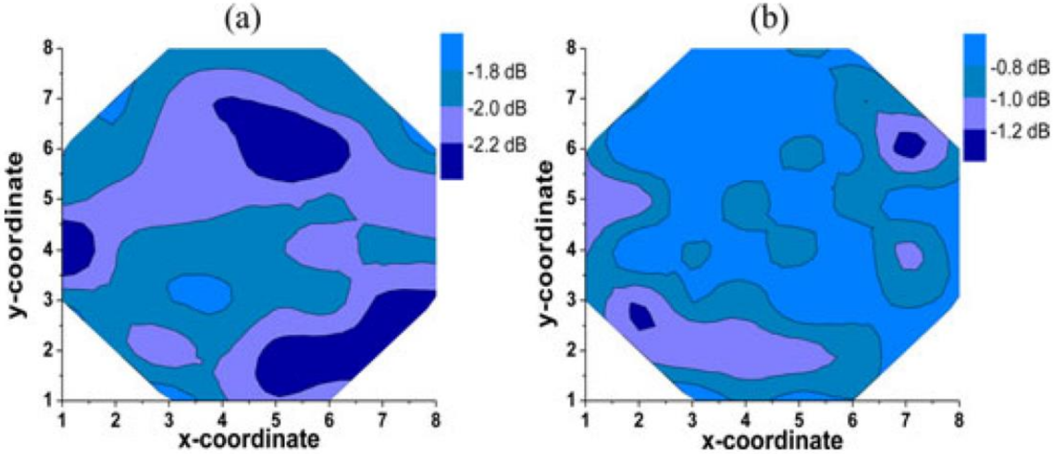
Classic Approach:
“Worse-Case/Corner Analysis”

- ❑ For each design/process parameter, consider corners at e.g., $\pm 2\sigma$ or $\pm 3\sigma$
- ❑ For *n* parameters, have 2^n combinations of corners to check
- ❑ But if parameters are *correlated* then some combined univariate corners will never occur (joint pdf extremely small)
- ❑ Could consider 2^n “multivariate corners” in orthogonalized *n*-dimensional space
  - Requires knowing correlation structure
  - Alternative: if know correlation structure, sampling methods are possible
- ❑ Corner analysis difficult to use for within-die variation
  - If *c* is number of components in circuit, then 2^{nc} corner simulations!



Wafer Level Variation – Waveguide Loss

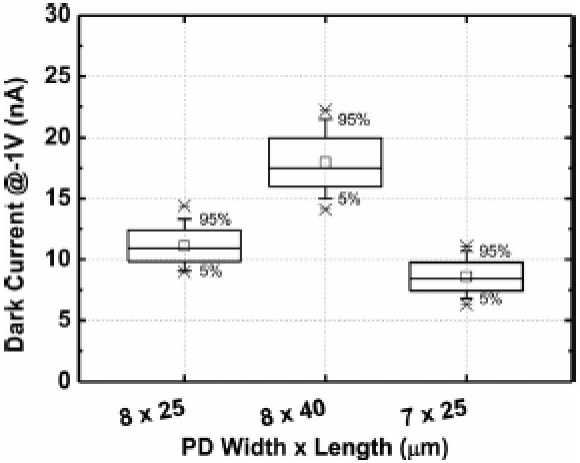
- ❑ Wafer-level map of (a) Si channel waveguide and (b) Si rib waveguide losses from a Si passives pilot wafer fabricated in GF. The WG width was 500 nm and slab thickness for the rib WG was 90 nm. Average WG loss was ~2 and ~0.8 dB/cm for Si channel and Si rib WG, respectively. A total of 52 dies were measured.

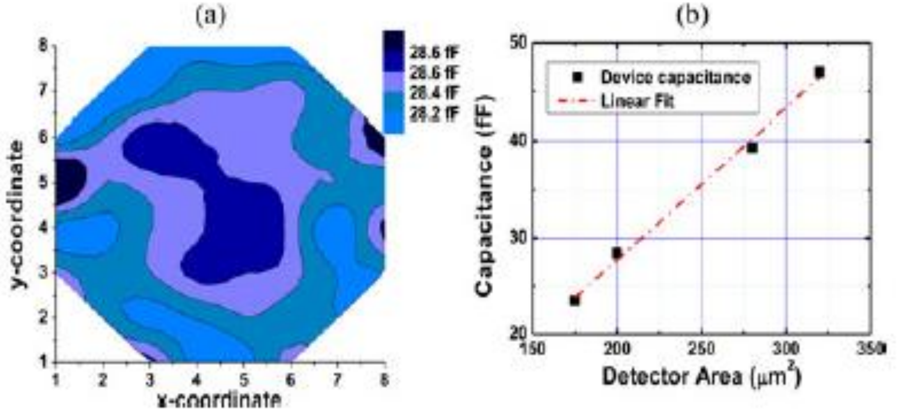


- ❑ Observations:
  - ▪ Spatial correlation in losses: chip-to-chip and (smaller) within-chip
  - ▪ Optical propagation loss distributions with std. dev. of ~0.2 dB/cm; bound or provide range in losses: ~1.6 to 2.4 dB, ~0.6 to 1.2 dB

A. E.-J. Lim et al., J. Sel. Topics in Q. Electronics, vol. 20, no. 4, July/Aug. 2014. (IME)

Wafer Level Variation – Ge Photodetectors





- ☐ Statistical distribution for waveguided vertical pin Ge photodetector dark current at -1V reverse bias, at different device dimensions. 52 dies measured on wafer.

a) Device capacitance at -1V bias plotted in a wafer map showing uniformity with mean capacitance of 28 ± 0.28 fF for 8x25 um photodetector.

b) The device capacitance scales linearly with detector area.

A. E.-J. Lim et al., J. Sel. Topics in Q. Electronics, vol. 20, no. 4, July/Aug. 2014. (IME)

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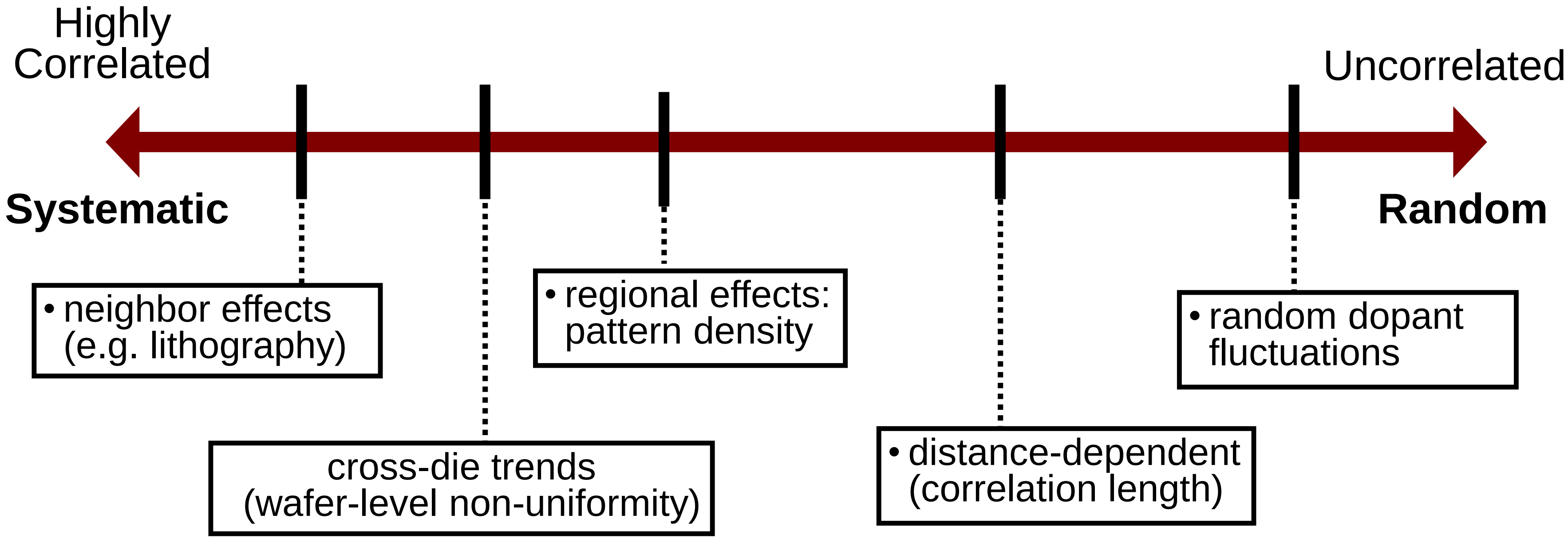
Within-Chip Spatial Variations



Highly Correlated

Uncorrelated

Systematic

Random

- neighbor effects (e.g. lithography)

cross-die trends (wafer-level non-uniformity)

- regional effects: pattern density

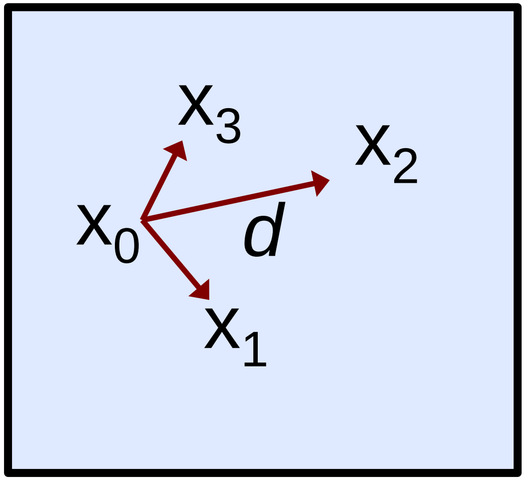
- distance-dependent (correlation length)

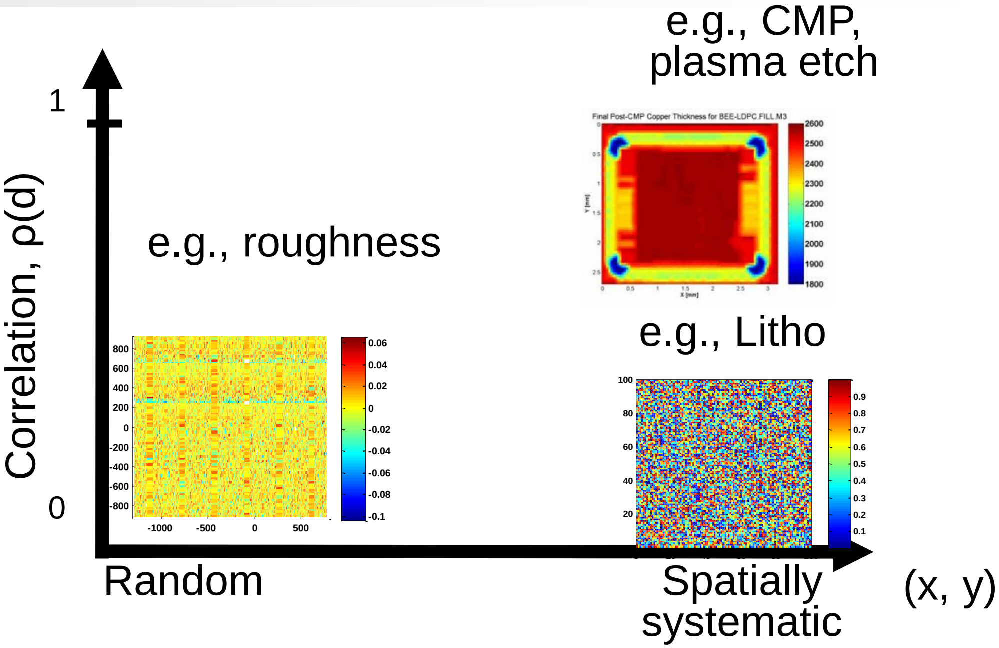
- random dopant fluctuations

- ❑ Spectrum of spatial variation signatures or dependencies
- ❑ May have very different impact on photonic devices and circuits:
  - ▪ E.g. random variations in long paths may “average out”
  - ▪ Correlated variations can help or hurt
    - – “common mode” offsets which don’t affect PIC
    - – Or, accumulation of correlated variation

Within-Chip Spatial Variations

$$\rho_{x,x\pm d}(d) = \frac{Cov(x,x\pm d)}{\sigma_x^2}$$

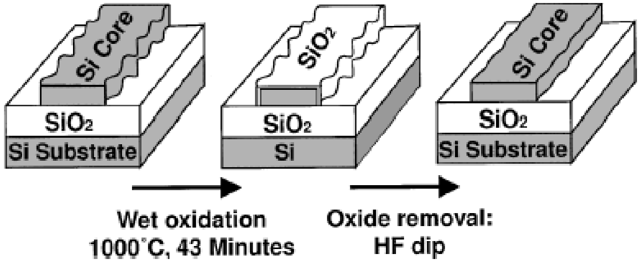




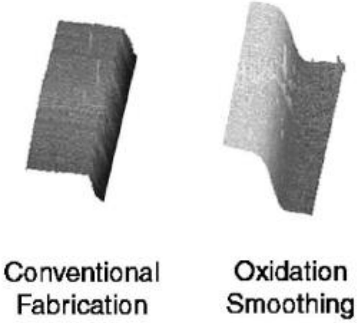
- ❑ Multiple spatial variation axes depending on physical source
- ❑ Differing impact on photonic devices and circuits:
  - ▪ Systematic vs. Random → Die-to-die predictability
    - – Same variation for all chips or variation different for each chip
  - ▪ Spatially Correlated vs. Uncorrelated
    - – “Common mode” offsets which don’t affect circuit
    - – Averaging of uncorrelated variation in long paths
    - – Or accumulation of correlated variation

Waveguide Sidewall Roughness

a) Fabrication steps of oxidation smoothing waveguides. The additional steps that the waveguides go through after they are patterned by photolithography and RIE are shown.



b) AFM images of top and sidewall of waveguides. Conventional waveguide has rms σ = 10 nm and correlation length L_c = 50 nm. Oxidation smoothed waveguide has rms σ = 2 nm and L_c = 50 nm.

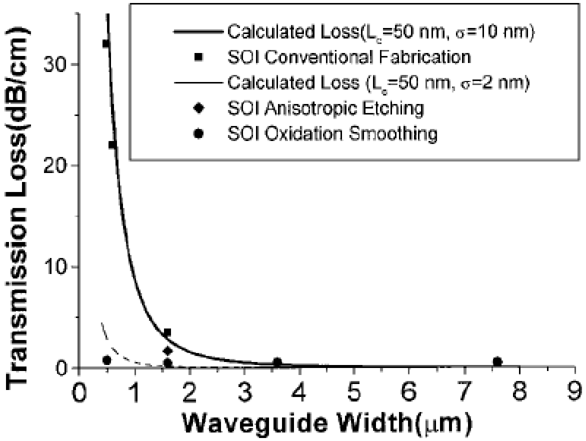


c. Resulting waveguide transmission losses depend on sidewall roughness

- Scattering loss α_S related to rms roughness σ:

$$\alpha_s = 4.3 \frac{\sigma^2}{\sqrt{2}\,k_0 d^4 n_1} g f_e$$

- Measured transmission losses



- Losses reduced from 32 dB/cm to 0.8 dB/cm for single mode waveguide width of 500 nm.

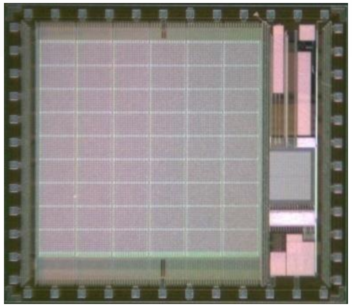
K. K. Lee et al., Optics Letters, vol. 26, no. 23, Dec. 2001. (MIT/UWM)

Example from IC World – Variation Test Circuits: V_T

- ☐ Take advantage of exponential dependence of V_T in sub-threshold
- ☐ Measure currents in sub-threshold regime and compute ΔV_T:

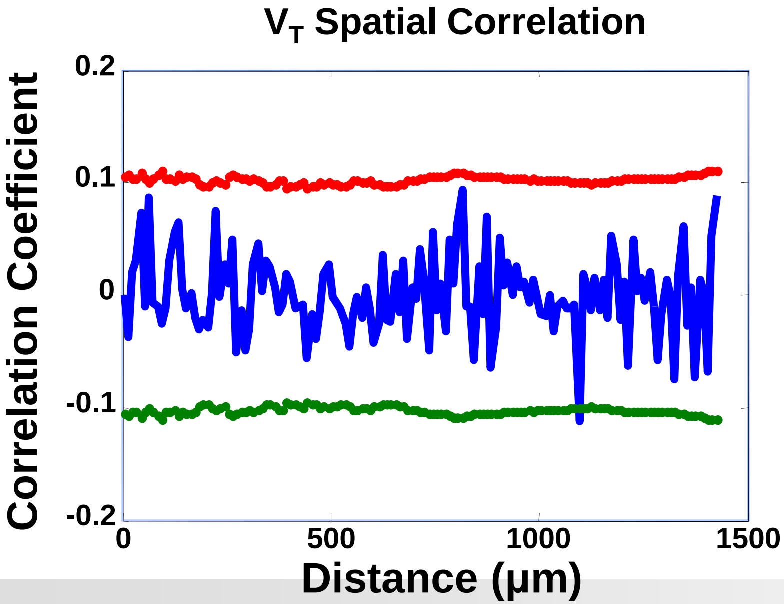
$$\triangle V_T = nV_{th} \cdot ln\left(\frac{I_{D_1}}{I_{D_2}}\right)$$

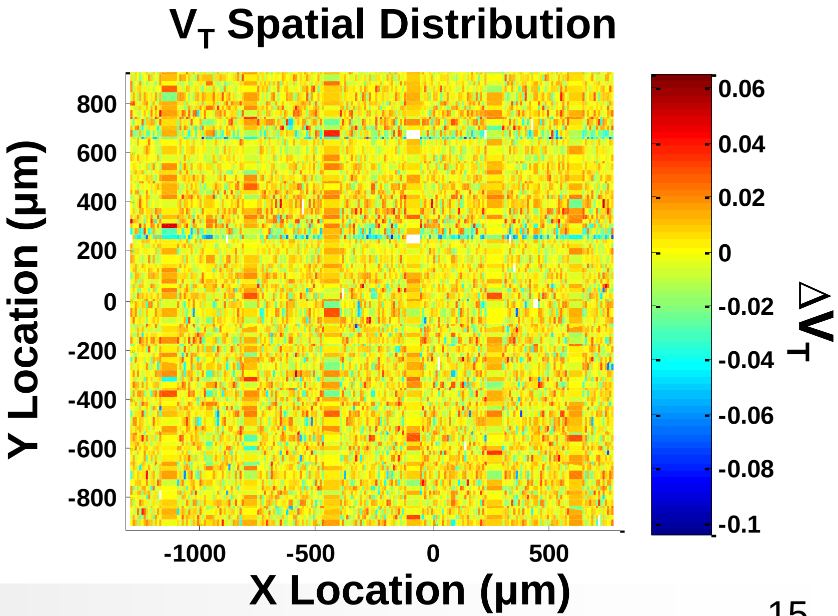
- ☐ Surprising result: No statistically significant spatial correlation or dependence on separation distance *D*



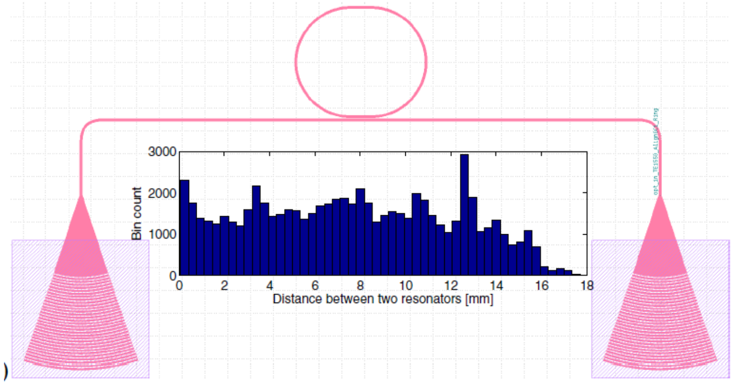
Vt Test Chip Die Photo

$$\boxed{\sigma^2(V_{T_0}) = \frac{A^2_{V_{T_0}}}{WL} + S^2_{V_{T_0}} D^2}$$





Effect of Spatial Separation Distance on Resonator Wavelength Mismatch

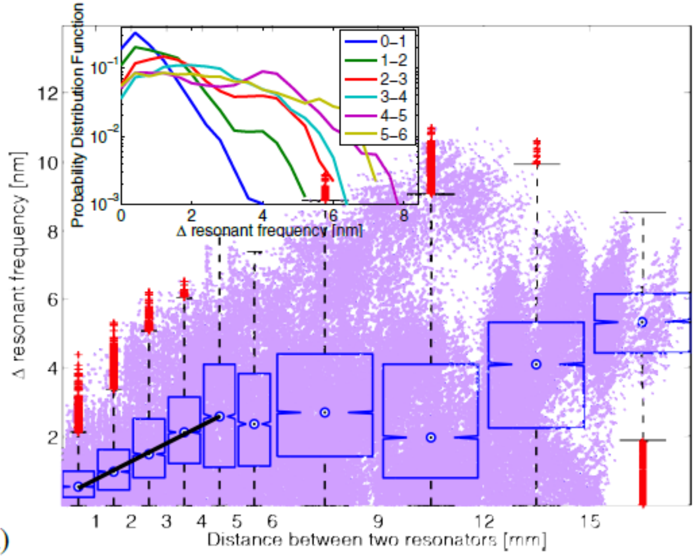


Device:

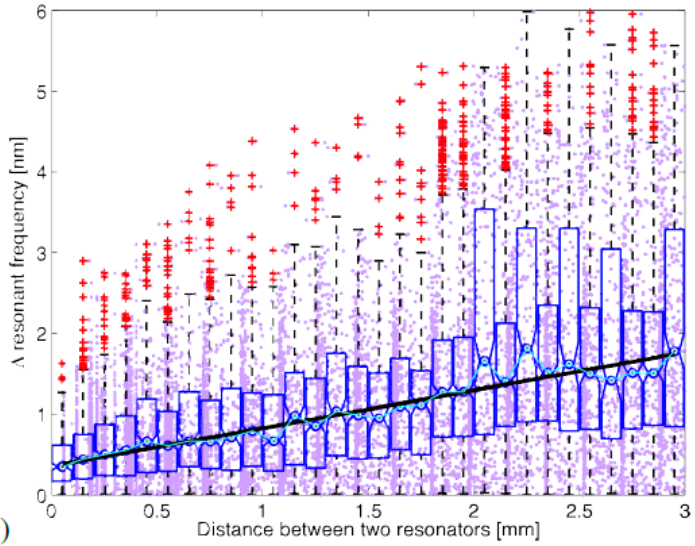
- 371 identical racetrack resonators (12 um radius) on a 16x9 mm chip.
- Devices between 60 um and 18 mm apart
- 68,635 different separation distance combinations

Results:

- Strong dependence of difference in resonator wavelength $\bar{\lambda}_{\text{ring}}$ on separation distance
- Linear dependence for *d* < 5 mm: $\bar{\lambda}_{\text{ring}} = 0.47\frac{nm}{mm}\cdot d + 0.35nm$



a)



b)

Conclusion: strong spatial correlation in sources of resonator variation

L. Chrostowski et al., paper Th2A.37, OFC 2014. (UBC)

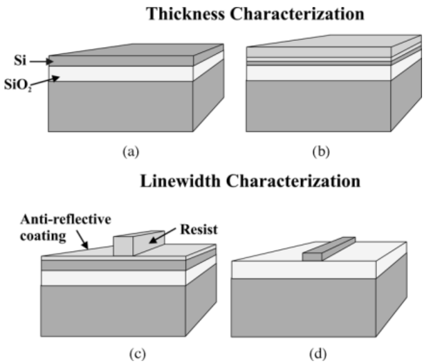
Wafer-Level vs. Die-Level Variation in Silicon Waveguides and Devices (1)

Device:

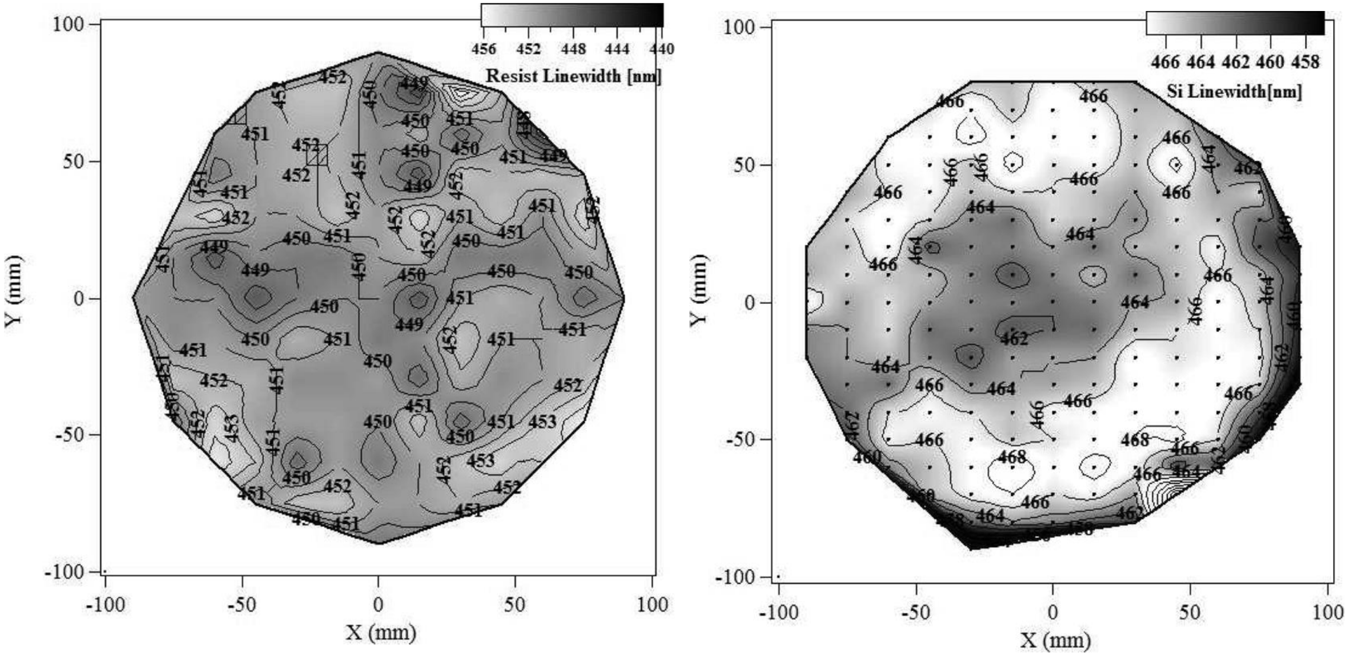
- ❑ Waveguides at 9 locations within each die
- ❑ Multiple die per wafer

Process:

- ❑ 200 mm SOI, 193 nm step and scan



Wafer Scale Variation: (a) Photoresist linewidth after litho; (b) Silicon linewidth after dry etch



Conclusions:

- ❑ Little wafer-scale lithography variation
- ❑ Circular post-etch variation attributed to chamber scale etch-rate variation due to plasma nonuniformity

S. K. Selvaraja et al., IEEE J. Sel. Topics in Q. Electron., vol. 16, no. 1, Jan./Feb. 2010. (Ghent/IMEC)

Wafer-Level vs. Die-Level Variation in Silicon Waveguides and Devices (2)

Chip Scale Process Variation: Linewidth uniformity within a die after lithography, after etch:

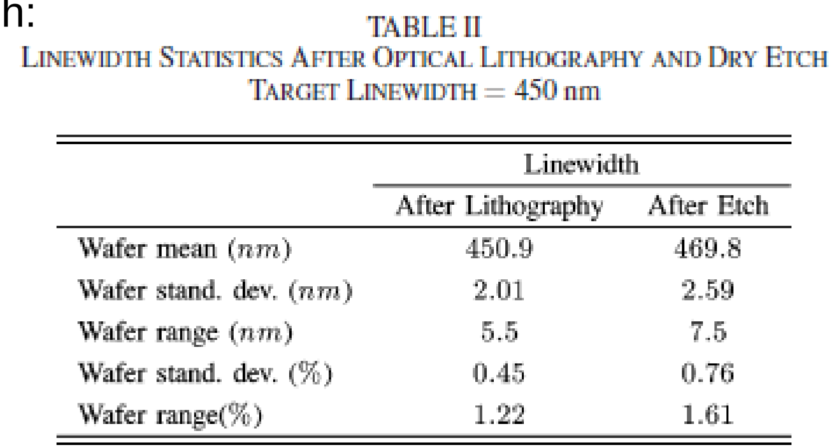
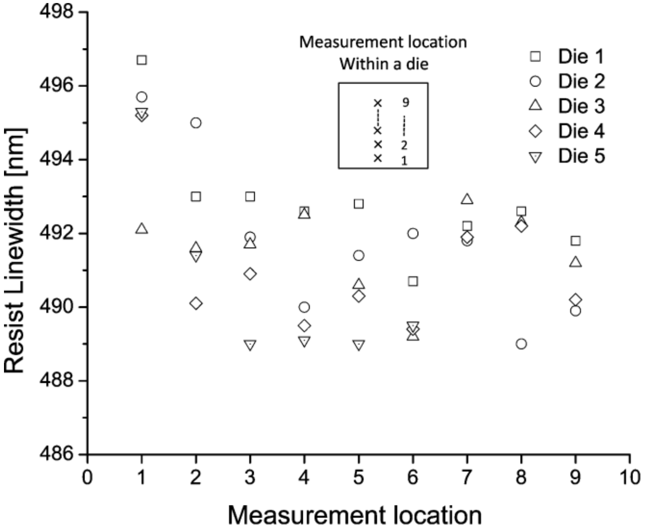


TABLE II

LINEWIDTH STATISTICS AFTER OPTICAL LITHOGRAPHY AND DRY ETCH

TARGET LINEWIDTH = 450 nm

	Linewidth	
	After Lithography	After Etch
Wafer mean (nm)	450.9	469.8
Wafer stand. dev. (nm)	2.01	2.59
Wafer range (nm)	5.5	7.5
Wafer stand. dev. (%)	0.45	0.76
Wafer range(%)	1.22	1.61



Chip Scale Device Variation: Separation distance dependence in ring, MZI and AWG variation:

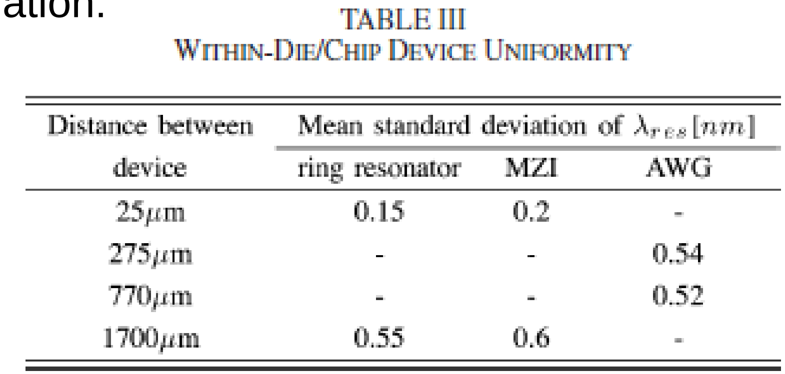
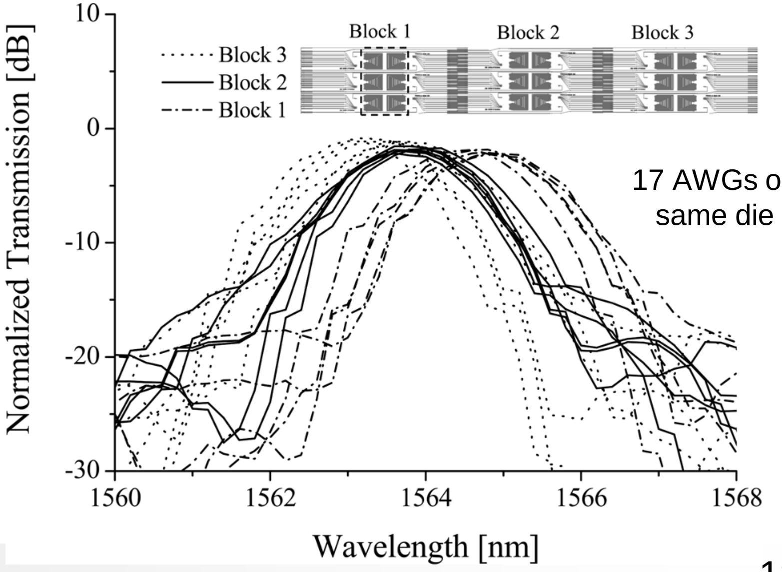


TABLE III

WITHIN-DIE/CHIP DEVICE UNIFORMITY

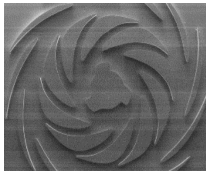
Distance between device	Mean standard deviation of λ_{res} [nm]		
	ring resonator	MZI	AWG
25μm	0.15	0.2	-
275μm	-	-	0.54
770μm	-	-	0.52
1700μm	0.55	0.6	-



17 AWGs on same die

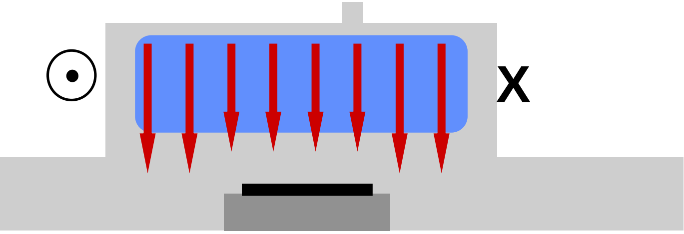
S. K. Selvaraja et al., IEEE J. Sel. Topics in Q. Electron., vol. 16, no. 1, Jan./Feb. 2010. (Ghent/IMEC)

Process Variation – Feature/Chip/Wafer-Scale Models of Plasma Etch

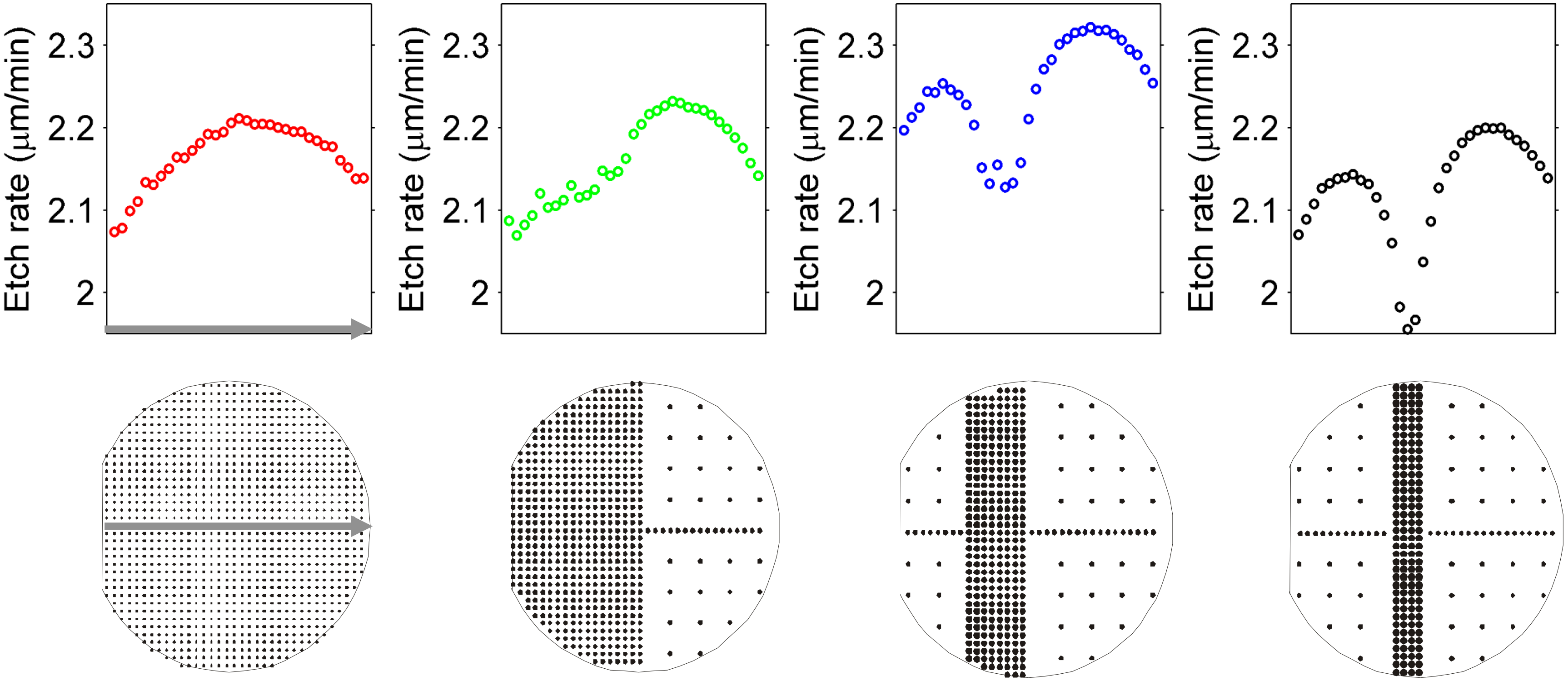


spatial variation

- **feature-scale**
  - **aspect ratio-dependent etching (ARDE)**
- **across-chip and between-chip**
  - **competition for reactants; diffusion**
- **wafer/chamber-scale**
  - **ion and radical flux distribution**
  - **wafer-level 'loading'**



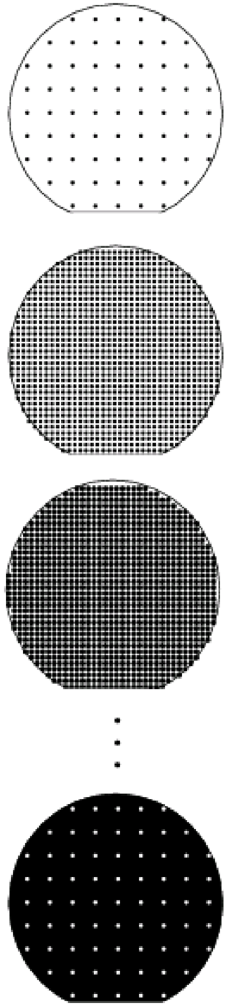
Plasma Etch: Layout Pattern-Dependent Variation



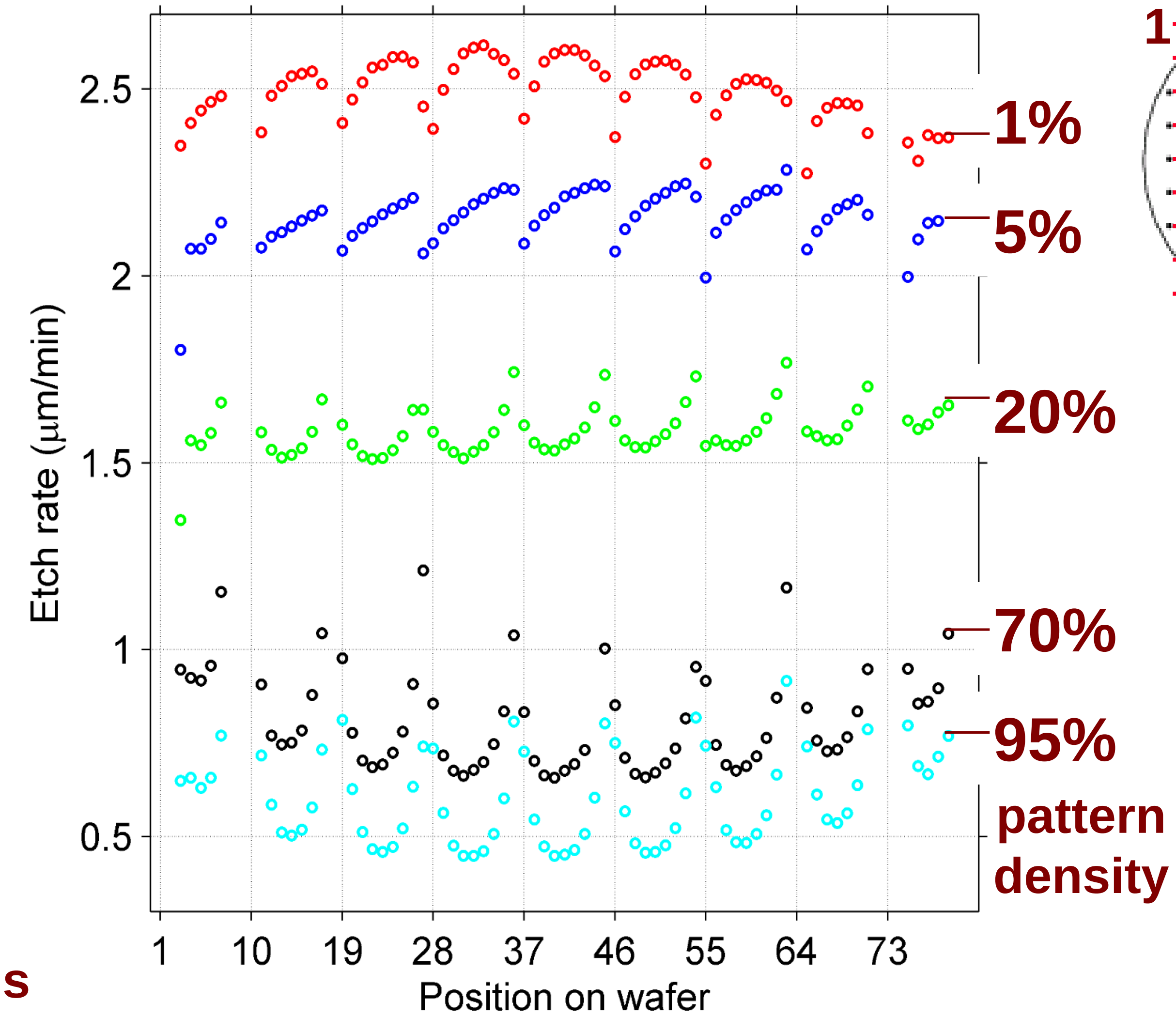
Experimental results using wafers with

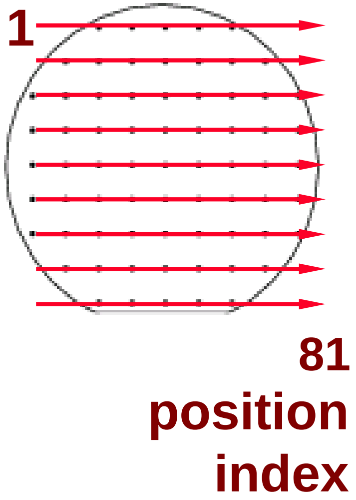
- **Average pattern density 5% throughout**
- **But density localized to differing extents**

Plasma Etch: Chamber-Scale Variation



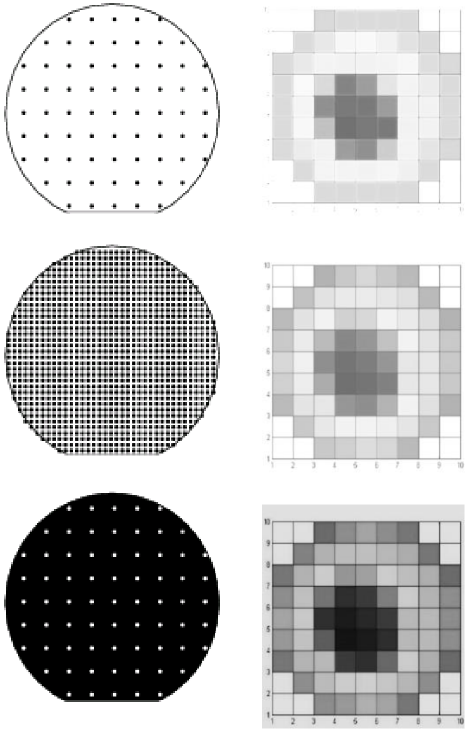
test patterns





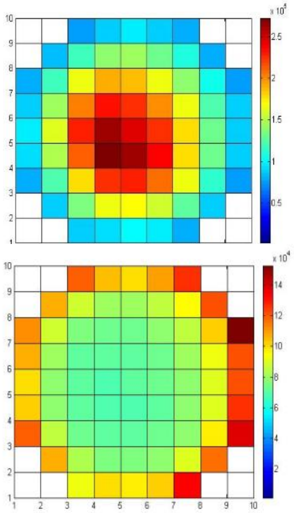
Predictive Models for Etch Depth/Width Variation

Chamber-scale variation



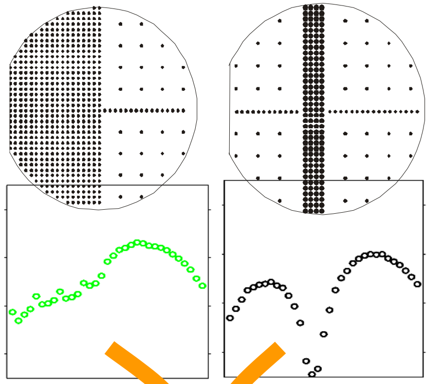
A

B

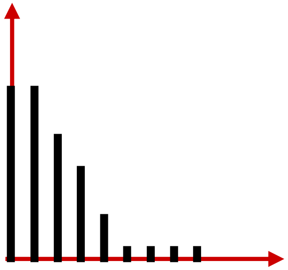


Reactant + Ion Effects

Chip-scale variation



spatial averaging filter

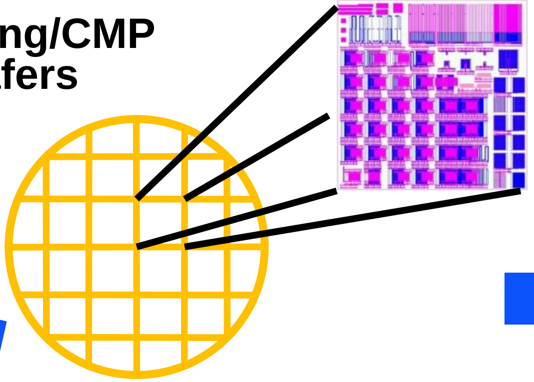


radial distance

Pattern Density, Loading, Die Location on Wafer

CMP/Plating Variation Modeling

Electroplating/CMP Test Wafers



Standard test pattern (MIT/Sematech 854 Mask)

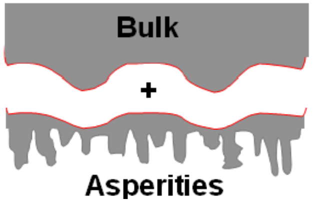
Measure Dishing, Erosion and Copper Thickness

Model Parameter Extraction

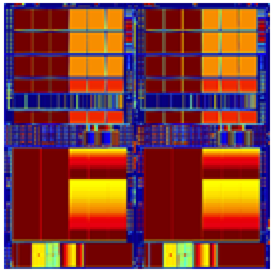
Calibrated Copper Pattern Dependent Model

CMP Process

- Fixed slurry, pad: effective Young’s modulus, characteristic asperity height, removal rate
- Fixed polish process settings: pressure, speed, etc.
- Variable polish times



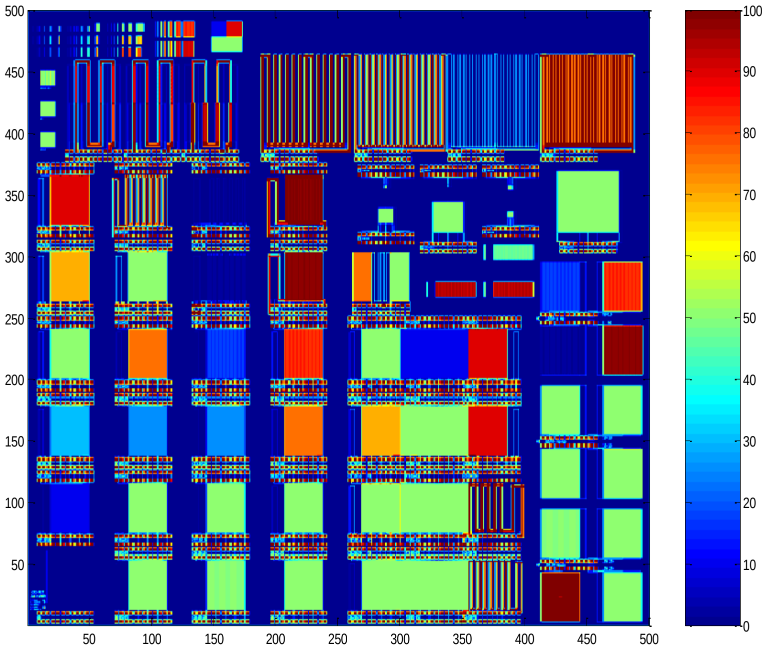
Product Chip Layout



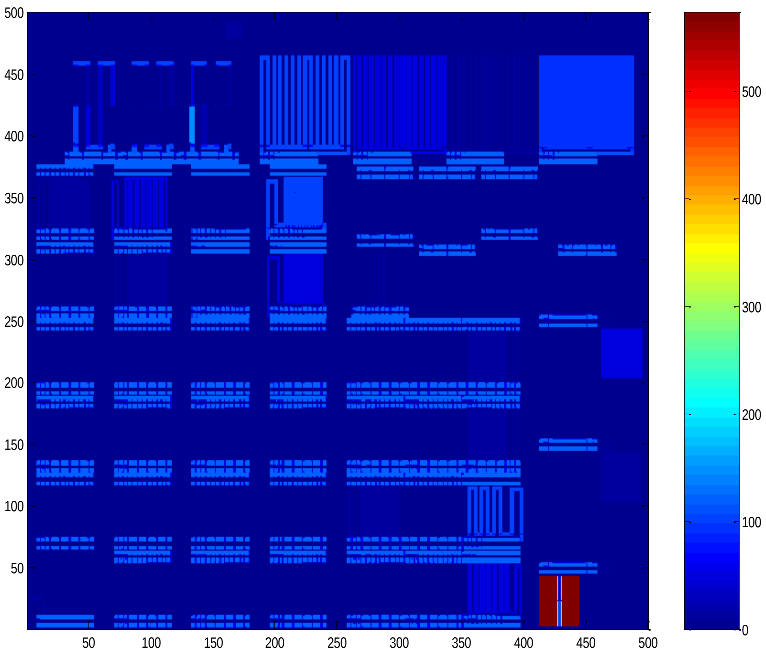
Chip-Level Simulation

- **Prediction of clearing time, dishing and erosion**
- **Assess and guide dummy fill insertions**

Coupled Plating & CMP Simulation: MIT/Sematech 854 M1 Mask



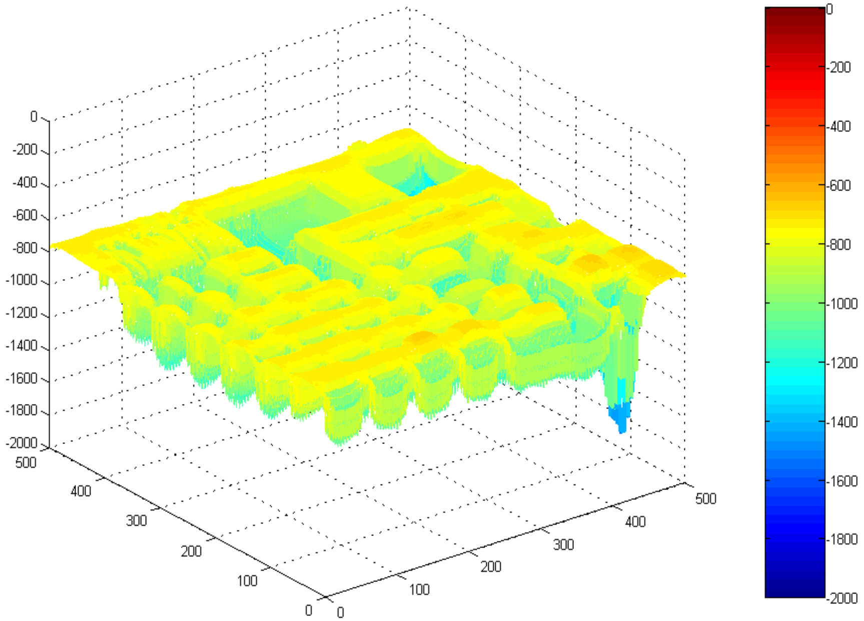
Pattern density map (%)



Line width map (μm)

Each map on 40μm x 40μm grid cells

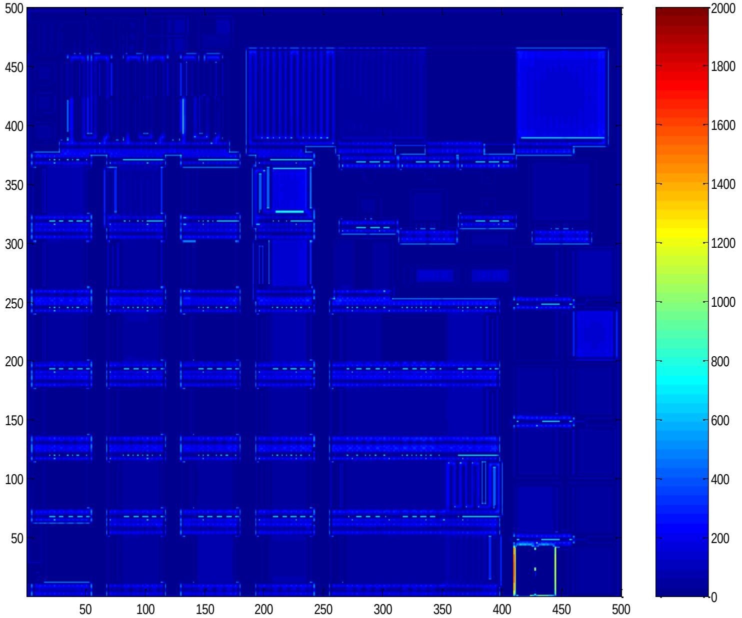
Copper Electroplating and CMP Simulation



Envelope map (Å)

Simulation result from CMP model

Step height map (Å)



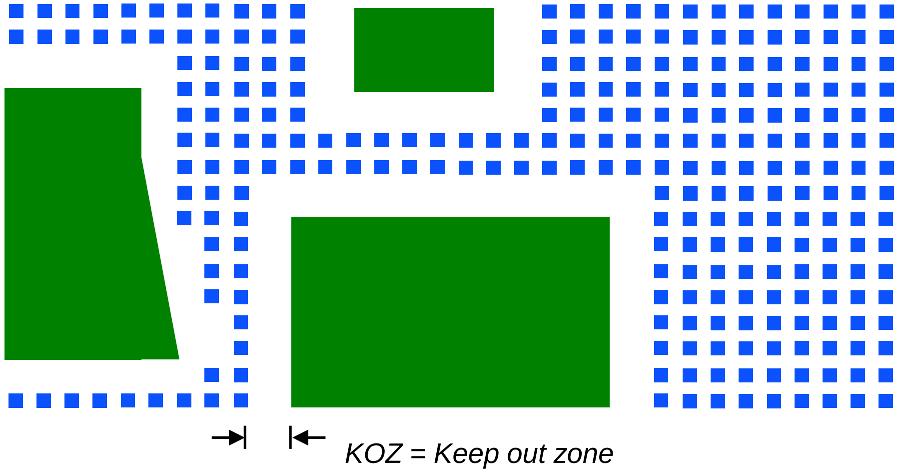
Finished removing barrier:

- Remaining step height (dishing)
- Substantial envelope variation (erosion)

Pattern Density Compensation – Dummy Fill Strategies

Approach:

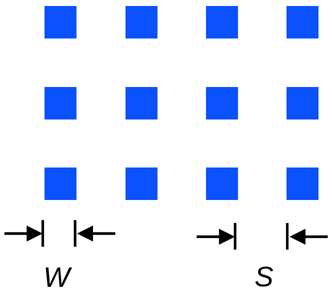
- ☐ Insert dummy (non-functional) patterns to equilibrate layout pattern density
- ☐ Important in CMP and etch processes
- ☐ Fill: add patterns to “empty” areas
- ☐ Cheese: add “holes” in large patterns



Design Approaches:

- ☐ Template based:
  - Fill/cheese all areas subject to available area, keep out zone, and/or blocking mask constraints
  - Usually fills with a fixed pattern density (e.g., 25%)
- ☐ Algorithmic:
  - Vary pattern (e.g., width, spacing, length of dummy) to achieve desired or needed pattern densities in moving windows
  - Model-based generation related to models of physical process

$$\rho = \frac{W^2}{(W+S)^2}$$



Photonics Process Variation: Examples and CAD/DFM Approaches

- Wafer-Scale Variations
  - Wafer-scale spatial decomposition and modeling
  - Sensitivity analysis, DOE, and RSM
  - Worst case/corner analysis of device/circuit impact

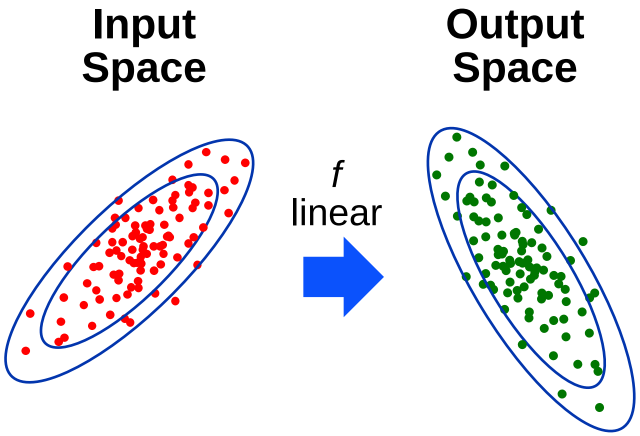
- Chip-Scale Variations
  - Separation distance correlation models
  - Physical or empirical models of layout pattern dependencies
  - Dummy fill approaches to minimize layout pattern effects

- Random, Correlated, and Combined Variations
  - Statistical models of variation sources
  - Monte Carlo and sampling based simulation
  - Design centering and robust design

Statistical Analysis & Sampling Approaches

Monte Carlo or other statistical sampling and analysis methods:

- Alternative to corner analysis
- Requires statistical model of input parameters (pdf, correlation structure, etc.)
- Draw samples based on variation statistics
- Simulate output (samples, pdf, etc.) corresponding to input (samples, pdf, etc.)
- Can accommodate *nonlinear* as well as *linear* input-output functions



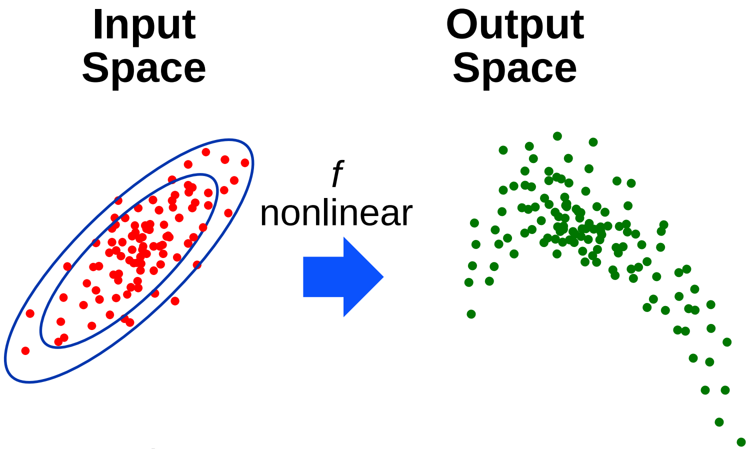
Input Space

f
linear

Output Space

Gaussian

Also Gaussian.
Corners map to
corners.



Input Space

f
nonlinear

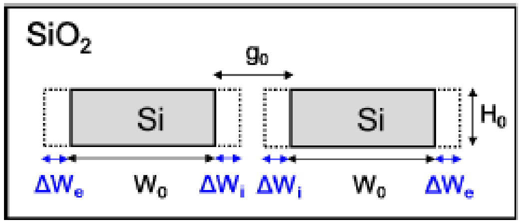
Output Space

Gaussian

Non-Gaussian.
Corners do not
necessarily map to
extremal points.

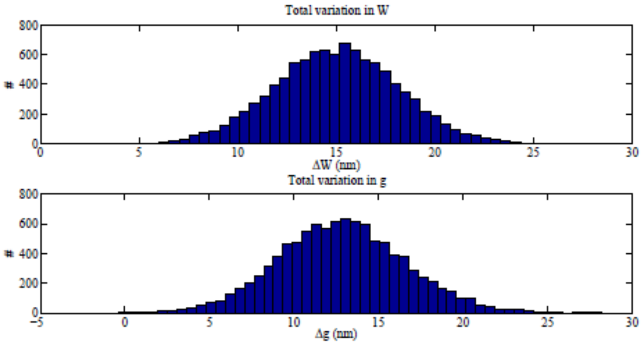
Photonic Coupler: Correlated and non-Gaussian Random Parameters

a) Cross section of an SOI-based directional coupler with nominal width W_0, nominal gap g_0, height H_0, and refractive indices n_{Si} = 3.48, n_{SiO2} = 1.445.



b) Variations in *W* and *g*:

- Each of *W* and *g* modeled as Gaussians



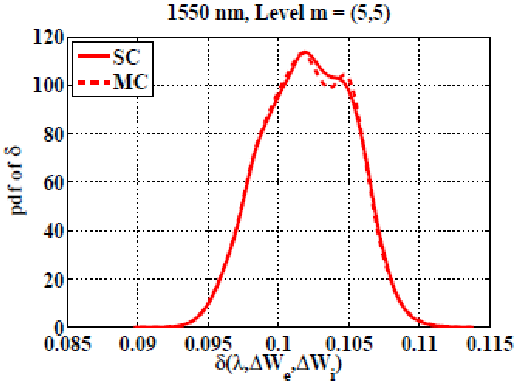
- BUT correlation structure is accounted for:

$$\begin{bmatrix}\Delta W_e\\ \Delta W_i\end{bmatrix} \sim 0.6\cdot N(\vec{\mu}_A,\Sigma_A)+0.4\cdot N(\vec{\mu}_B,\Sigma_B)$$

$$\mu_A=\begin{bmatrix}9\\6\end{bmatrix}\text{nm},\quad \Sigma_A=\begin{bmatrix}6&0\\0&3\end{bmatrix}\text{nm}^2$$

$$\mu_B=\begin{bmatrix}8\\7\end{bmatrix}\text{nm},\quad \Sigma_B=\begin{bmatrix}5&1\\1&4\end{bmatrix}\text{nm}^2.$$

c. Stochastic Collocation (SC) and Monte Carlo (MC) simulations of field coupling coefficient *d*



- Resulting output is non-Gaussian
- SC can be much more efficient than MC: 81 quadrature points (105 sec. cpu time) gives similar accuracy to 10,000 MC points (4800 sec. cpu time).

T.-W. Weng et al., Optics Express, vol. 23, no. 24, Feb. 2015.

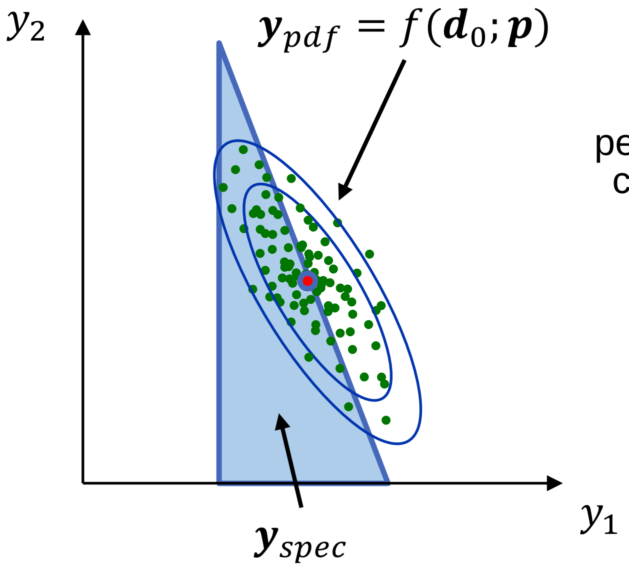
Design Centering for Yield Optimization

Nominal Design:

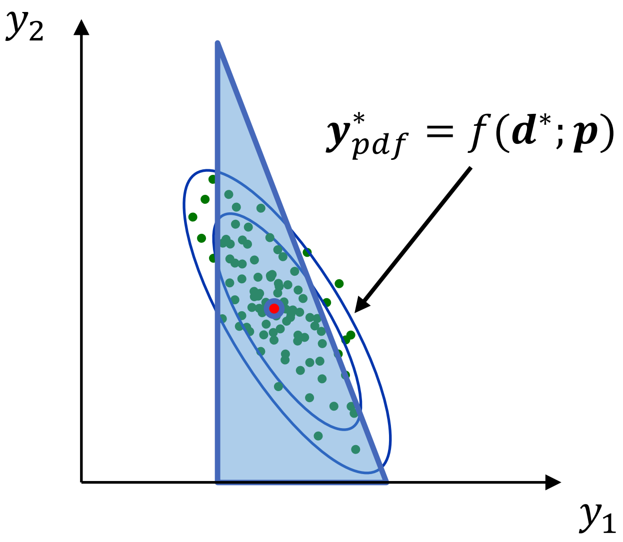
- ❑ Find design choices $\boldsymbol{d}_0$ that achieve performance goals and specification $\boldsymbol{y}_{spec}$
- ❑ A nominal design may meet specs (and in many cases, maximize nominal performance) but have terrible yield over variations $\boldsymbol{p}$

Design Centering

- ❑ Find optimal design choices $\boldsymbol{d}^*$ that achieve performance goals and specification $\boldsymbol{y}_{spec}$
- ❑ But that also maximize yield
  - E.g., intersection of performance specs and centered performance distribution $\boldsymbol{y}^*_{pdf}$

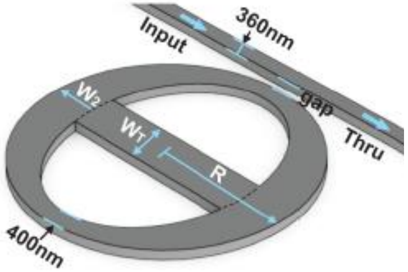


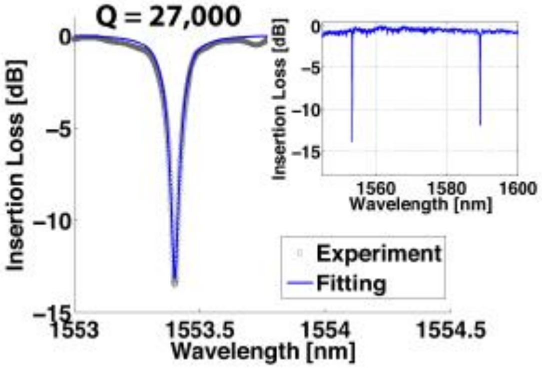
Center performances $\boldsymbol{y}$ by changing design parameters $\boldsymbol{d}$



Robust Design: Reduced Wafer-Scale Frequency Variation in Adiabatic Microring Resonators

Device Design Goal: Adiabatic geometry for high-Q operation, and ***improved manufacturing robustness***





$$\sigma(\lambda)=\sqrt{\left(\frac{\partial\lambda}{\partial T}\sigma_T\right)^2+\left(\frac{\partial\lambda}{\partial R}\sigma_R\right)^2+\left(\frac{\partial\lambda}{\partial W}\sigma_W\right)^2}$$

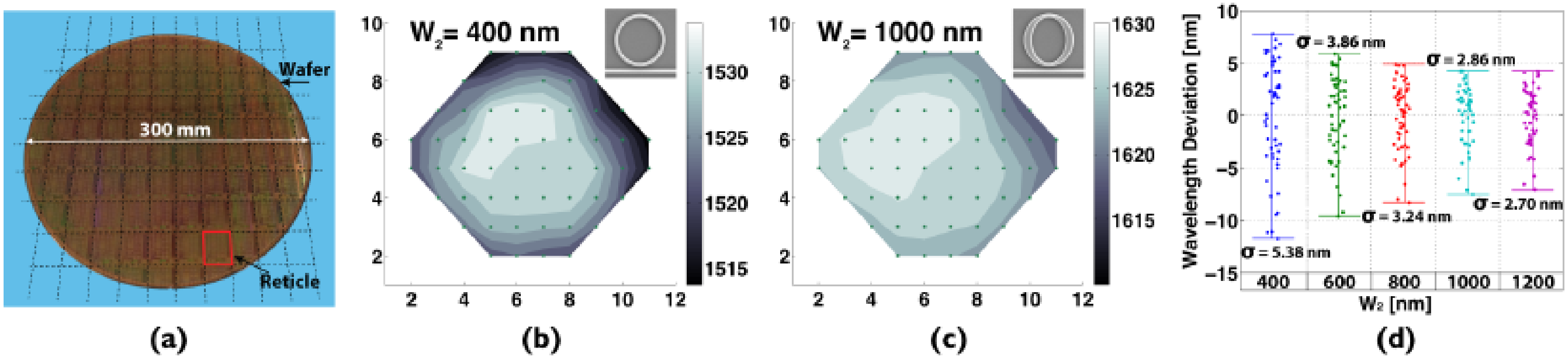
- ☐ Consider **variance sensitivities** of resonant wavelength λ with respect to thickness *T*, radius *R*, and width *W*:

$$\partial\lambda/\partial T = 1.367\ \mathrm{nm/nm}$$
$$\partial\lambda/\partial R = 0.291\ \mathrm{nm/nm}$$
$$\partial\lambda/\partial W = 0.894\ \mathrm{nm/nm}$$

- ☐ Result:

$\sigma(\lambda) = 5.38\ \mathrm{nm}$

$\sigma_W = 5.520\ \mathrm{nm/nm}$ thus W_2 dominates



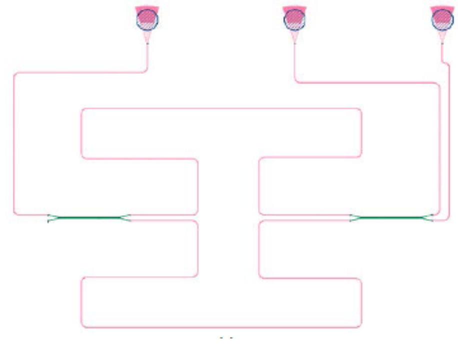
(a) (b) (c) (d)

(a) Fabricated 300-mm wafer with single reticle marked with red rectangle. Wavelength distribution across the wafer for (b) W_2 = 400 nm and (c) W_2 = 1000 nm. The dots represent the position of the measured chips. Insets are the SEMs of the corresponding adiabatic microring resonators. (d) Resonant wavelength variations across the wafer for various W_2 sizes. **Larger W_2 devices are more robust to variation.**

Z. Su et al., paper Th2A.5, OFC 2014. (MIT/CNSE)

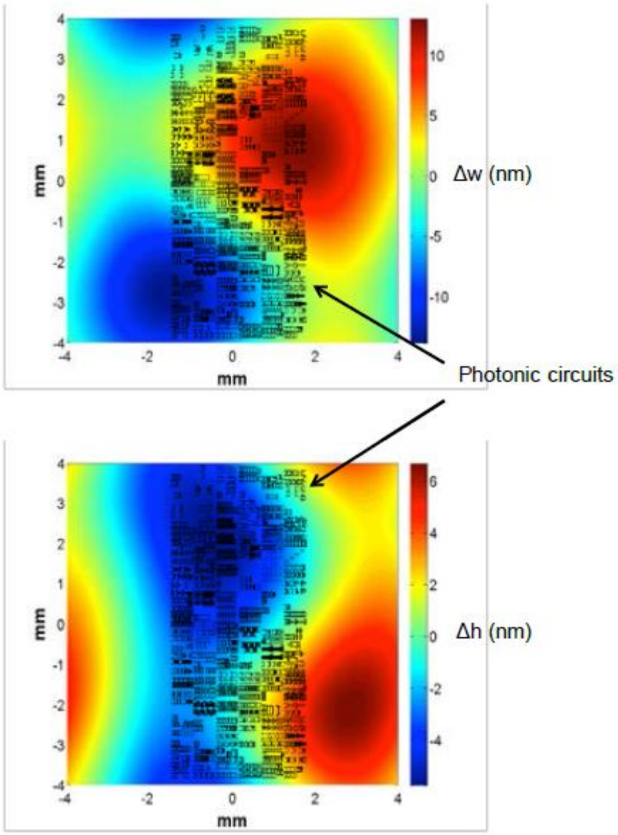
Monte Carlo with Spatial Correlations

a) Balanced Mach-Zehnder Interferometer Test Structure

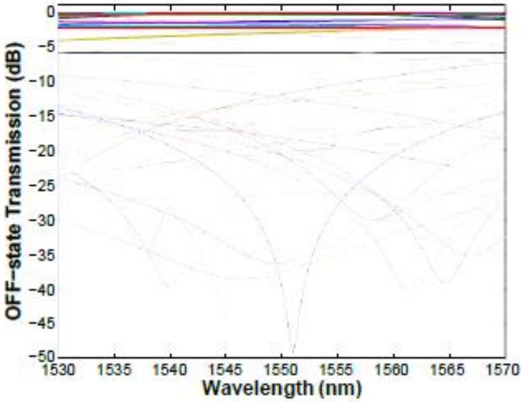


❑ Goal: High extinction ratio at designed wavelength

b) Simulated spatial waveguide linewidth (Δw) and thickness (Δh) deviations across a wafer



c. Monte carlo simulations: off-state transmissions



❑ Result: Extinction ratio of the interferometer is no longer distinguishable due to the spatially dependent phase errors

L. Chrostowski et al., Proc. SPIE Vol. 9751, 2016.

Toward *Statistical* Photonic Device/Circuit Simulation

Device Models

- Components:
  - Laser (rate equation)
  - Optical connector
  - Optical coupler
  - Straight waveguide
  - Photodetector

Modified nodal analysis

Circuit Level

- Differential equation in Matlab:

$$M(x)\frac{dx}{dt} = f(x, u(t))$$

- x: magnitude and phase of E-field envelope
- M(x): mass matrix

☐ Typical implementation: deterministic, with external MC or SC sampling to generate statistical outputs

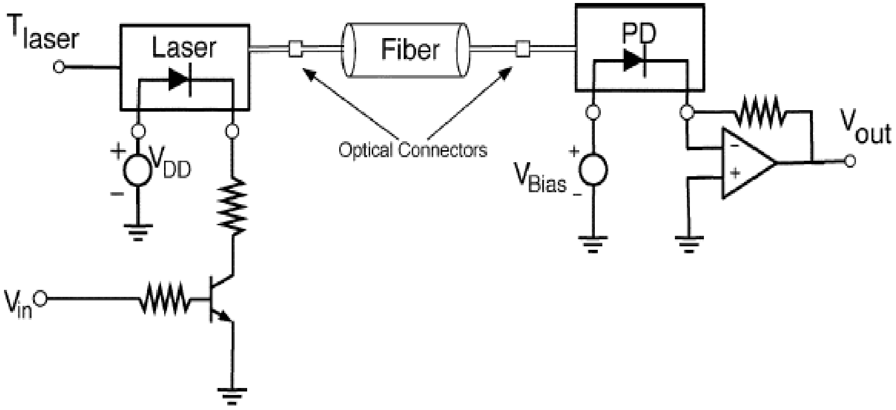
☐ **Alternative: stochastic testing implementation**

- Photonic circuit with variations are described by stochastic equation
- Represent the stochastic solution (e.g., magnitude and phase of electrical field) by stochastic basis functions
- Compute the weights for basis functions by solving a new deterministic equation

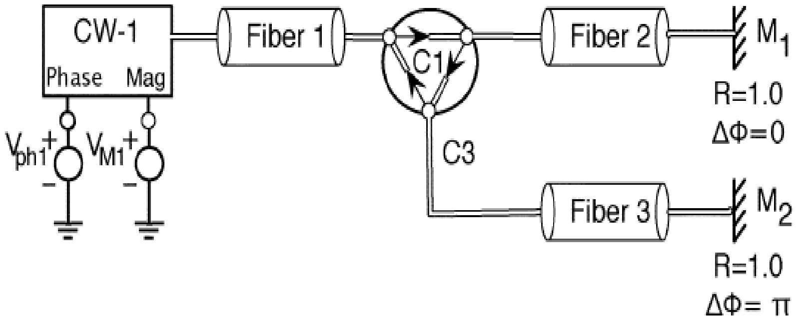
Future Outlook (1): Stochastic Testing Photonic Simulation

- ☐ **Examples for stochastic testing (hard-coded implementation)**

(a) Photonic Fiber Link Circuit



(b) Photonic Circular Circuit



- ☐ Two Gaussian variables describing variations
  - ○ I_{off} (offset current) in the laser
  - ○ Length of the fiber waveguide

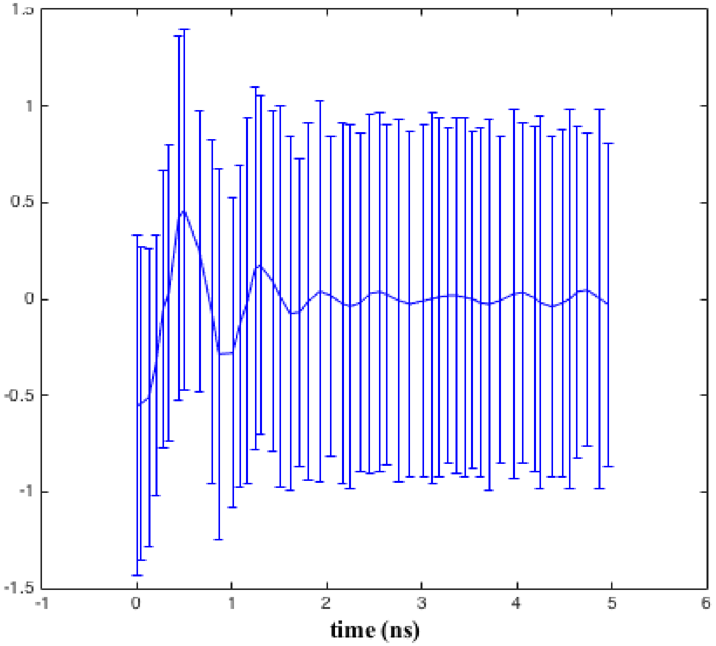
- ☐ Two Gaussian variables describing variations
  - ○ Length of Fiber1
  - ○ Length of Fiber2

- Note: this is not a complete or general purpose simulator; the examples are hard-coded manually

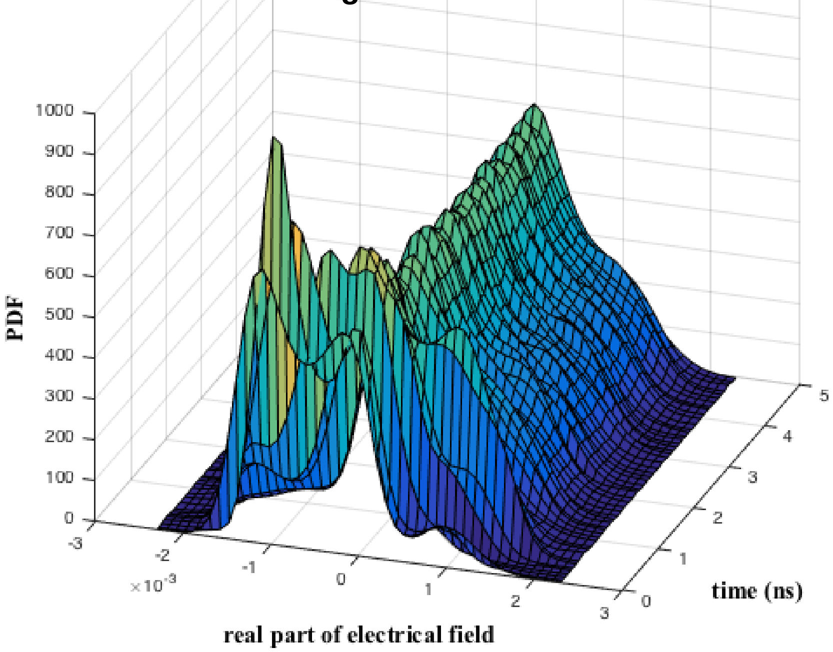
Future Outlook (2): Stochastic Testing Photonic Simulation

- ❑ Stochastic testing simulation result for the Fiber Link Circuit

(a) Mean and s.t.d. of electrical field at the output waveguide



(b) Extracted density function along the time axis



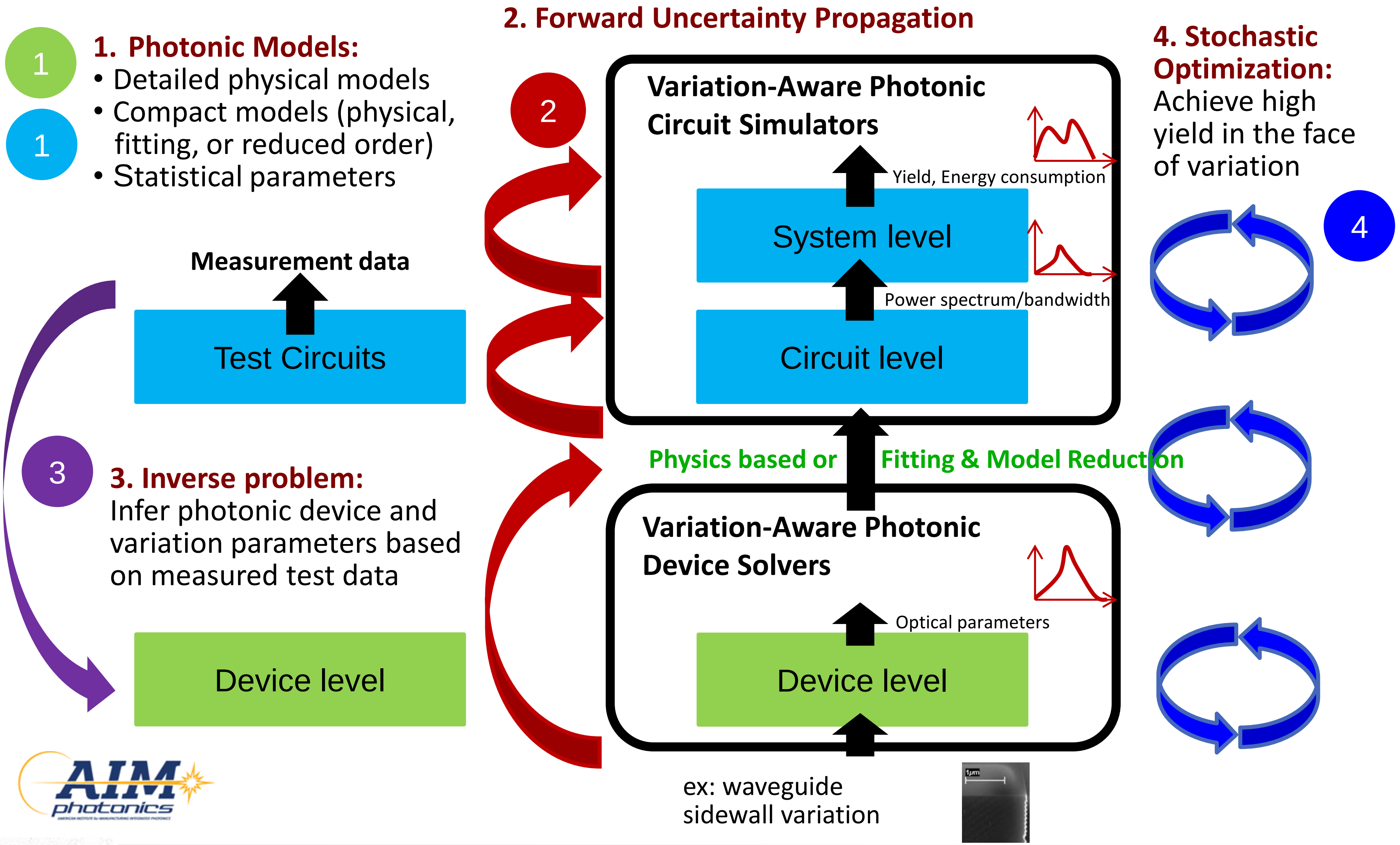
- ❑ Advantages:
  - ○ Requires only one simulation to compute stochastic models (no Monte Carlo!)
  - ○ PDF can be easily obtained from computed stochastic models

Luca Daniel, Zheng Zhang, Lily Weng (MIT) – work in progress under AIM Photonics DFM project

Photonics Design-for-Manufacturability

- Understanding Process Variations in Photonic Processes and Devices
  - Wafer-level geometry, materials variations
  - Chip-scale spatial variations
  - Device-level geometry impacts
- Need: Modeling of Spatial/Layout-Dependent Process Variation
  - Develop process variability models for silicon photonics fabrication
  - Extract models from test structure and fabrication data
- Need: Statistical Compact Models
  - Identify sensitive parameters in photonic compact models
  - Device/component test structures and statistical characterization
  - Generate statistical compact models (from efficient physical models/methods, fitting/reduced order, or data) for subset of sensitive photonic components
- Need: DFM Simulation Techniques and Tools
  - Statistical photonics simulation for prediction of forward propagation of process and component variation to system performance
  - Statistical optimization methods for high yield of photonic systems given variation models

Key Challenges in Photonic DFM Framework



1

1

1. Photonic Models:

- Detailed physical models
- Compact models (physical, fitting, or reduced order)
- Statistical parameters

Measurement data

Test Circuits

3

3. Inverse problem:
Infer photonic device and variation parameters based on measured test data

Device level

2. Forward Uncertainty Propagation

2

Variation-Aware Photonic Circuit Simulators

Yield, Energy consumption

System level

Power spectrum/bandwidth

Circuit level

Physics based or **Fitting & Model Reduction**

Variation-Aware Photonic Device Solvers

Optical parameters

Device level

ex: waveguide sidewall variation

4. Stochastic Optimization:
Achieve high yield in the face of variation

4

Acknowledgments

- Current photonics design-for-manufacturability project funded under AIM Photonics: MIT/UCSB team

- Contributions of many previous students, colleagues, and collaborators