DesignCon® 2019
WHERE THE CHIP MEETS THE BOARD

Effect of Power Plane Inductance on Power Delivery Networks

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Effect of Power Plane Inductance on Power Delivery Networks (PDNs)

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Speakers

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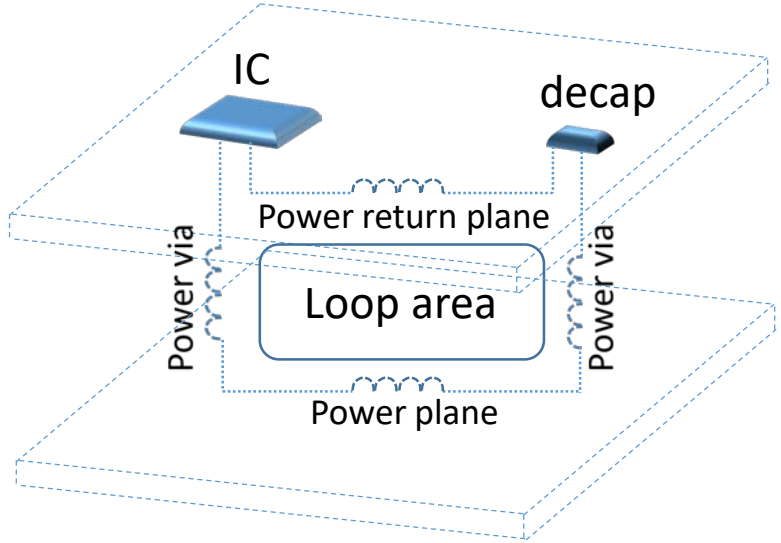
Ethan Koether is a Senior Hardware Engineer at Oracle Corporation. He is currently focusing on system power-distribution network design, measurement, and analysis. He received his master's degree in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology.

Power Plane Inductance

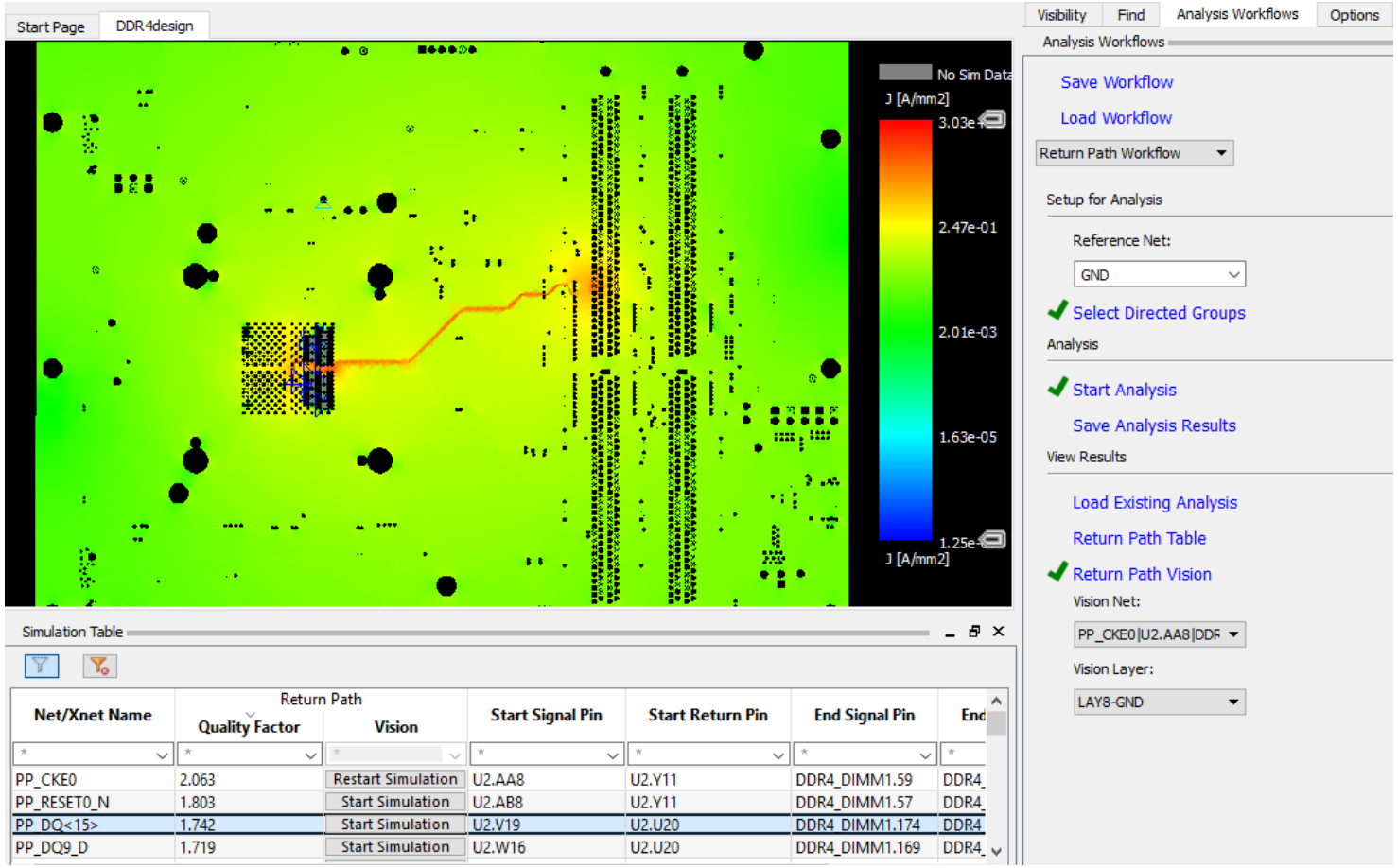
- Power plane inductance is important for PDN design
  - Impacts frequency response
  - Affects ground bounce noise
  - Affects power network decoupling
  - Can be difficult to intuitively estimate
- Power plane loop inductance is necessary for PDN design optimization
- Efficient simulation of power plane loop inductance is valuable for PDN design



Re-drawn based on: Kim, J, Fan, J, Drewniak, J.L., "Inductance Calculations for Plane-Pair Area Fills with Vias … ", *IEEE Trans Microwave Theory*. 2011

Net Inductance

- Allegro workflow for quickly simulating net loop inductance at 1MHz
- Visualize return current on the Allegro canvas

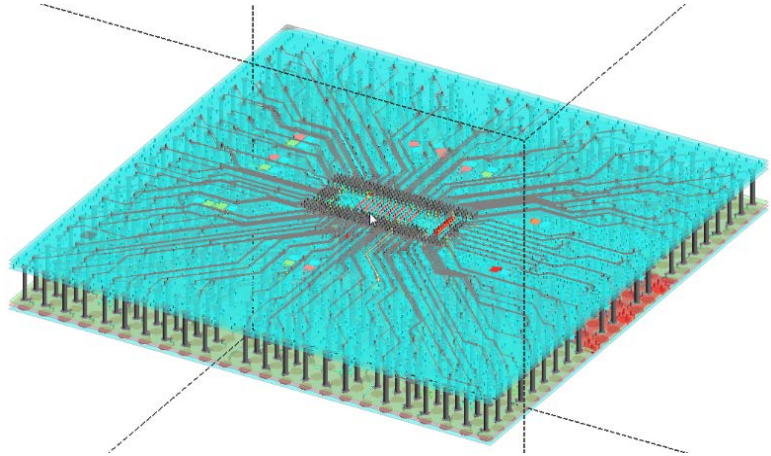


Outline

- Hybrid simulator correlation
  - Impedance of ball grid array
  - Power plane loop inductance on a small IC test board
  - Power plane loop inductance on a large motherboard
- Impact of design variations on power plane loop inductance
- Loop inductance and coupling
- Conclusion

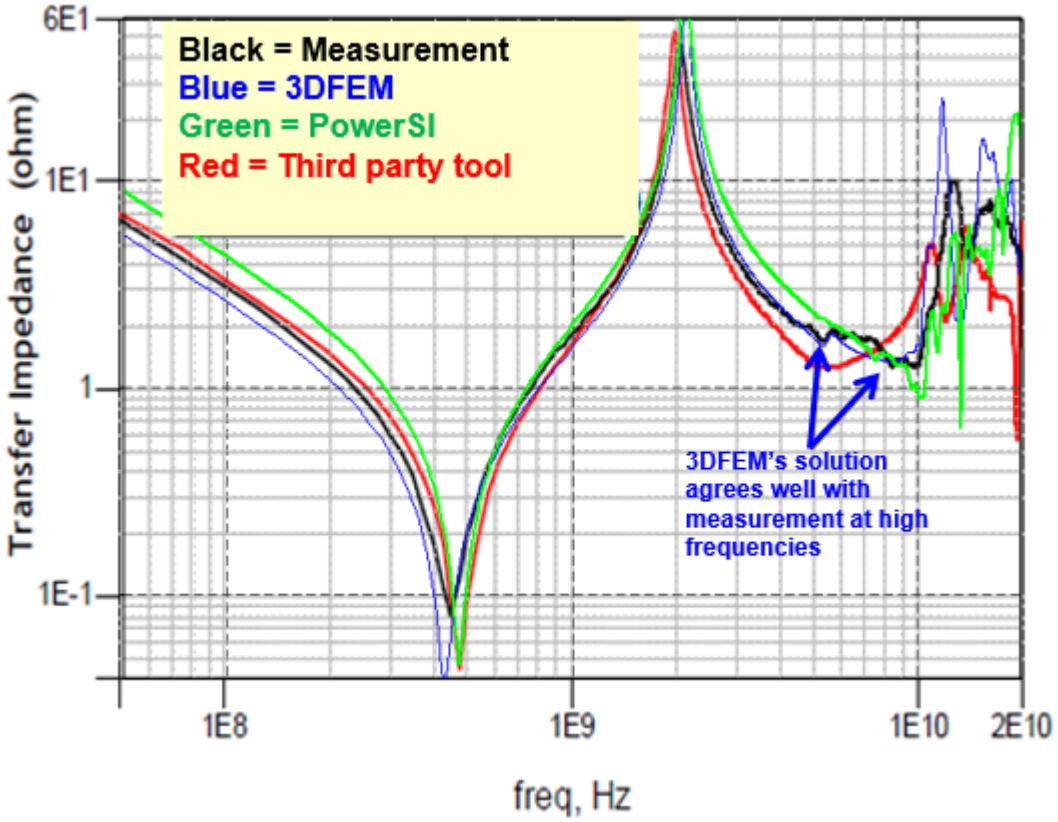
Hybrid Simulator – Sigrity PowerSI Technology

- Uses numerical methods and approximations to solve electromagnetic fields and extract S-parameters
- Impedance parameters are then extracted from the S-parameters and used to extract inductance quantities for several structures
- Measurement to simulation correlation of ball grid array
  - 2” x 2” organic
  - Two layers with 800µm core
  - Unpopulated



Hybrid Simulator – Sigrity PowerSI Technology

- Measurement to simulation correlation of ball grid array package is obtained
- 2” x 2” package size, unpopulated, 800µm core
- Excellent correlation between measurement and simulation of transfer impedance between Cadence® Sigrity™ PowerSI® 3D solver and a third-party tool is shown in the plots
- The good correlation is exploited to extract circuit parameters for more complex structures



Correlation of Loop Inductance – Case 1: Small IC Test Board

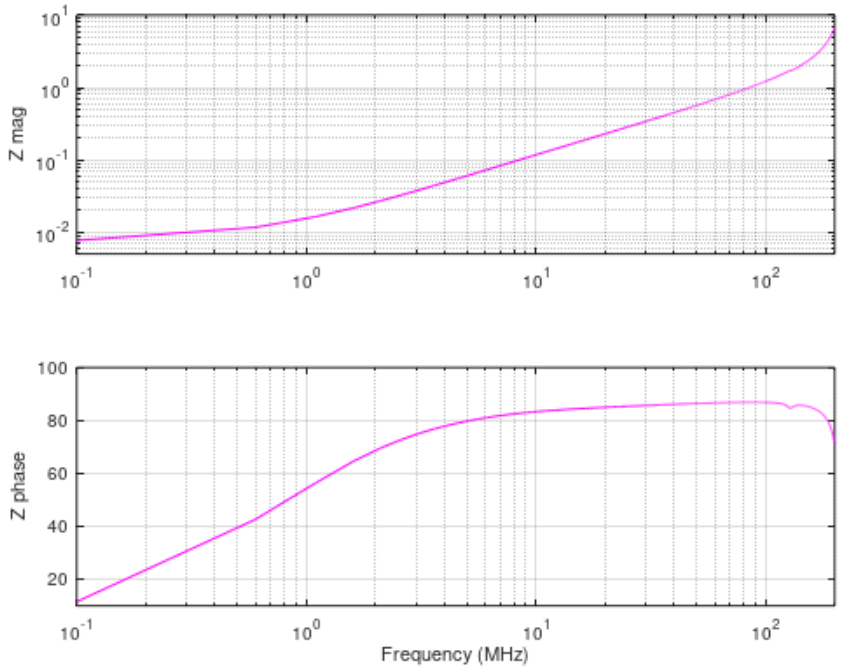
- Power plane loop inductance measurements on a small IC test board
  - Keysight E5061B VNA from 100kHz to 200MHz
  - Used S_{21} measurement to avoid measurement error with a one-port setup*
  - Power plane being measured/simulated on Layer 5

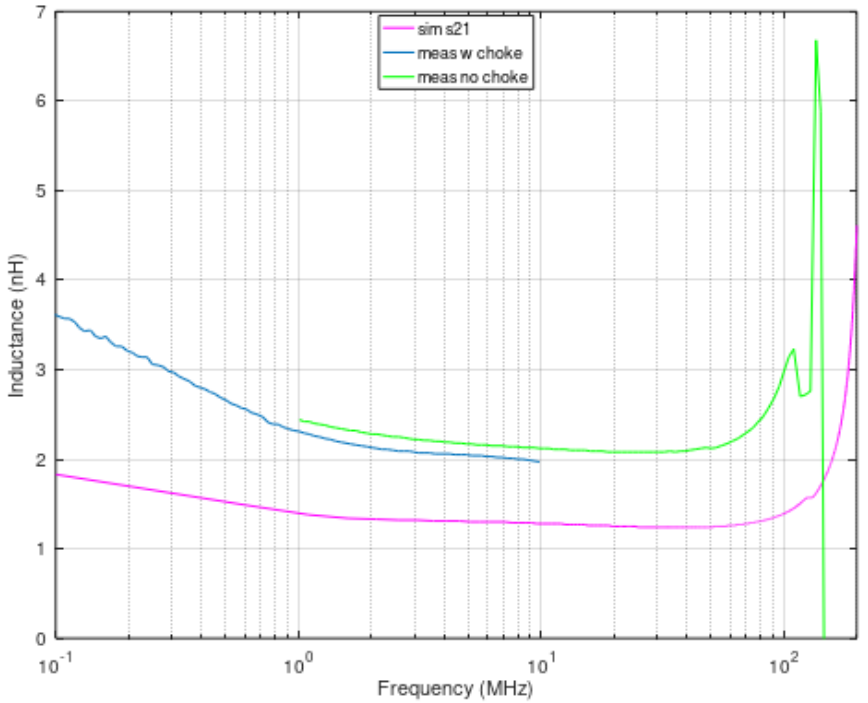
Layer	Material	Thickness (mils)
TOP	Copper	2.1
	FR4	3.7
LAY2 – GND Plane	Copper	1.2
	FR4	6
LAY3 – SIG1	Copper	1.2
	FR4	5.8
LAY4 – GND Plane	Copper	1.2
	FR4	4
LAY5 – PWR1 Plane	Copper	1.2
	FR4	15.4
LAY6 – PWR2 Plane	Copper	1.2
	FR4	4
LAY7 – GND Plane	Copper	1.2
	FR4	5.8
LAY8 – SIG2	Copper	1.2
	FR4	6
LAY9 – GND Plane	Copper	1.2
	FR4	3.7
BOTTOM	Copper	2.1

* Novak, I., “Probes and Setup for Measuring Power-Plane Impedances with Vector-Network Analyzer”, DesignCon 1999

Correlation of Loop Inductance – Case 1: Small IC Test Board

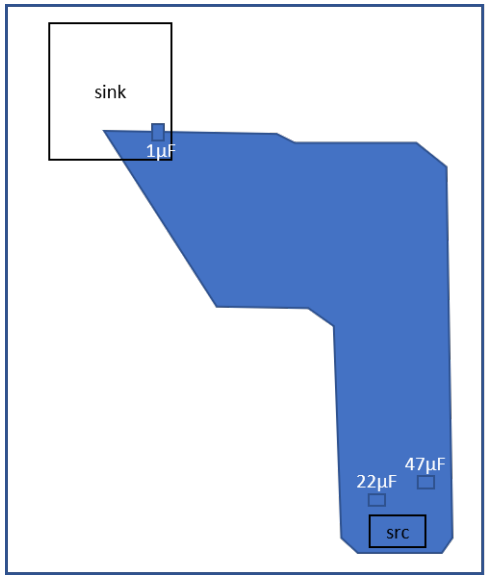
- Power plane loop inductance measurements on a small IC test board
  - Keysight E5061B VNA from 100kHz to 200MHz
  - Common-mode toroid transformer used as a choke to suppress cable-braid loop error at low frequencies
  - Simulation done using the same port configuration
  - Measurements taken on bare board with short added at source

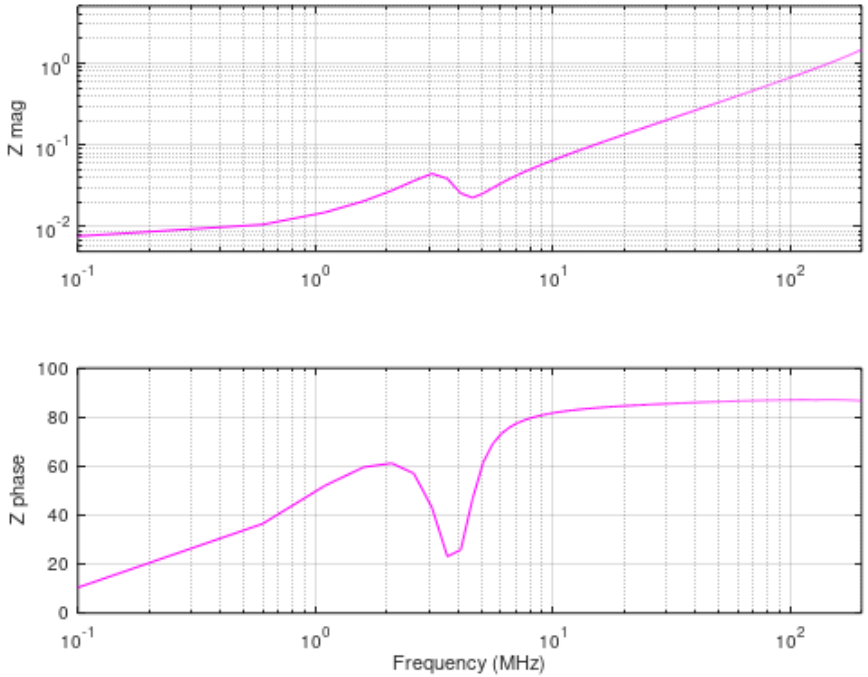


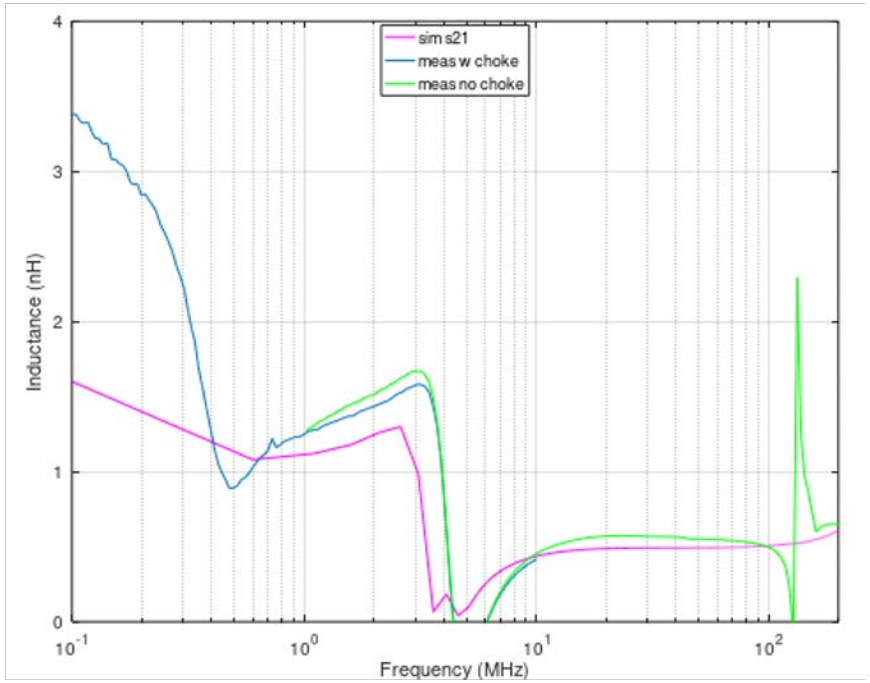


Correlation of Loop Inductance – Case 1: Small IC Test Board

- Power plane loop inductance measurements on a small IC test board
  - Added capacitors to power plane

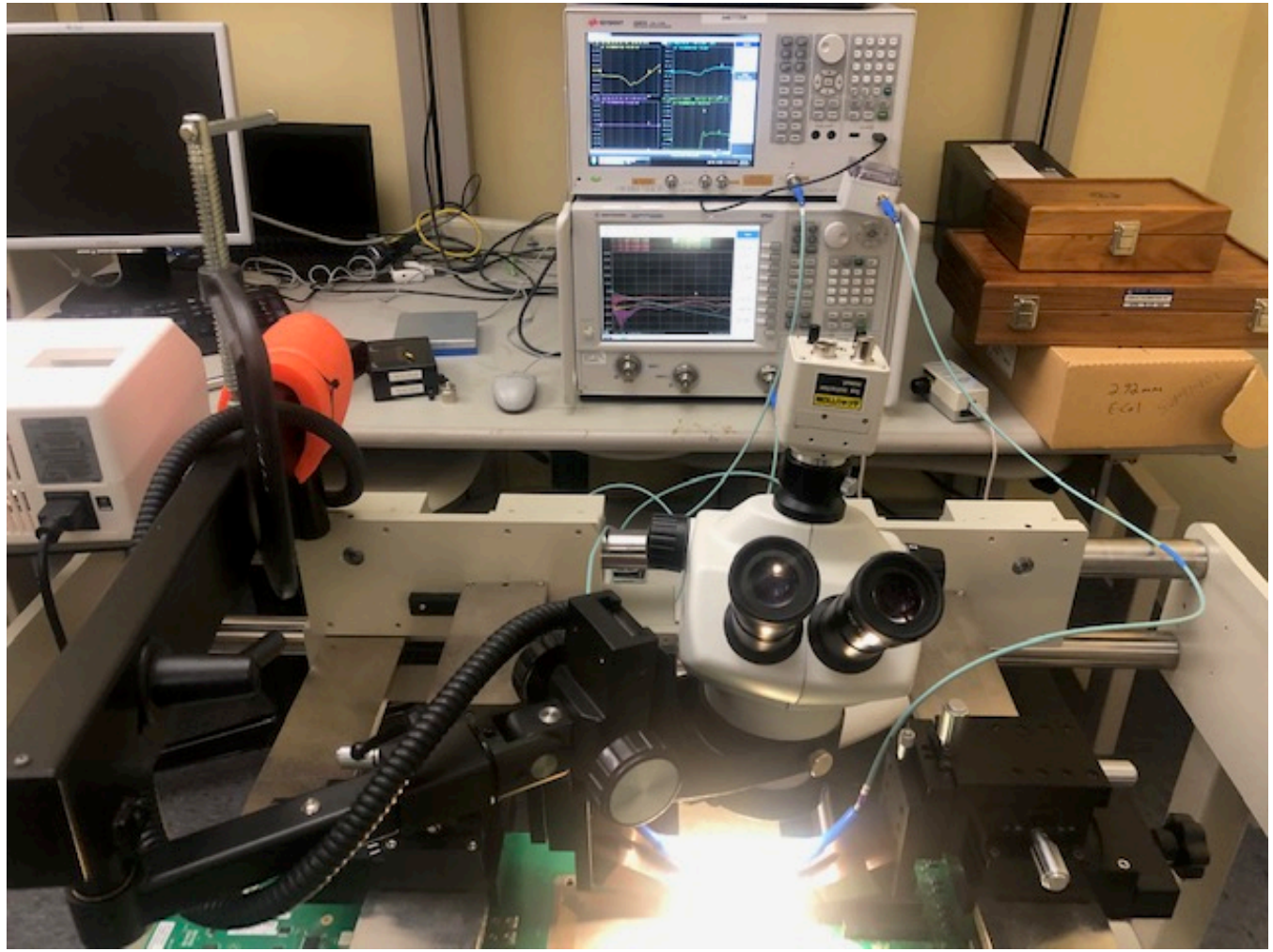






Correlation of Loop Inductance – Case 2: Large Motherboard

- Power plane loop inductance measurements on a large motherboard
  - 24 layers, two processors, and four PCIe® ports per processor
  - First version had noise coupling on PCIe lane due to nearby DC-DC converter*

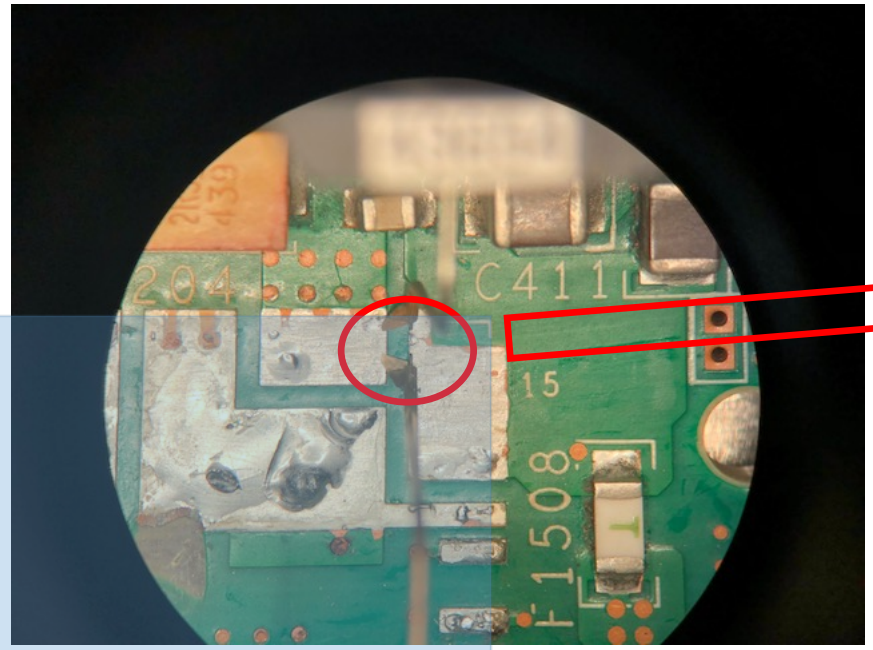


* Kocubinski, L, Blando, G, and Novak, I., “Mid-Frequency Noise Coupling between DC-DC Converters and High-Speed Signals”, DesignCon 2016

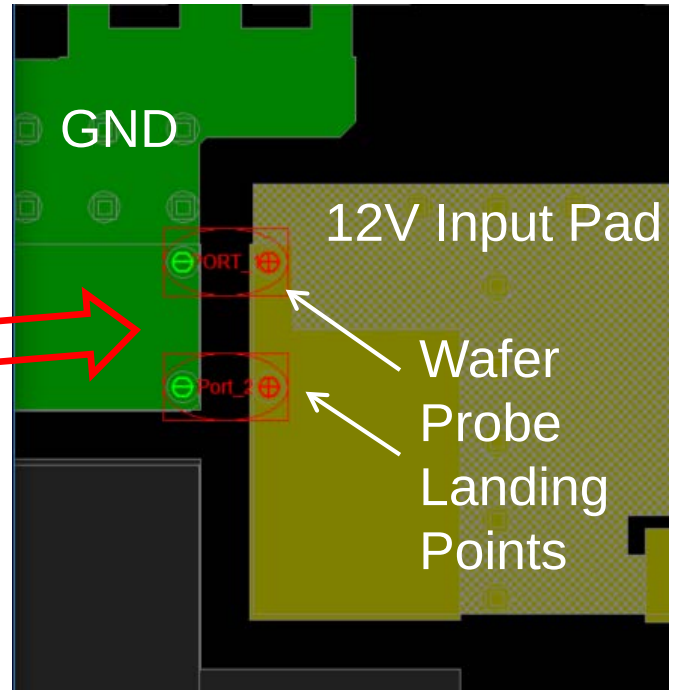
Correlation of Loop Inductance – Case 2: Large Motherboard

- Power plane loop inductance measurements on a large motherboard
  - Probe configuration for power plane measurement

Photo of Wafer Probe Landing

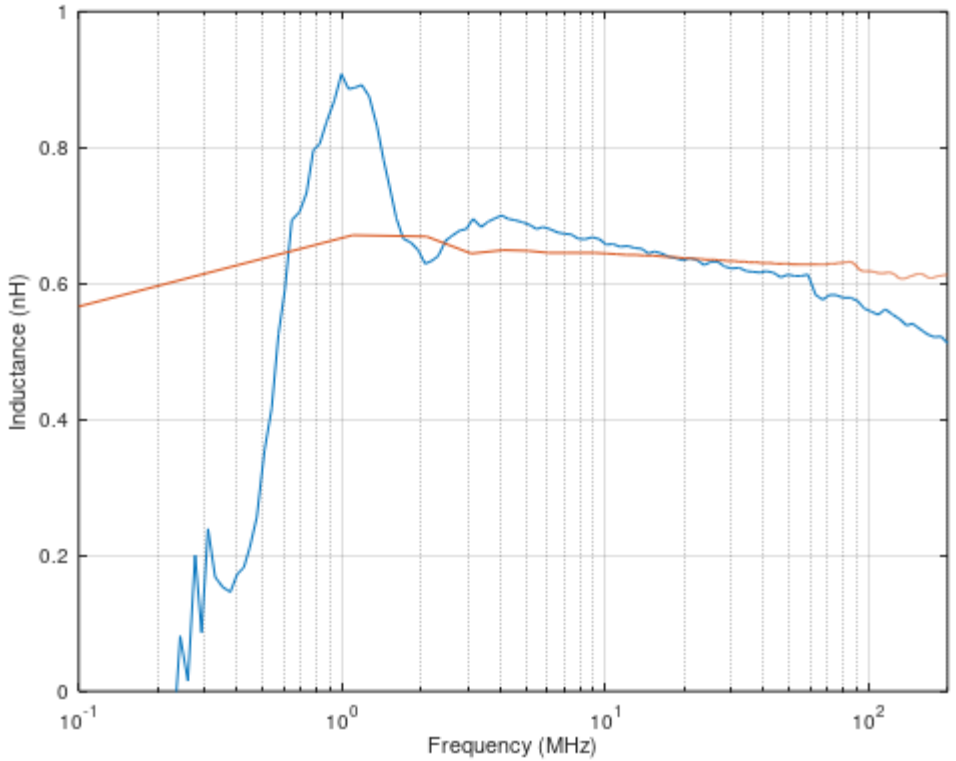


Zoomed Layout Detail

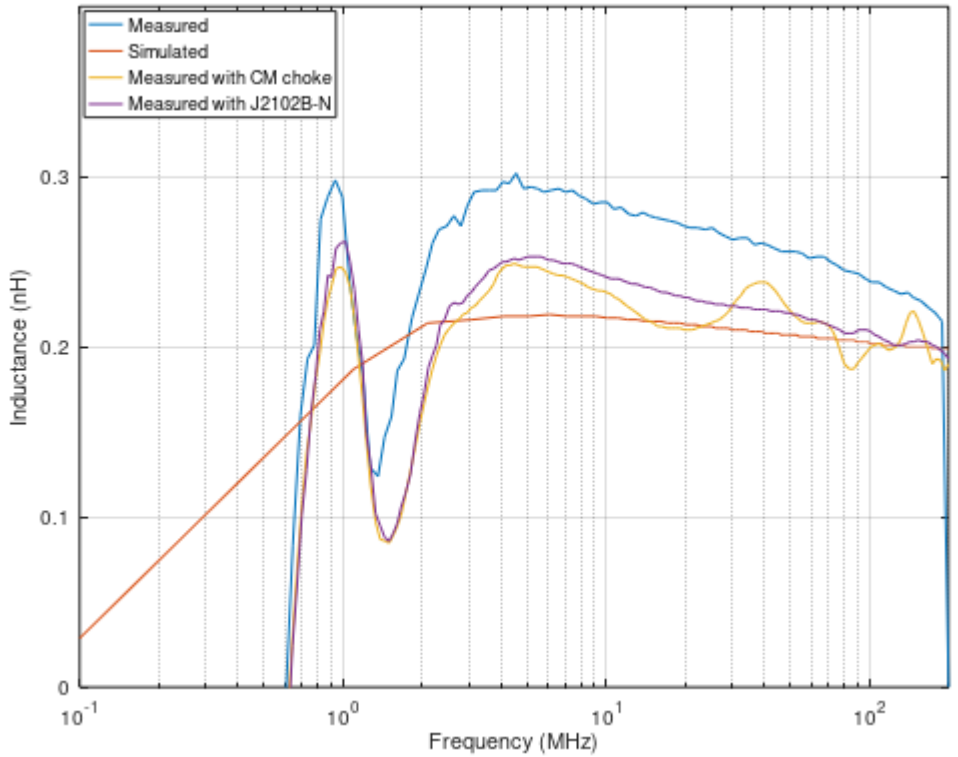


Correlation of Loop Inductance – Case 2: Large Motherboard

Power plane inductance on first version of the motherboard, Blue = measured, orange = sim

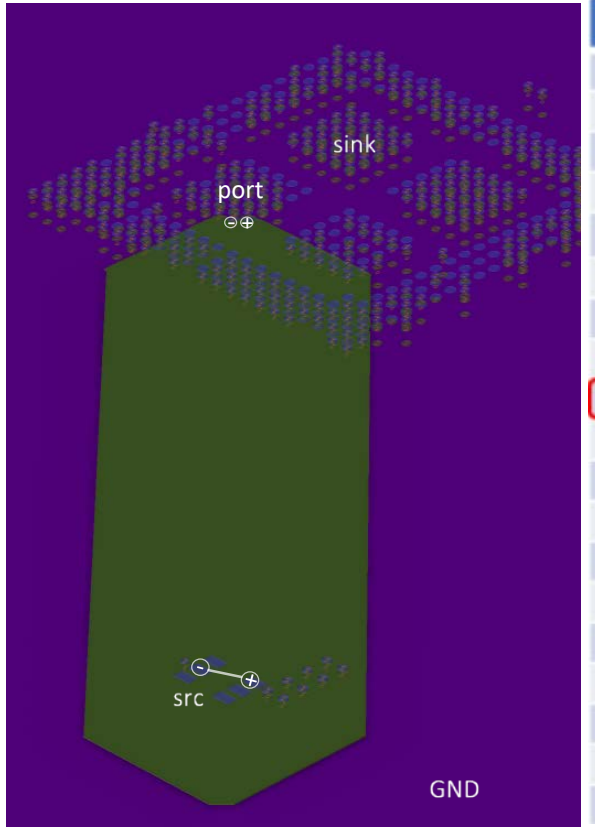


Power plane inductance on final version of the motherboard, Blue, yellow, and purple = measured, orange = sim



Impact of Design Changes on Power Plane Loop Inductance, Case 1 Variant

- Design variations:
  - Plane width
  - Anti-pads
  - Power vias
  - Ground vias
  - Decoupling capacitors
  - Power to ground short
  - Power to ground inductance
- Inductance values reported at 2MHz as seen by the sink with the source pins shorted



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TOP	Copper	2.1
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LAY2 – GND Plane	Copper	1.2
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	FR4	15.4
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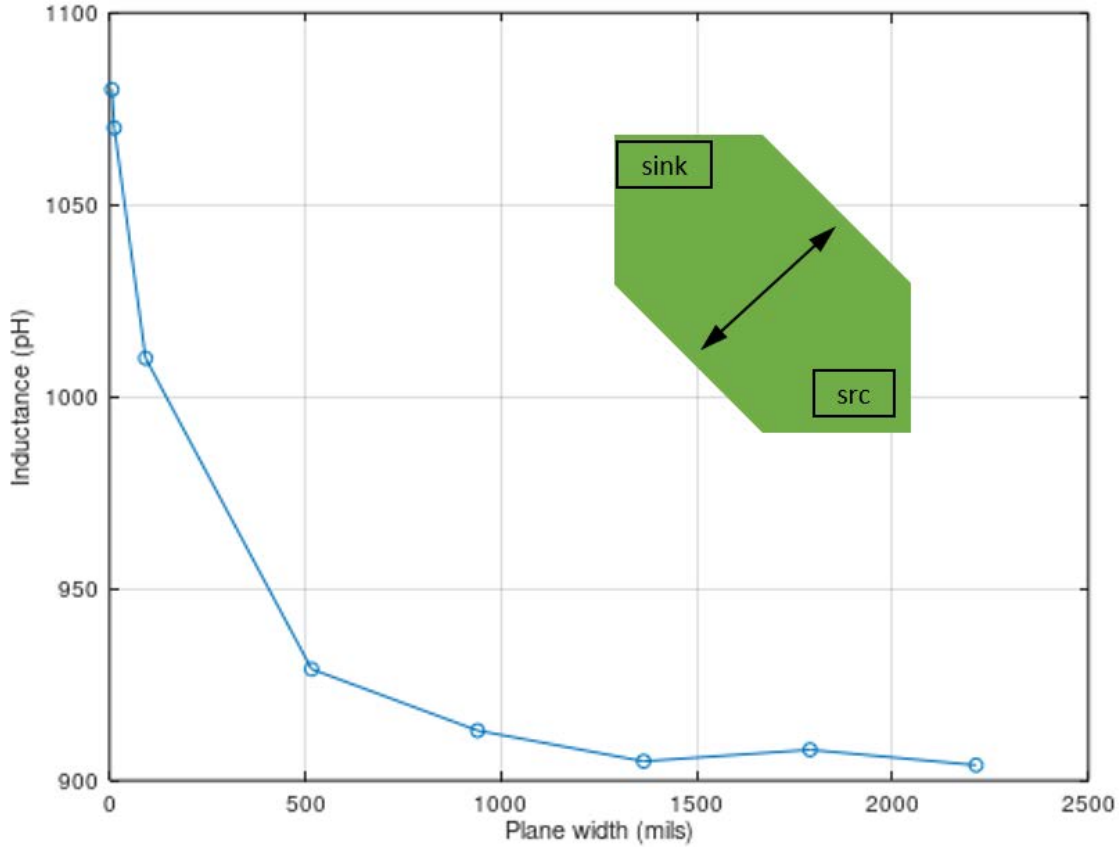
	FR4	4
LAY7 – GND Plane	Copper	1.2
	FR4	5.8
LAY8 – SIG2	Copper	1.2
	FR4	6
LAY9 – GND Plane	Copper	1.2
	FR4	3.7
BOTTOM	Copper	2.1

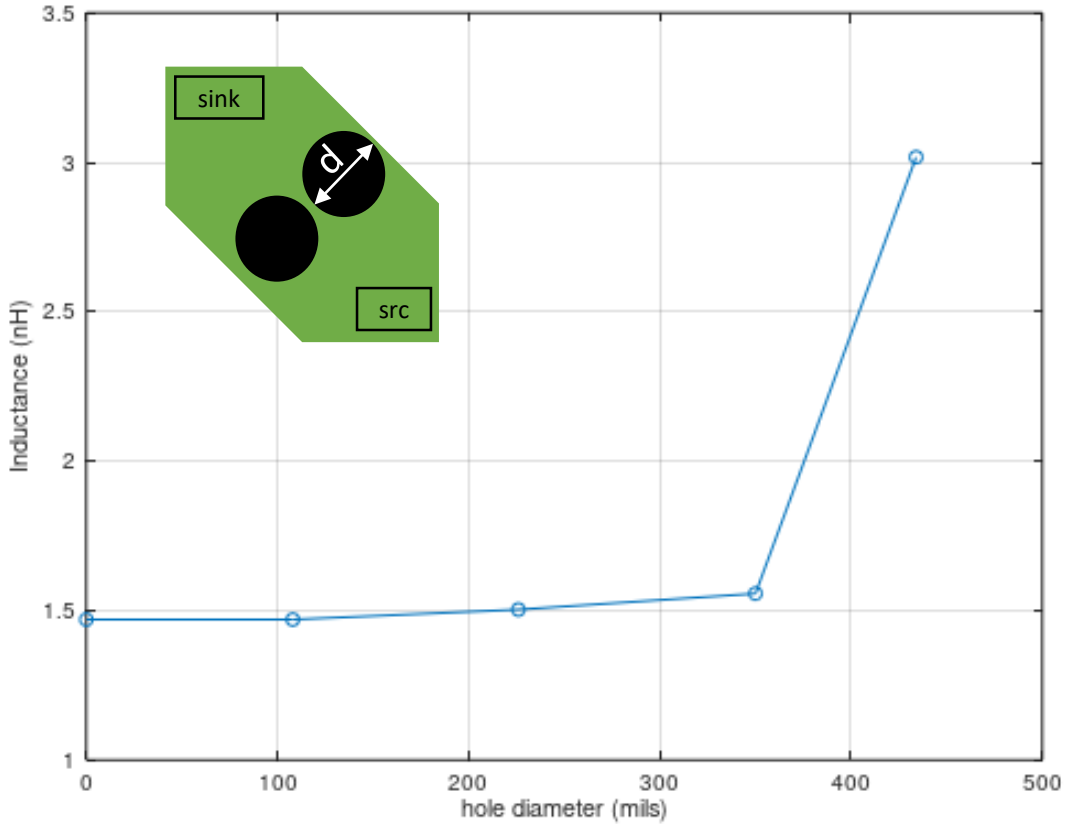
Impact of Plane Width on Power Plane Loop Inductance, Case 1 Variant

- Increasing plane width decreases loop inductance seen by sink
- Biggest change seen from 100mils to 500mils



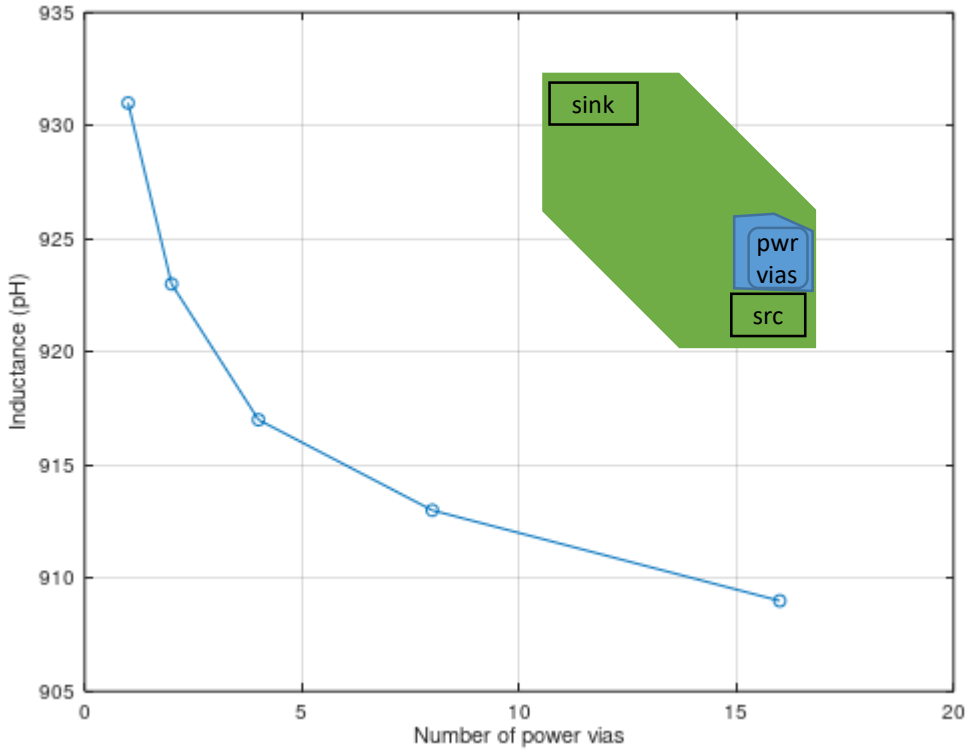
Impact of Design Changes on Power Plane Loop Inductance, Case 1 Variant

- Anti-pad diameter must be very large to have a significant impact on loop inductance
- Also found that number of anti-pads and location didn't have a big impact on inductance
- Plane width 500mils, distance from source to sink is 1500mils



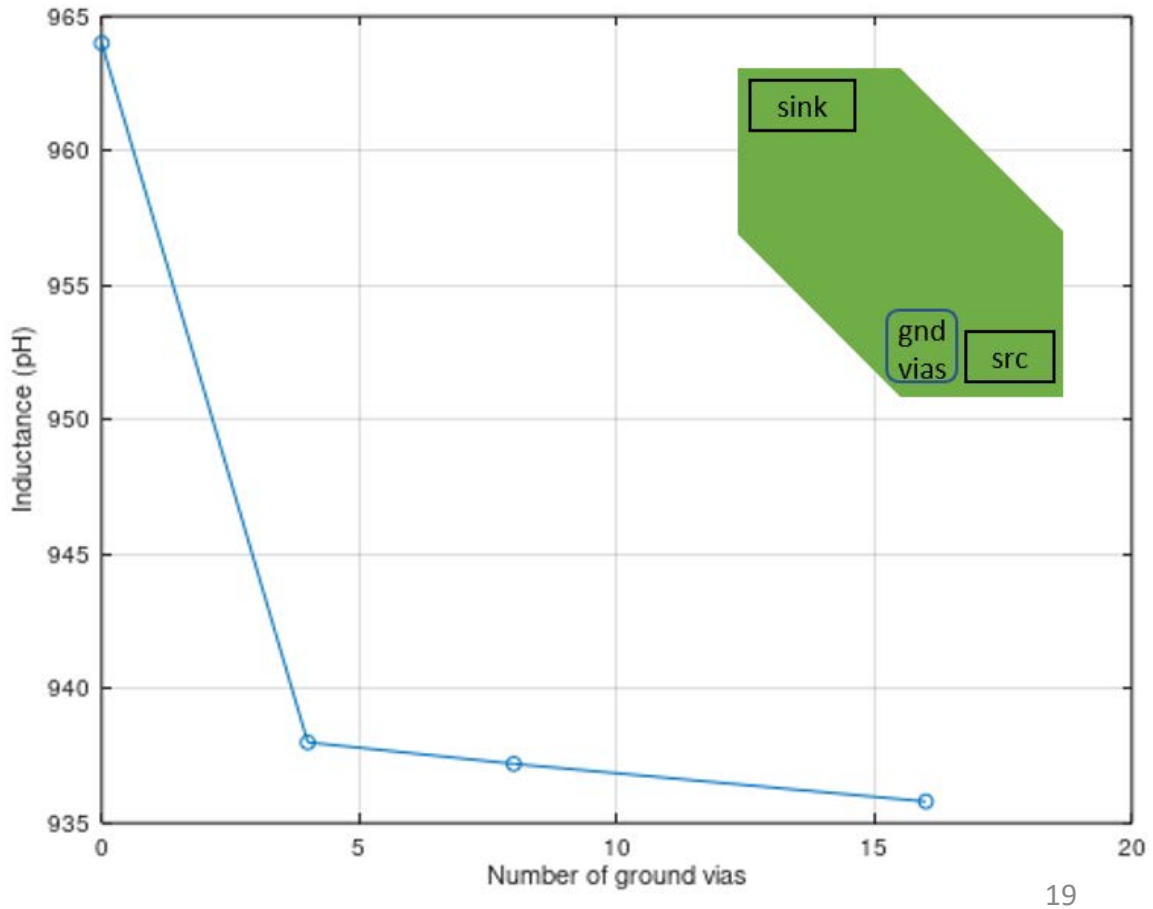
Impact of Design Changes on Power Plane Loop Inductance, Case 1 Variant

- Increasing number of power vias near the source decrease loop inductance seen by the sink
- Power vias connect to a power plane shape on the surface



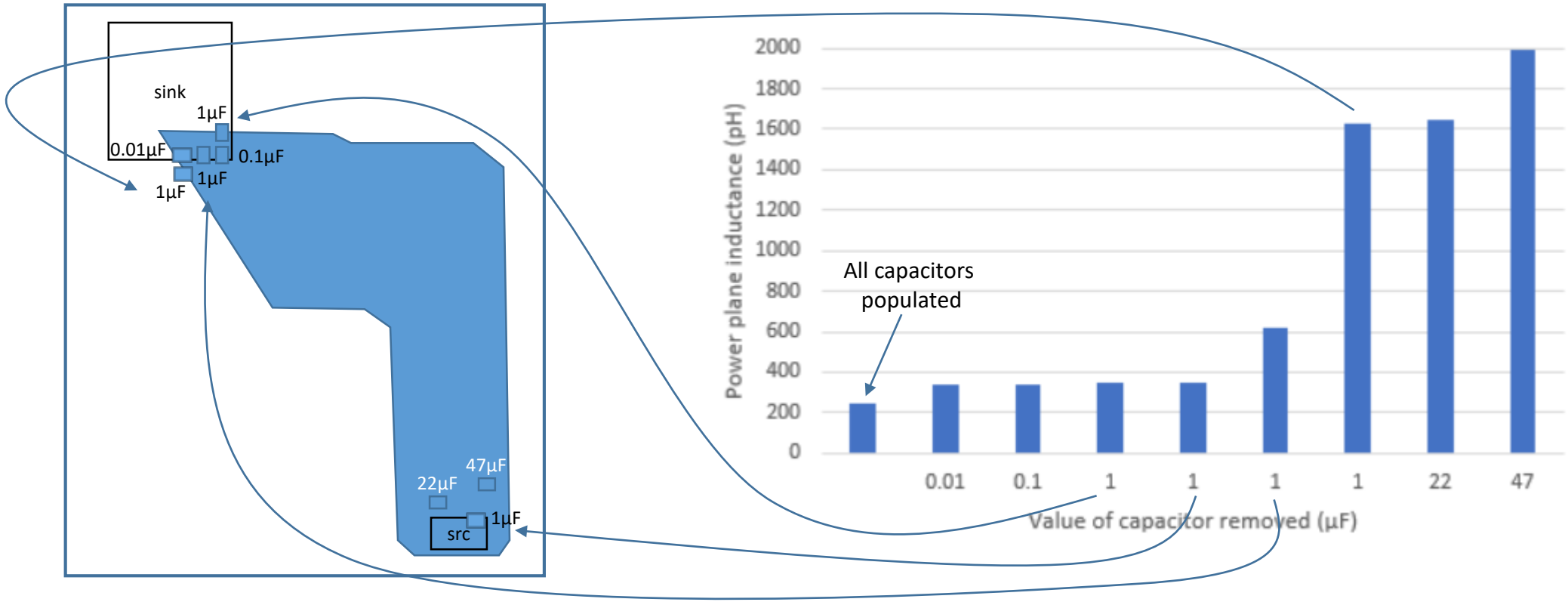
Impact of Design Changes on Power Plane Loop Inductance, Case 1 Variant

- Similar findings to impact of power vias
- More vias near source decrease loop inductance seen by sink



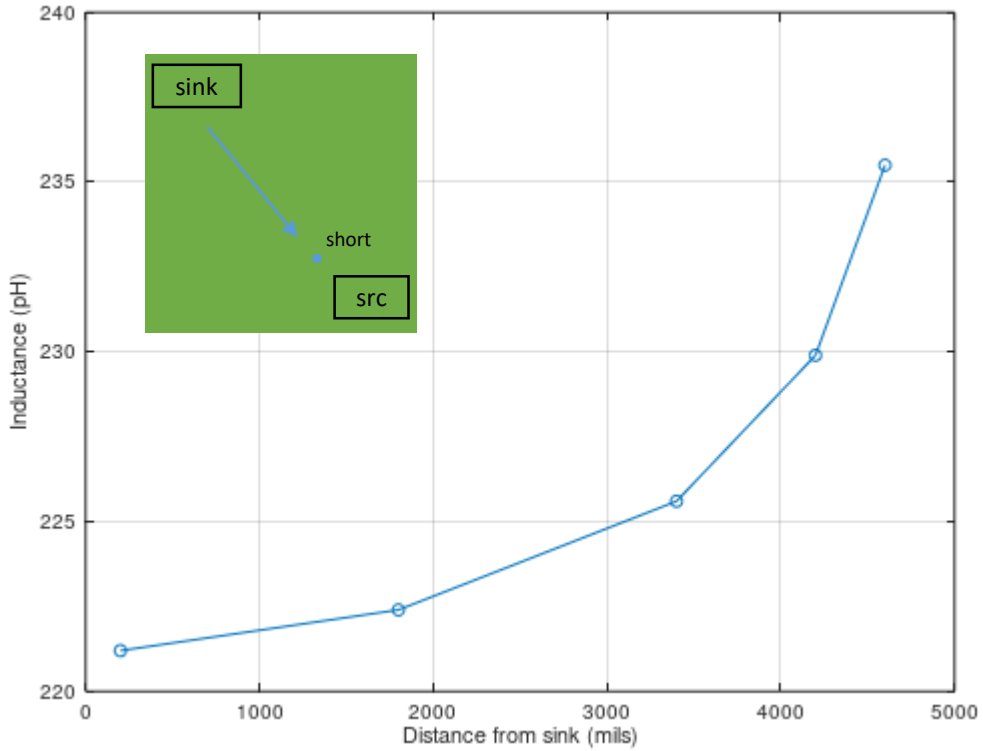
Impact of Number of Decoupling Capacitors on Power Plane Inductance

- Removing each decoupling capacitor increased power plane loop inductance
- Biggest impact when removed last decoupling capacitor between plane and ground



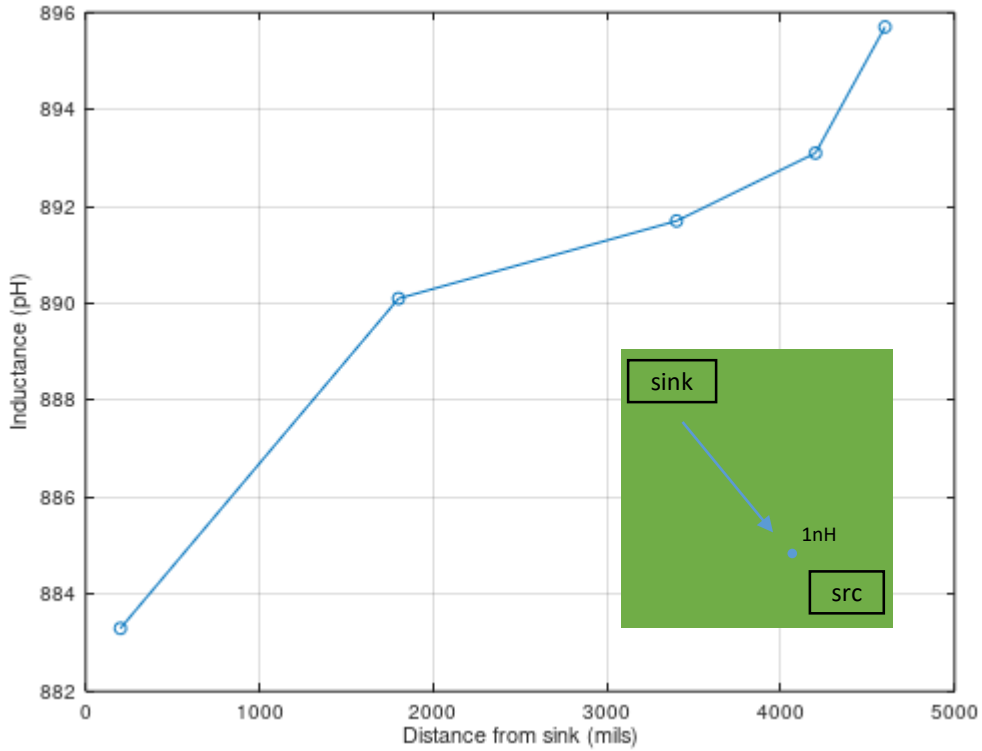
Impact of Design Changes on Power Plane Loop Inductance, Case 1 Variant

- Power to ground via short moved from near source to near sink
- Inductance increases as short gets further from sink



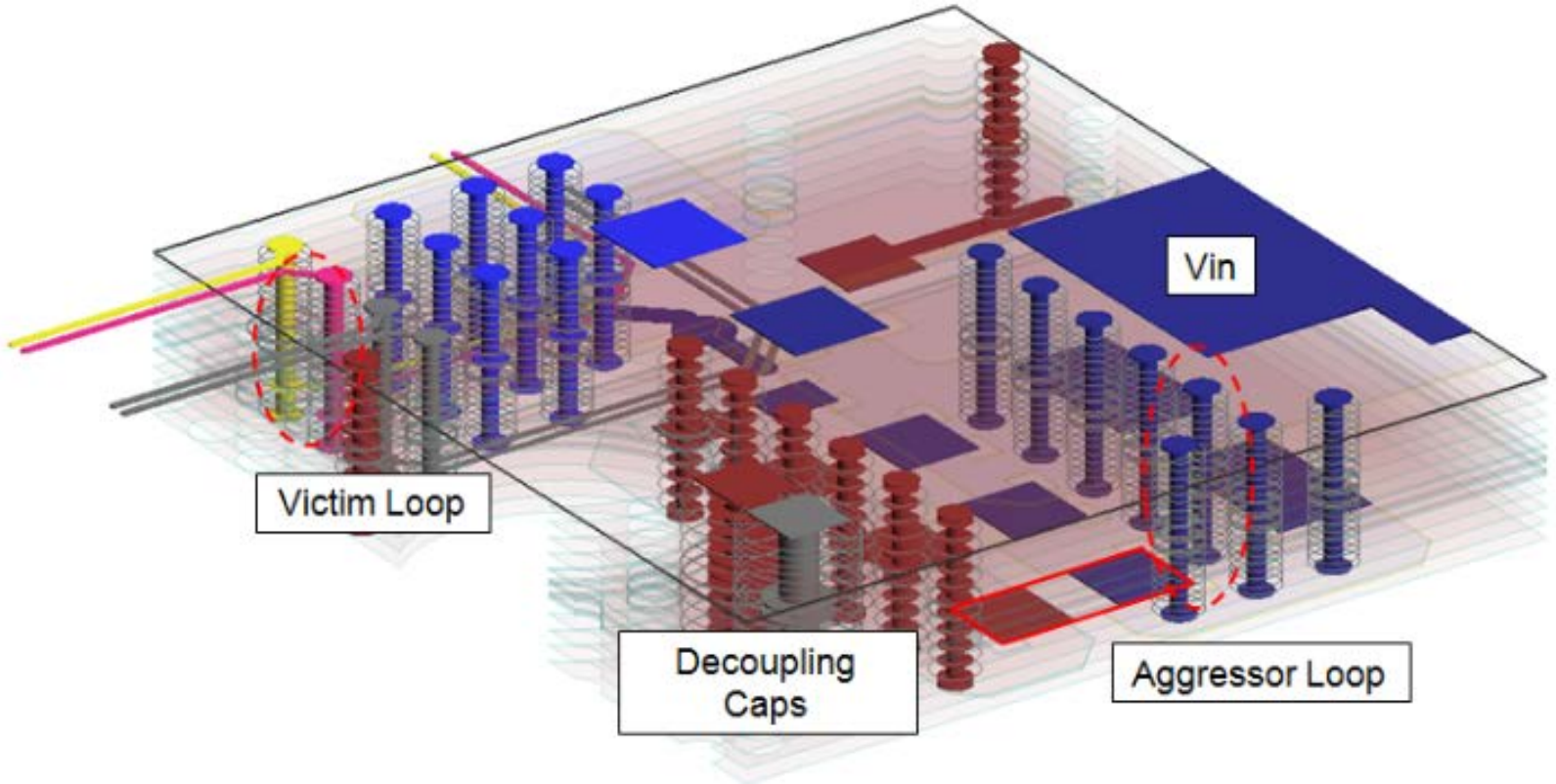
Impact of Design Changes on Power Plane Loop Inductance, Case 1 Variant

- Via short now replaced with a ground via connected to power plane by 1nH inductor to mimic decoupling capacitor
- As before, loop inductance increased as inductor got further from sink



Loop Inductance and Coupling, Case 2

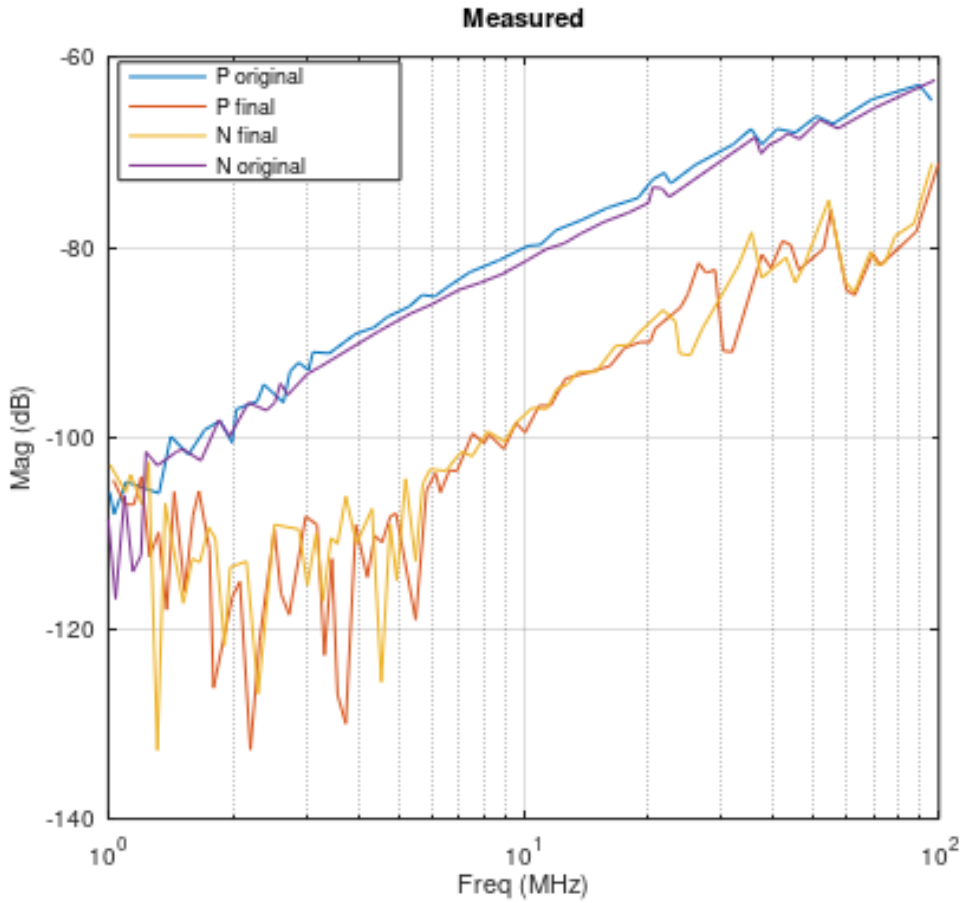
- Mid-frequency noise from a DC-DC converter to a PCIe® lane required two re-spins to resolve
- Final version of board had more ground vias near victim and moved decoupling capacitors to top of board

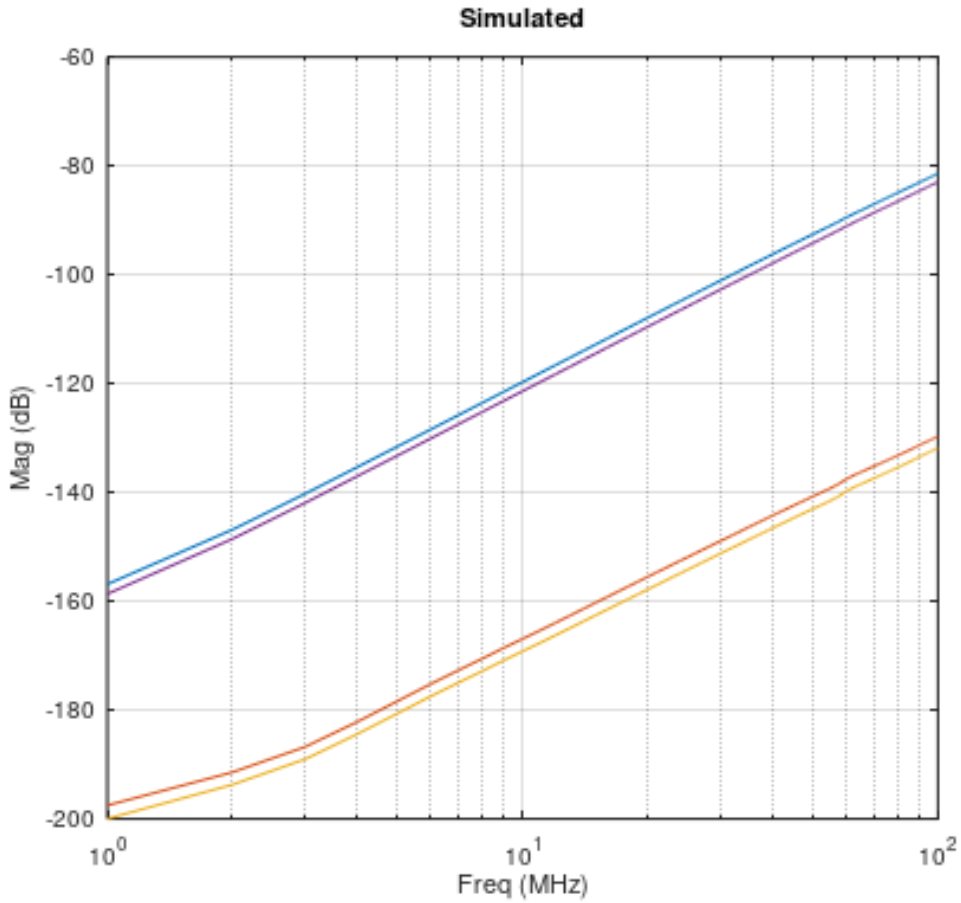


* Kocubinski, L, Blando, G, and Novak, I., “Mid-Frequency Noise Coupling between DC-DC Converters and High-Speed Signals”, DesignCon 2016

Loop Inductance and Coupling, Case 2

- Change in coupling (S_{21}) due to board design changes well captured by simulation





Conclusions

- Power plane loop inductance is important for PDN frequency response and for understanding a design's ground bounce noise and noise coupling
- Our hybrid simulation approach provides an efficient method of estimating power plane loop inductance and coupling due to inductive effects
- Impact of design parameter changes on plane loop inductance
  - Plane width: ↓ width → ↑ L
  - Anti-pads: ↑ diameter → ↑ L
  - Power vias: ↑ vias → ↓ L
  - Ground vias: ↑ vias → ↓ L
  - Decoupling capacitors: ↑ decaps → ↓ L
  - Power to ground short: ↑ loop → ↑ L
  - Power to ground inductance: ↑ loop → ↑ L

Acknowledgements

- **Bradley Brim, Cadence Design Systems**
- **Gustavo Blando, Samtec**

Questions?