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Developing secure IoT systems as fast as possible

Cadence and Arm Seminar 2018

Petach Tikvah, Israel

- Phil Burr, Director, Embedded Portfolio, Arm
- Bernd Reinkemeier, Senior Technical Executive, Cadence

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What are today's embedded and IoT challenges?

- Extreme low-power
- Integration complexity
  - Many elements
  - Logic, memory, flash, mixed signal, RF, power, sensors…
- Long life, in remote location
- Security
- Very low cost

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Challenges vary across types of devices

Constrained

- Ultra-low-cost, simple sensors
- Often battery powered
- Connecting to gateway or cloud

Mainstream

- Balancing performance and cost
- Moderate data or audio capabilities
- High power efficiency

Rich IoT nodes & gateways

- High levels of data processing at edge
- Autonomous decision making or machine learning
- Providing gateway to cloud

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Security is a common challenge across all devices

Constrained

Mainstream

Rich IoT nodes & gateways

- Ultra
- Oft
- Conn

sing at edge
ing or ML
dd

Security – a key requirement for all

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Arm's Platform Security Architecture (PSA)

Consistently design in the right level of security into low-cost IoT devices

Analyze

Threat models & security analyses

Architect

Hardware & firmware architecture specifications

01001

Implement

Firmware source code

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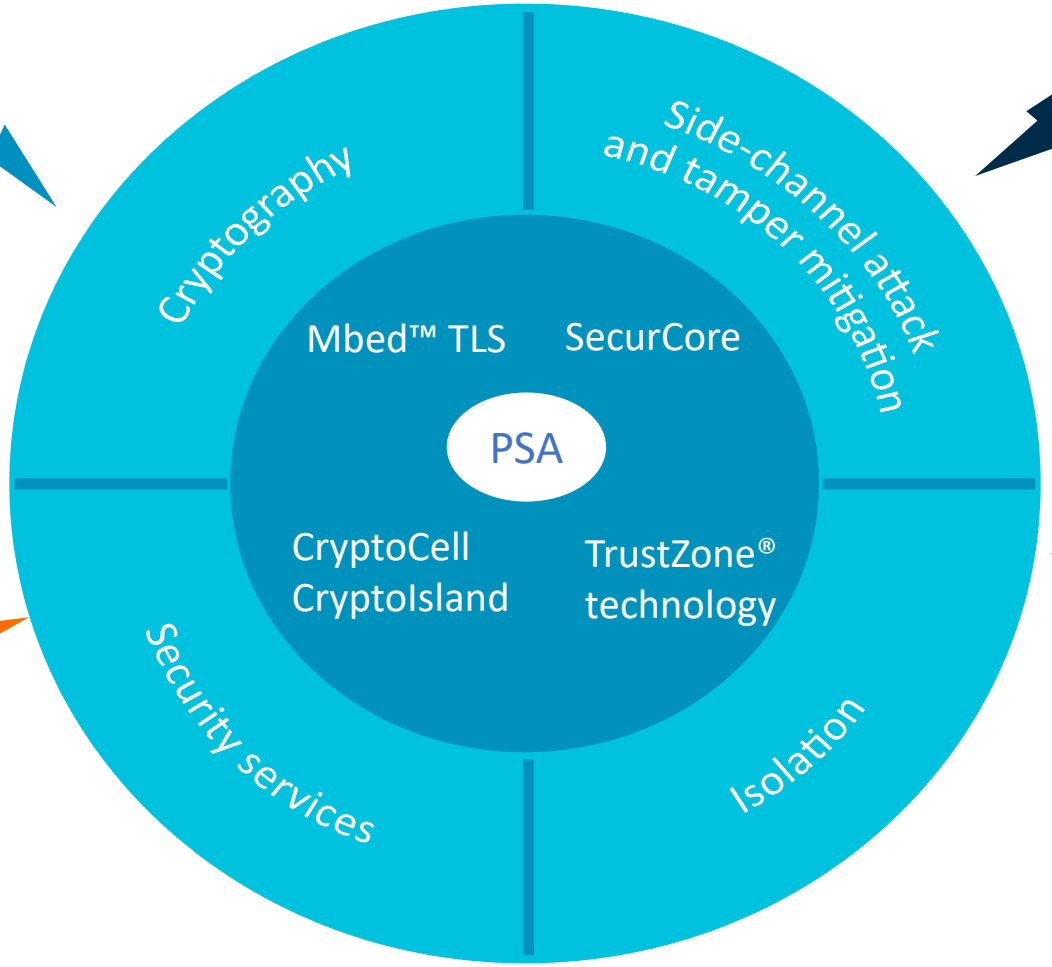
What are we protecting against? Threat modelling

Communications

- Man-in-the-middle
- Weak RNG
- Code vulnerabilities

Physical

- Non-invasive (e.g. clock, power glitch or SCA)
- Invasive: package removal (e.g. microprobe station FIB)



Lifecycle

- Code downgrade
- Change of ownership or environment
- Unauthorized overproduction

Software

- ROP (e.g., buffer overflows)
- Interrupts
- Malware

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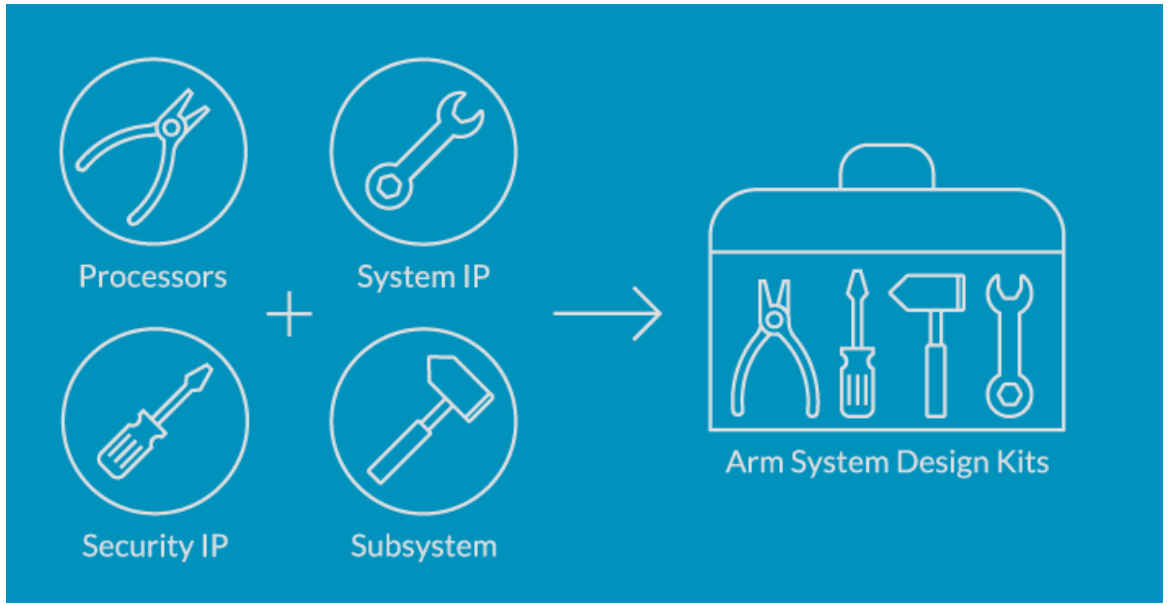
Arm SoC solutions: A complete toolbox for SoC designers

- Standardized interfaces and architecture, common software development
- Pre-verified and pre-integrated foundation
- Extendable for differentiation and diversity of applications
- Bring your secure SoC to market fast, with lower risk



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There are subsystems for each class of device

Constrained

SSE-050

Mainstream

SSE-200

Rich IoT nodes & gateways

SDK-700

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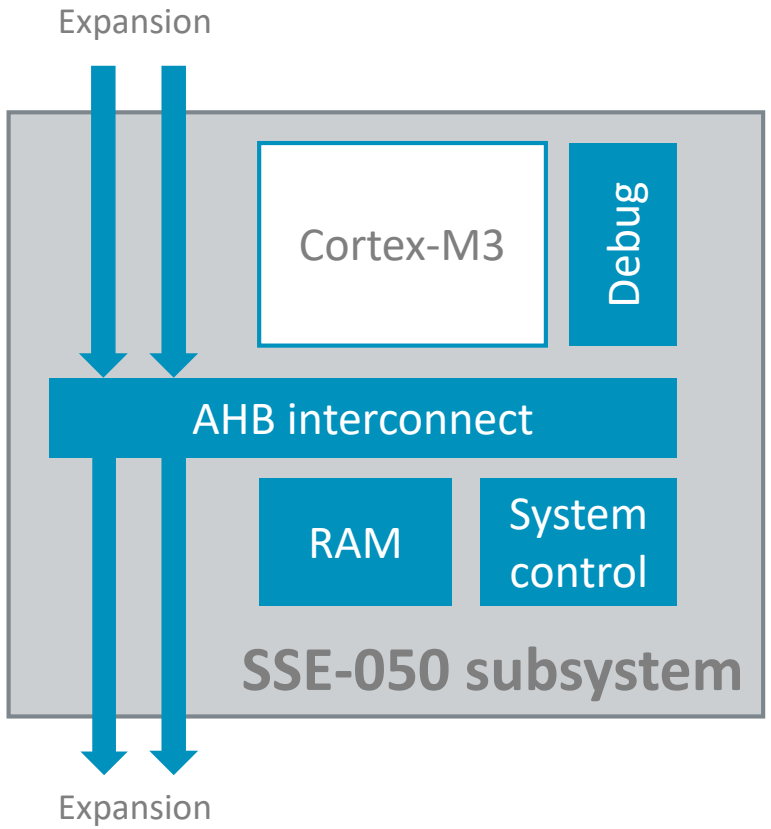
SSE-050 subsystem (part of SDK-101 / SDK-200)

A fast way to start in IoT

Compact
- Based on Cortex-M3

Good starting point

Software support
- Mbed OS
- Other RTOS



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SSE-200 subsystem (part of SDK-200)

A reference system to build secure systems with TrustZone technology

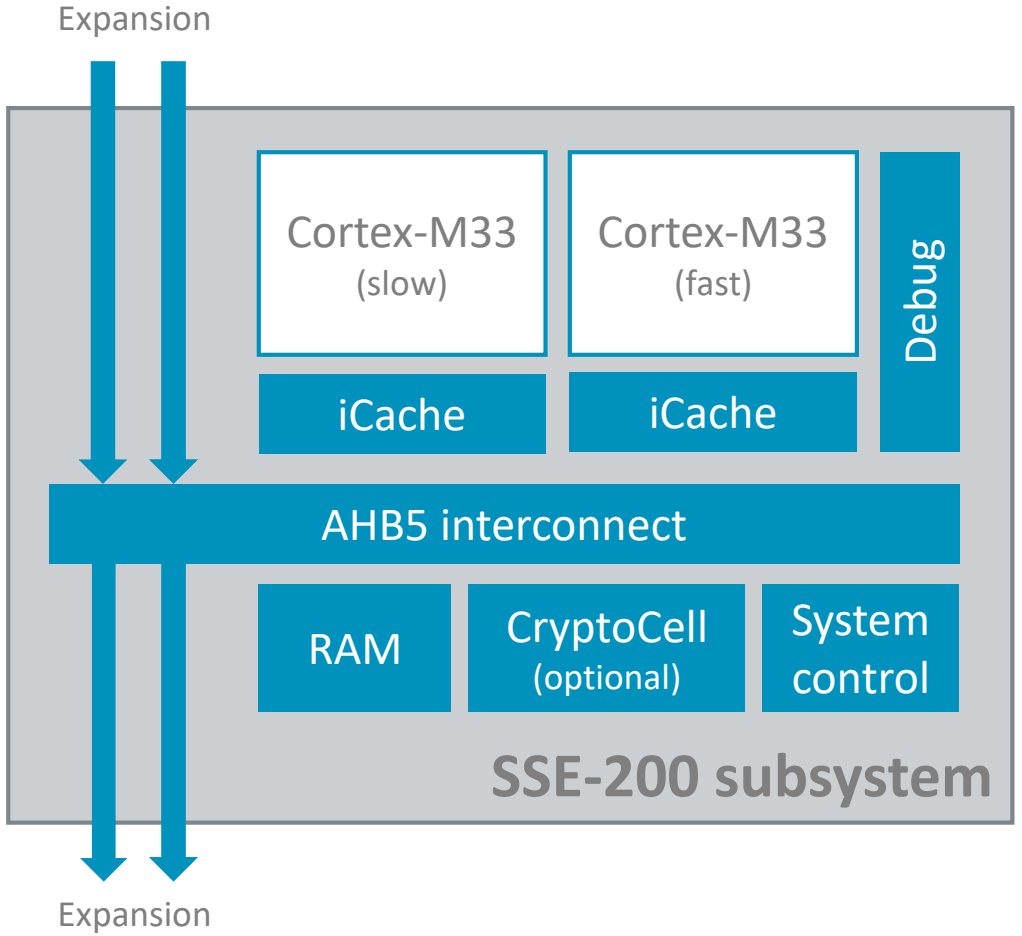
Using Cortex-M33

- Armv8-M architecture

Built for IoT

- Fine-grain power control
- Asymmetric processing
- Always-on domain

PSA ready



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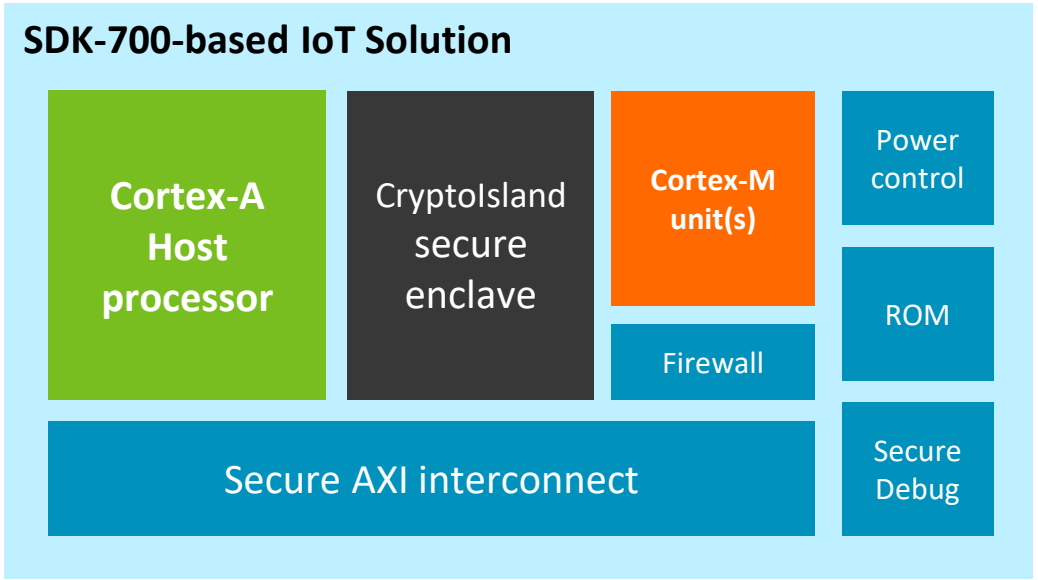
Arm SDK-700 System Design Kit

A new flexible SoC solution for rich IoT nodes and gateways

- Flexible compute
  - Arm® Cortex®-A – performance & rich OS
  - Arm Cortex-M – real-time & highest efficiency
- Secure SoC foundation
  - Supports Microsoft Azure Sphere
- Built on PSA principles
  - Secure system architecture
  - Common software architecture



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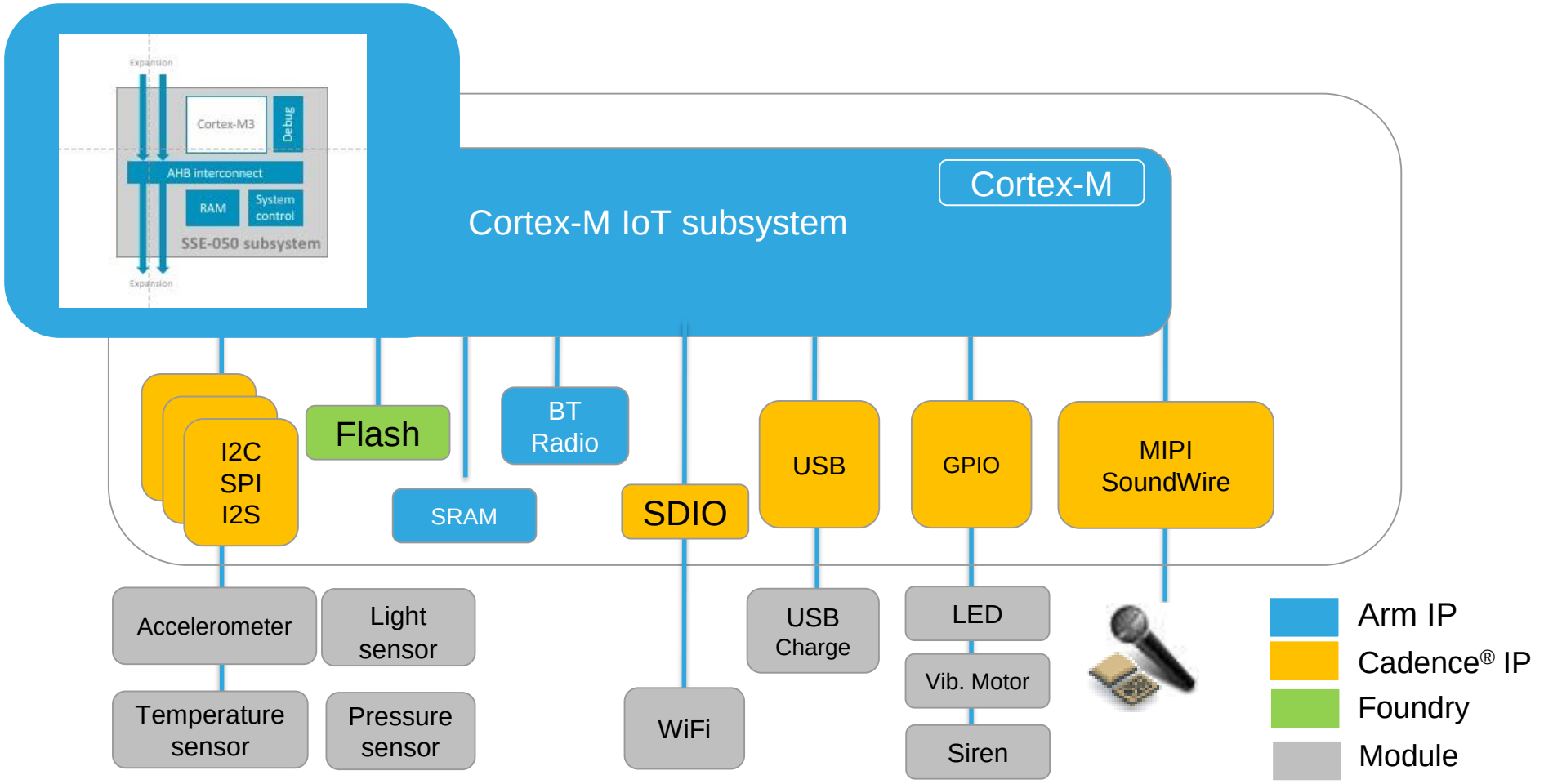
Extending Arm's subsystem with Cadence IoT IP



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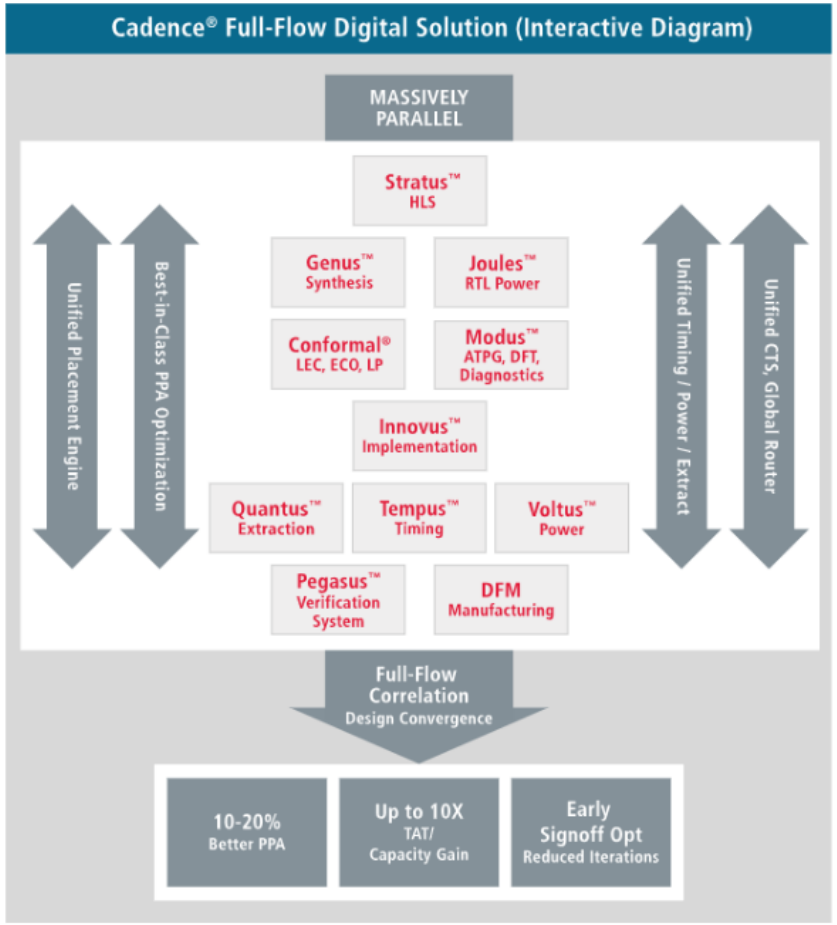
Cadence Rapid Adoption Kit (RAK) for Arm Cortex-M23 and Cortex-M33

- Quick path to implementation via a full-flow digital and signoff reference methodology that provides optimal power, performance and area (PPA)
- Achieve fast runtimes and efficient design closure through the integrated Cadence RTL2GDS
- Implement IoT devices using the complete Cadence low-power flow: design, verification, implementation



For accessing Cadence RAKs, contact your local Cadence office and support AE

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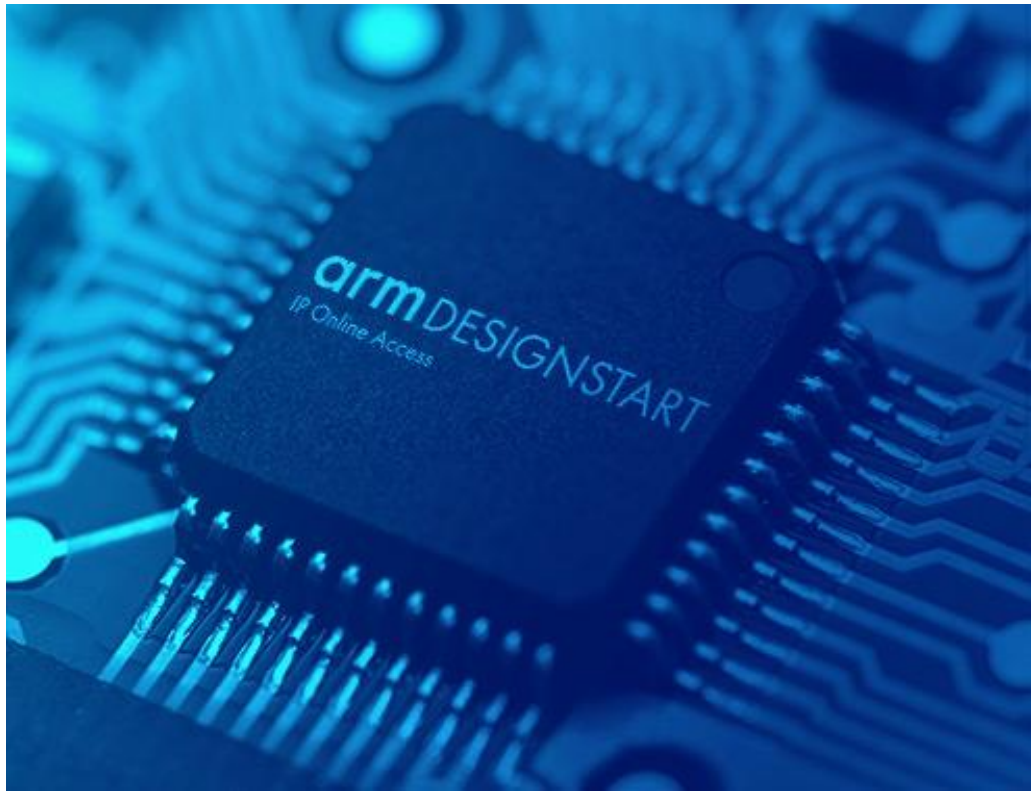
Building a chip yourself? Use Arm DesignStart™ portal

Fast access to industry-leading processor IP and physical IP – for no upfront fee



- Simple, quick web-based access to Arm IP
- Leading Cortex-M processors and subsystems
- System design kits with pre-verified subsystems for faster development
- Access to Cadence tools, support, and methodologies in Hosted Design Solution chamber
- 1000s of physical IP libraries
- Used in 1000s of SoC designs

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designstart.arm.com

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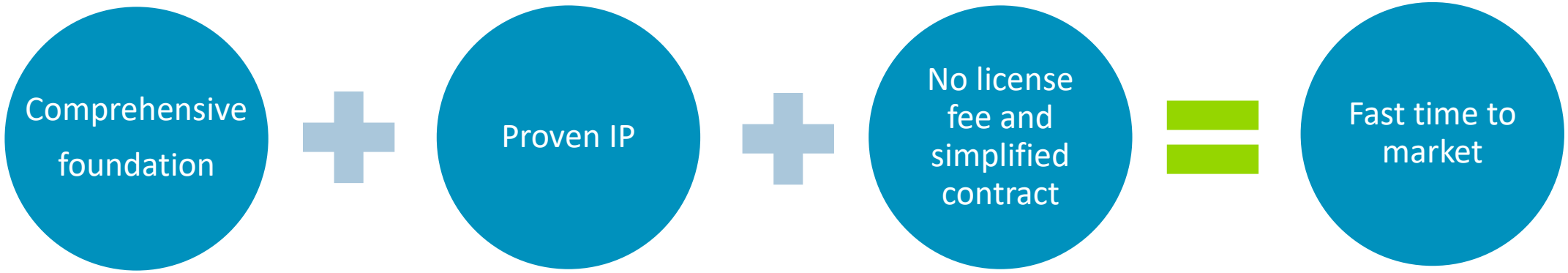
Case study: Speeding time to market with proven Arm IP

EIGENCOMM
More than connection



Focused on value-added activities: the transceiver

Success at first tapeout

Saved time and reduced upfront investment

6 months from start to tapeout

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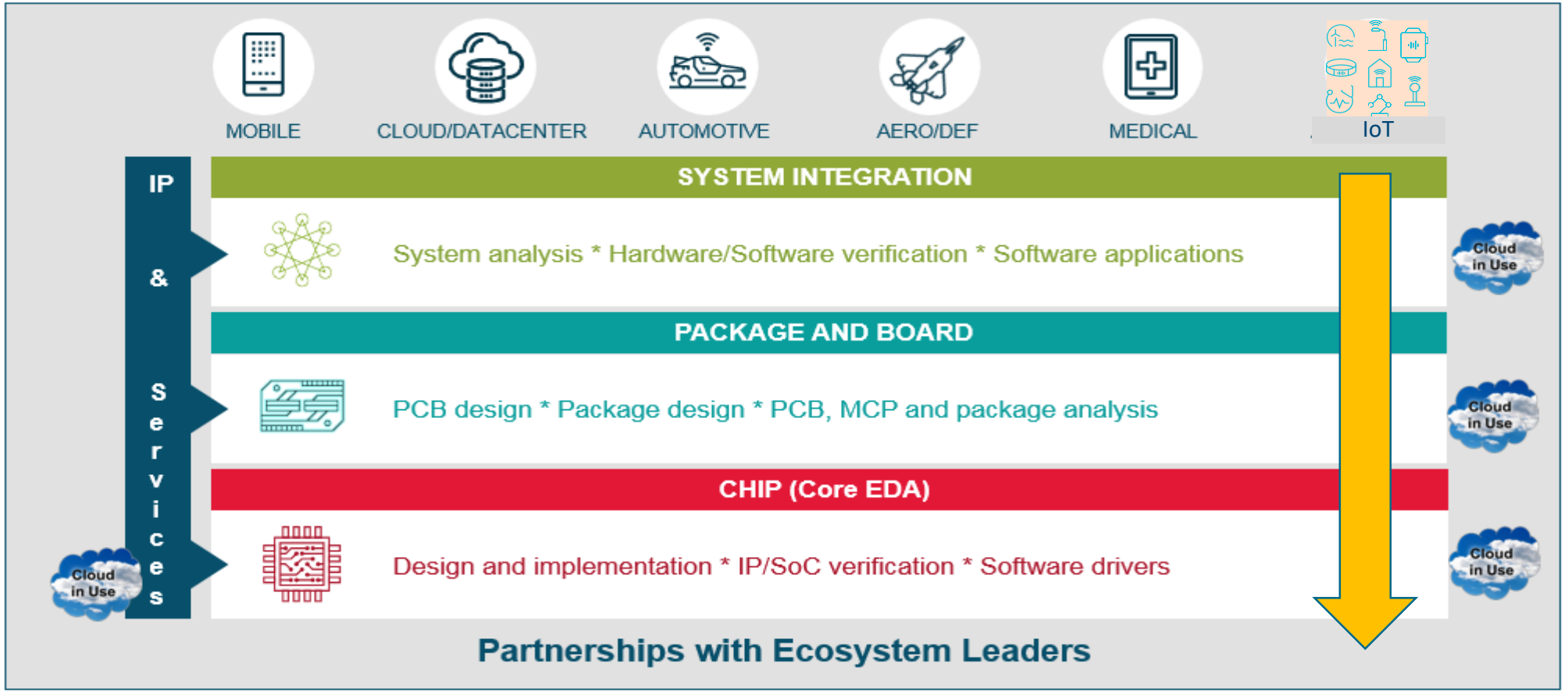
Cadence System Design Enablement

Holistic and scalable design solution for enabling IoT differentiated products



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Cadence SDE: Vertical markets enablement

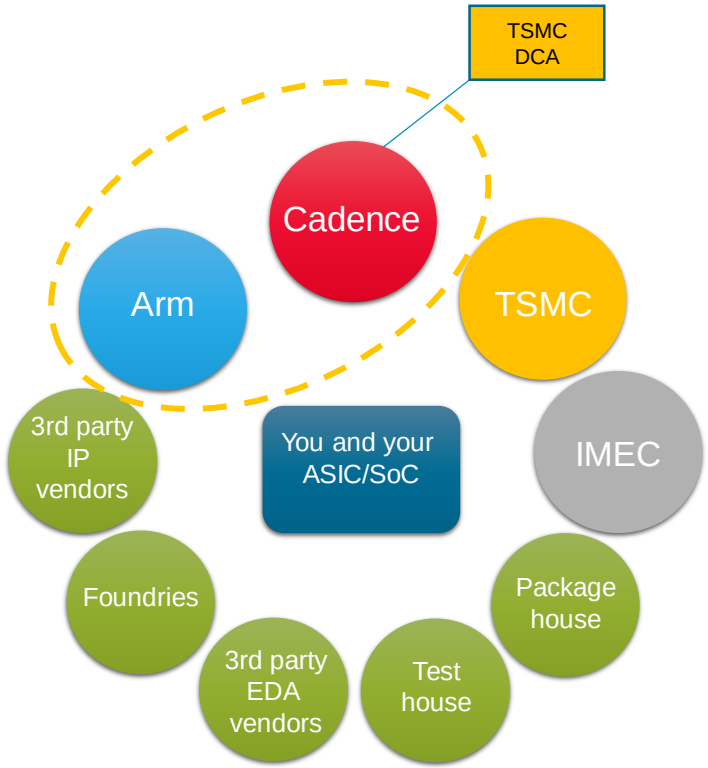
EMEA SDE Competency	Automotive	AI ML/DL	HPC	5G	Mil/Aero	Imaging	IoT
System architecture							
HW/SW partitioning							
HW emulation and acceleration							
IP and IP integration							
Design and verification							
Functional safety							
DFT							
Phys implementation and signoff							
Package and board							

Design Infrastructure

High-Speed Processor SS

Library Characterization

SCM (Interface)



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Reduce complexity, risk, and cost

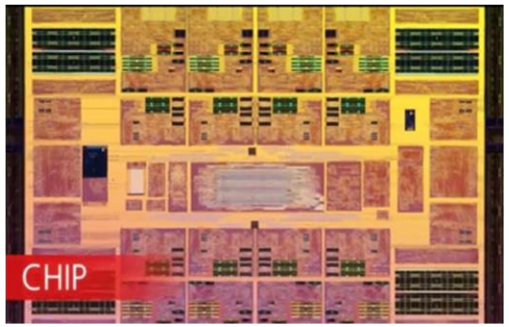
Concept Phase

System architecture

SoC Development

Prototyping

Design



Verification

Implementation

CAD foundation
(EDA SW)

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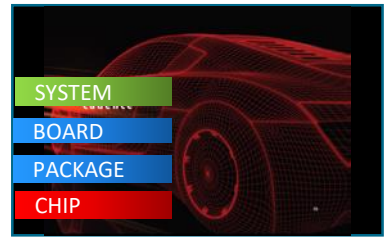
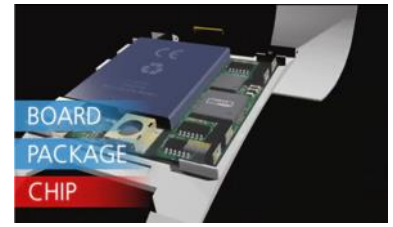
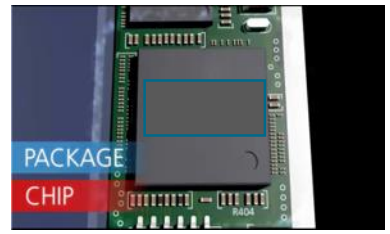
CLOUD-HOSTED
DESIGN SOLUTION

System Integration







BOM

Functionality

Software

Hardware

Customer Product

PPA

IP

BOM

SoC Architecture → SoC Design & Implementation → Silicon Bring Up & System Integration

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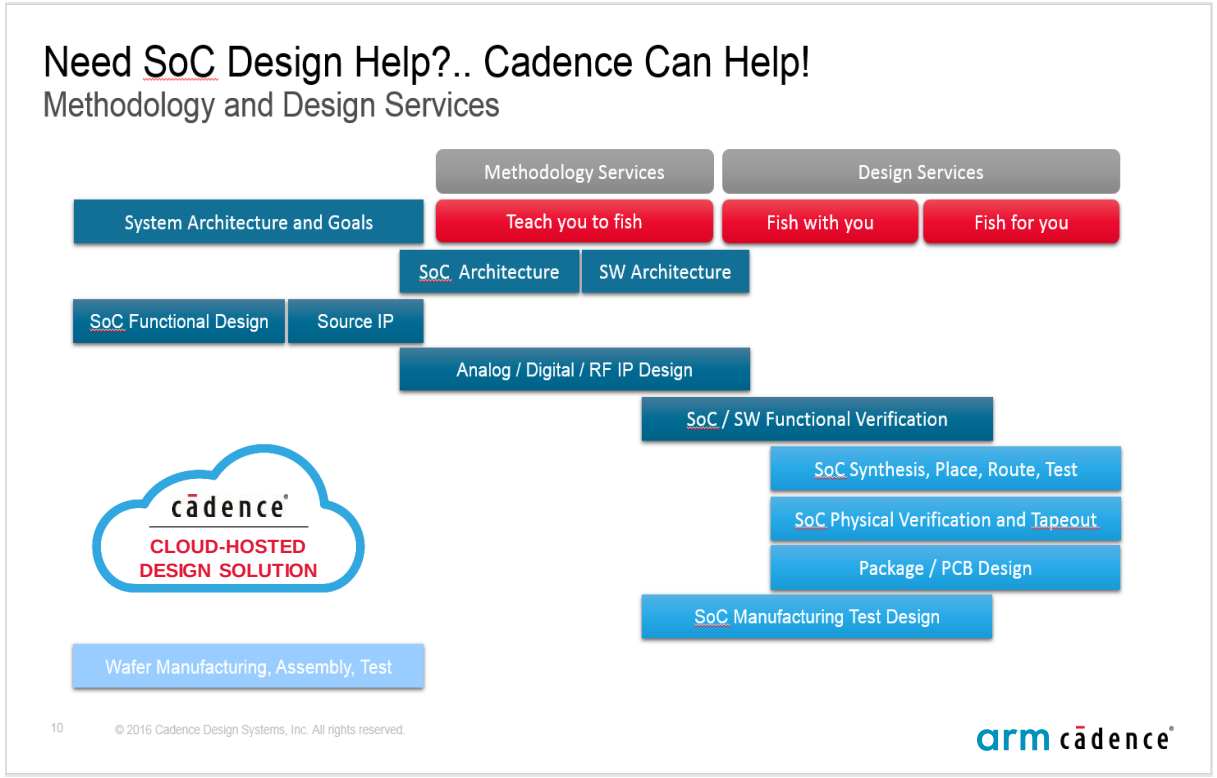
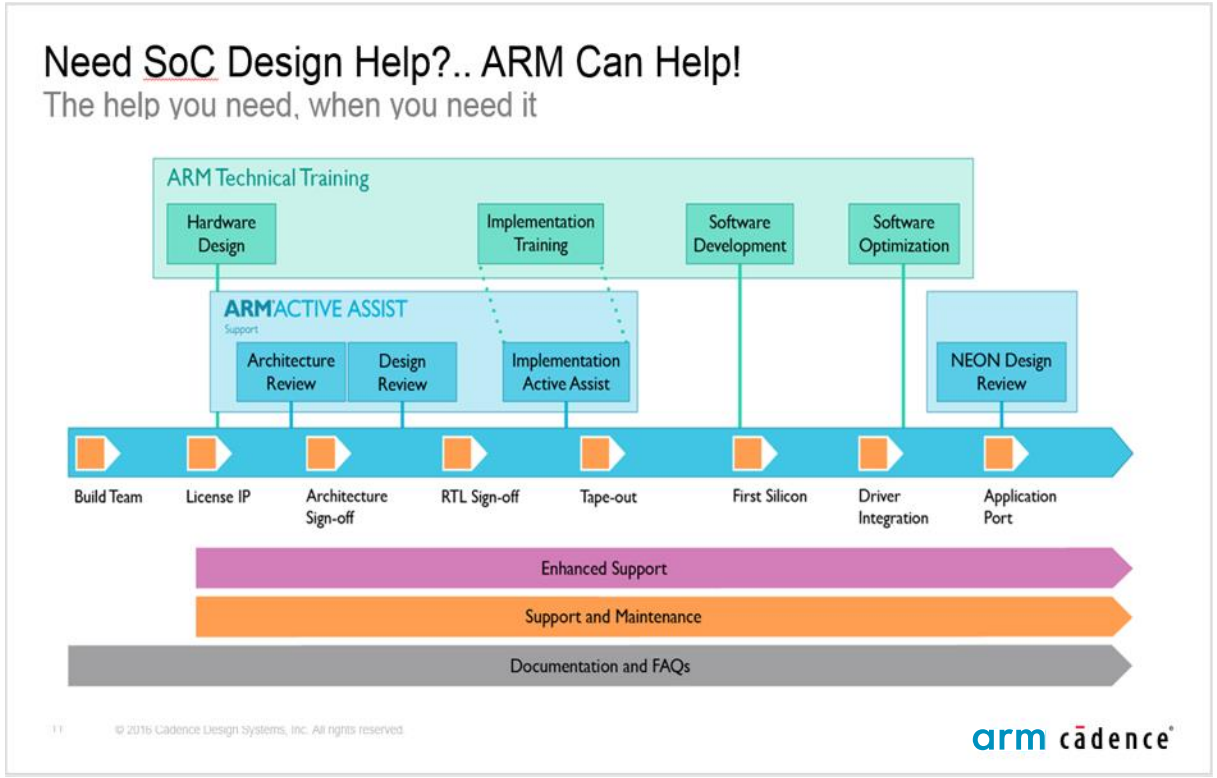
Cadence and Arm Design Enablement

Need SoC design help?





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Some key risks in ASIC/SoC design – Cadence can help you

Risk area	Cadence offers
• Design complexity rising	• One of the strongest SoC verification methodology & services teams in the industry
• RTL-GDSII implementation	• RTL-GDSII implementation methodology • 200+ tapeouts in last 5 years, spanning 180nm to 3nm! Many Arm-based designs.
• IC-package-board co-design	• SI/PI/thermal analysis and optimization
• Hardware-software coherence	• SoCs stress testing
• Analog/mixed to digital interfacing	• Analog/mixed-signal/RF design & verification
• IP integration	• A broad IP portfolio with integration support

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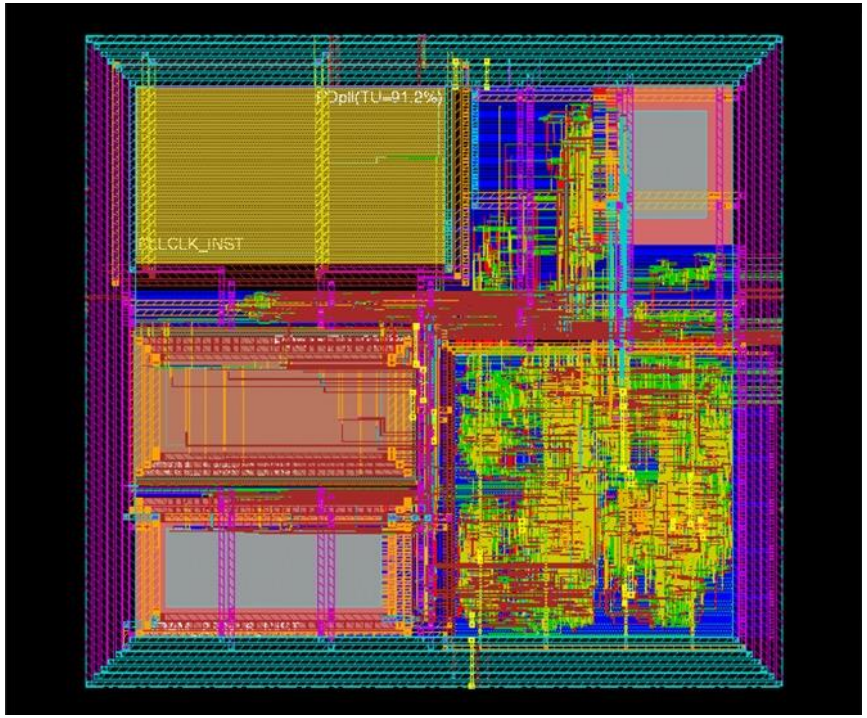
There is mixed signal in IoT



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System(s)-on-a-Chip*: Changes in SoC Design Methodology*

Reasons for re-spins in analog mixed-signal SoCs

1. Logical and functional errors
2. Clocking issues
3. Analog–digital interfaces
4. Crosstalk
5. Power management
6. Analog circuits
7. Yield/reliability
8. Timing
9. Firmware
10. IR drops

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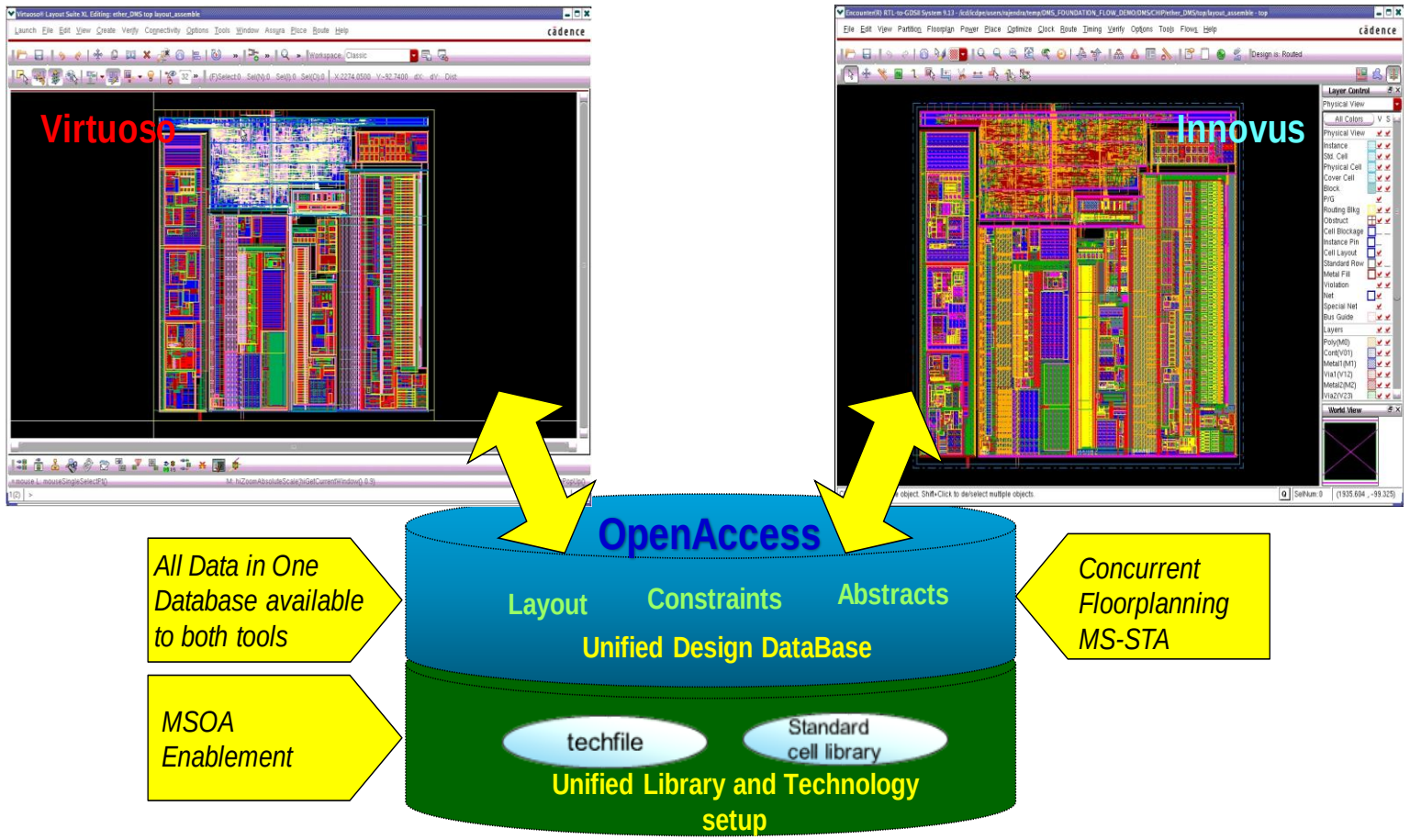
Cadence solution for mixed signal

Cadence Mixed-Signal Flow has produced many thousands of successful tapeouts



Cadence Mixed-Signal Methodology Guide

ISBN: 978-1300035206

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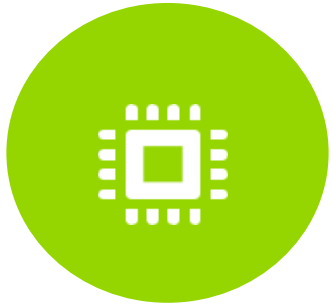
IoT is quicker, easier and more flexible with Arm Cadence design solutions

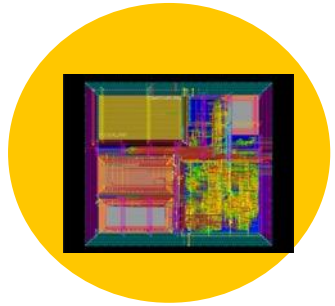
Low power, scalable compute

Security, identity & platform security architecture



Configurable SoC frameworks

OS & tools



Design assistance

Arm: System-level solutions to simplify IoT development and deployment: Secure, scalable, configurable, and power efficient

Cadence: Low-power solution, IoT System Design Enablement (IP, software, hardware, methodology, design services), cloud-hosted design solution

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Thank You
Danke
Merci
谢谢
ありがとう
Gracias
Kiitos
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